CY7C191
CY7C192

64K x 4 Static RAM with Separate I/O

Features

- **High speed**
  — 12 ns
- **Transparent write (7C191)**
- **CMOS for optimum speed/power**
- **Low active power**
  — 880 mW
- **Low standby power**
  — 220 mW
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

Functional Description

The CY7C191 and CY7C192 are high-performance CMOS static RAMs organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

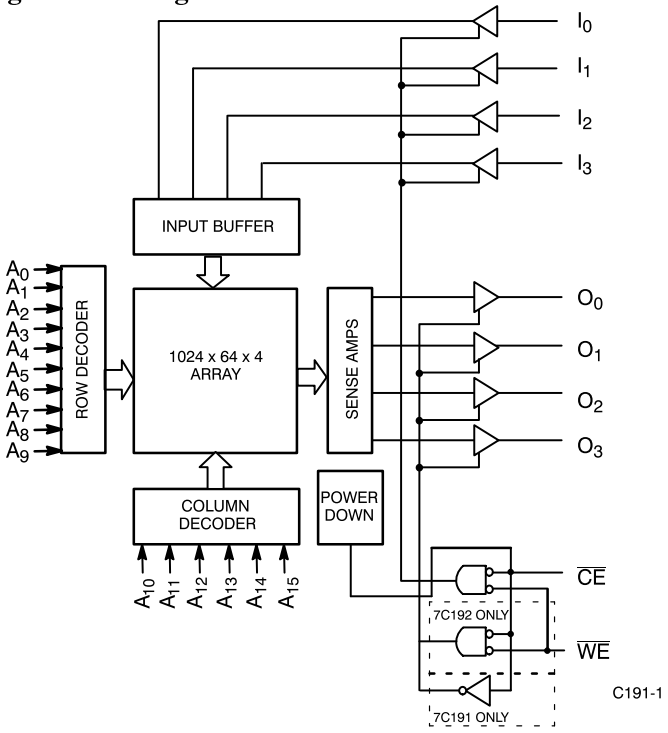
Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while the write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

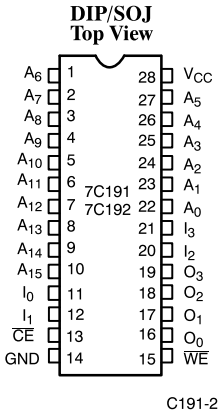
The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (CY7C192 only), or chip enable ($\overline{CE}$) is HIGH.

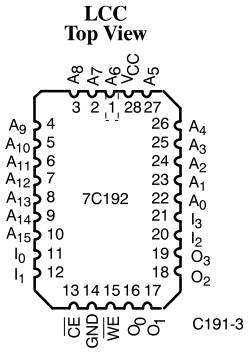
A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations





Selection Guide

		7C191–12 7C192–12	7C191–15 7C192–15	7C191–20 7C192–20	7C191–25 7C192–25	7C191–35 7C192–35	7C191–45 7C192–45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	155	145	135	115	115	
	Military		160	150	125	125	125
Maximum Standby Current (mA)		30	30	30	30	30	30

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C191−12 7C192−12 Min.	7C191−12 7C192−12 Max.	7C191−15 7C192−15 Min.	7C191−15 7C192−15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		155		145	mA
			Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		10		10	mA
			Mil				15	

Shaded area contains advanced information.

Notes:

1. Minimum voltage is equal to − 2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Electrical Characteristics Over the Operating Range[3] (continued)

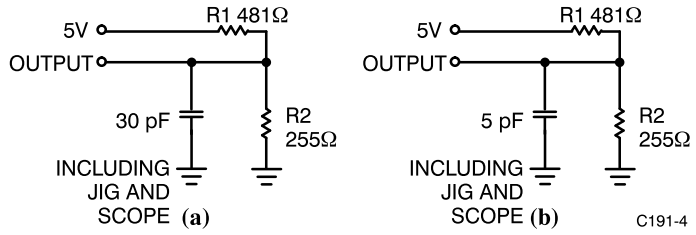
Parameter	Description	Test Conditions		7C191−20 7C192−20 Min.	7C191−20 7C192−20 Max.	7C191−25, 35, 45 7C192−25, 35, 45 Min.	7C191−25, 35, 45 7C192−25, 35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3V	2.2	V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		135		115	mA
			Mil		150		125	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≤ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			15		15	mA

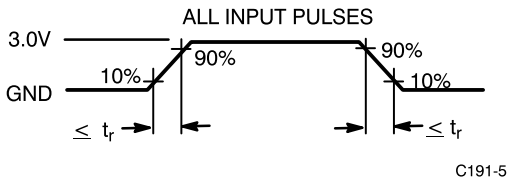
Shaded area contains advanced information.

Capacitance[5]

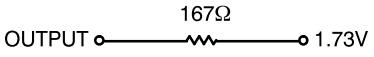
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[6]





Equivalent to: THÉVENIN EQUIVALENT



Notes:
5. Tested initially and after any design or process changes that may affect these parameters.
6. t_r = ≤ 3 ns for the −12 and −15 speeds. t_r = ≤ 5 ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3,7]

Parameter	Description	7C191−12 7C192−12		7C191−15 7C192−15		7C191−20 7C192−20		7C191−25 7C192−25		7C191−35 7C192−35		7C192−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,9]		5		7		9		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35		45	ns
WRITE CYCLE[10]														
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		18		22		22		ns
t_{AW}	Address Set-Up to Write End	9		10		15		20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		9		15		18		22		22		ns
t_{SD}	Data Set-Up to Write End	8		9		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z (7C192)[8]	3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z (7C192)[8,9]		7		7		10		11		15		15	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C191)		12		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C191)		12		15		20		20		30		35	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C191)		12		15		20		25		35		45	ns

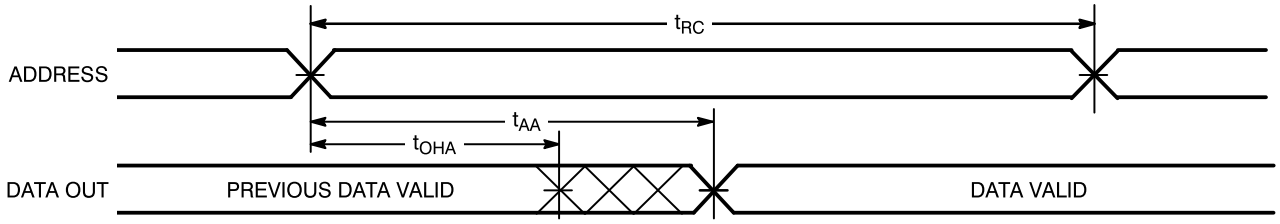
Shaded area contains advanced information.

Notes:

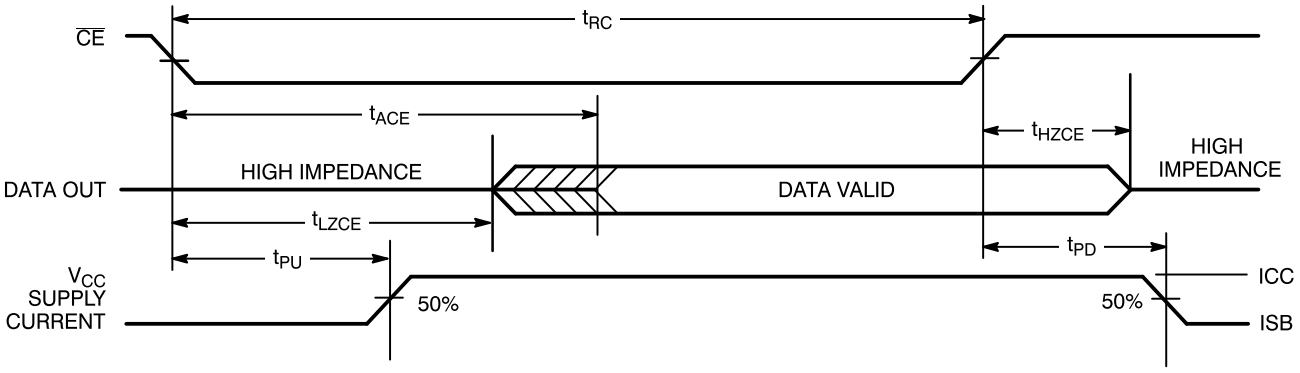
7. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 through −45 speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZWE} is less than t_{LZWE} for any given device. These parameters are guaranteed by design and not 100% tested.
9. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

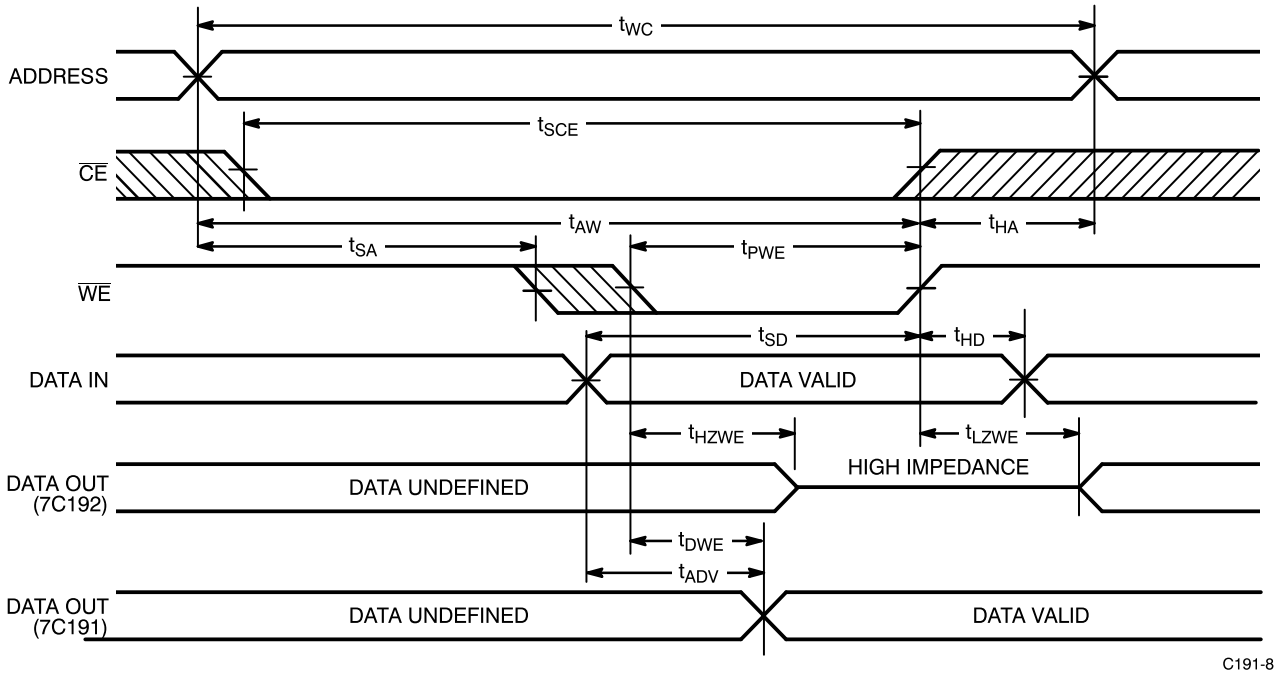
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



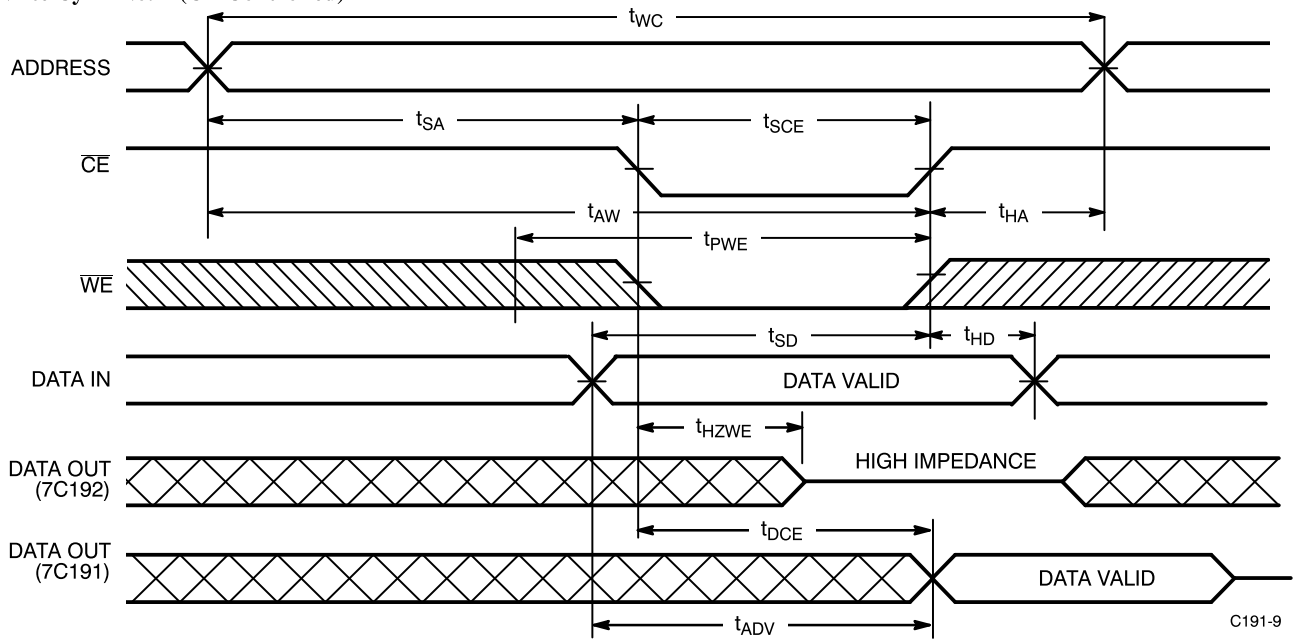
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



Notes:
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C192 only).

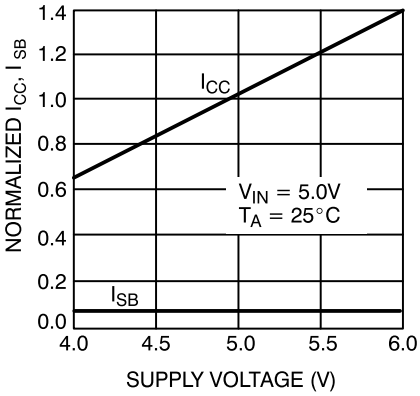
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 14]

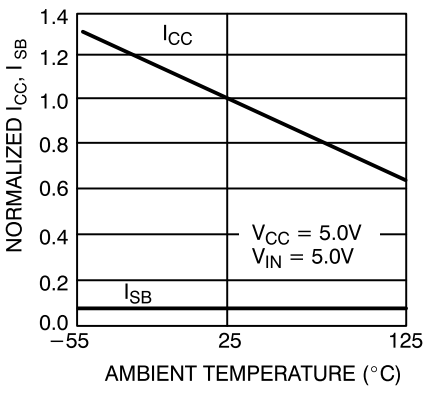


Typical DC and AC Characteristics

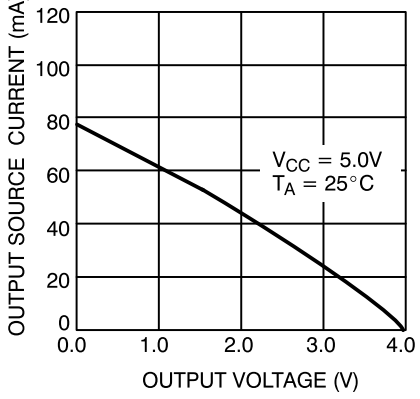
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



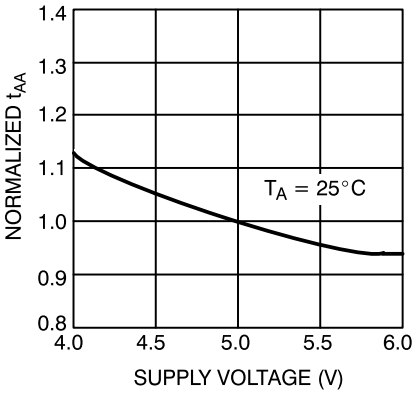
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



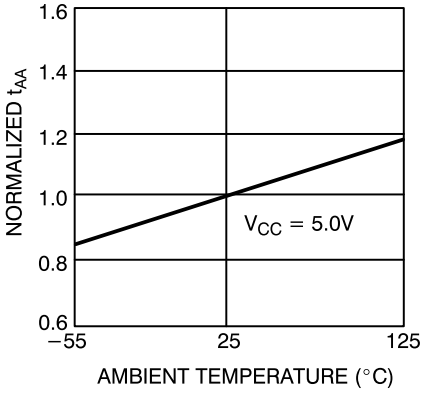
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



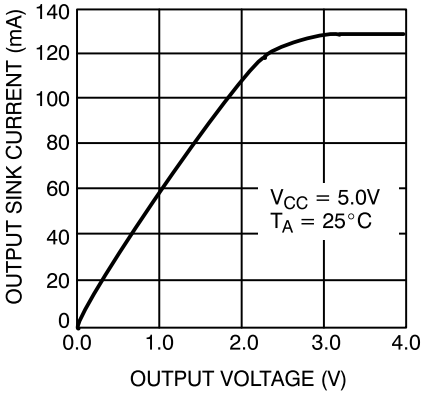
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

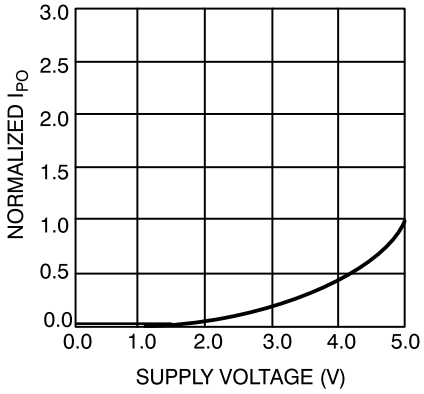


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

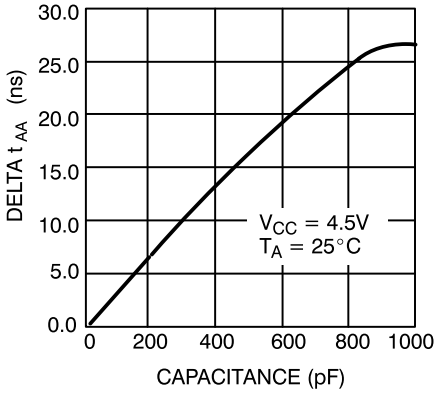


Typical DC and AC Characteristics (continued)

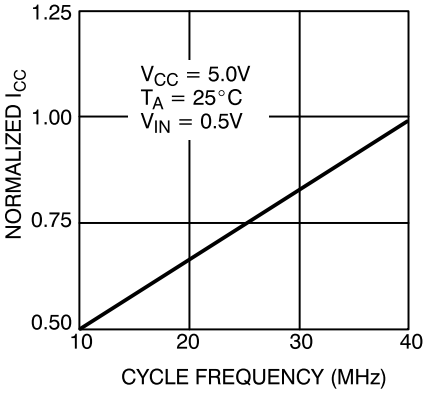
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C191−12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191−12VC	V21	28-Lead Molded SOJ	
15	CY7C191−15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C191−15VC	V21	28-Lead Molded SOJ	
20	CY7C191−20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
25	CY7C191−25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
35	CY7C191−35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial

Shaded area contains advanced information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C192−12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192−12VC	V21	28-Lead Molded SOJ	
15	CY7C192−15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192−15VC	V21	28-Lead Molded SOJ	
	CY7C192−15DMB	D22	28-Lead (300-Mil) CerDIP	Military
20	CY7C192−20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192−20VC	V21	28-Lead Molded SOJ	
	CY7C192−20DMB	D22	28-Lead (300-Mil) CerDIP	Military
25	CY7C192−25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192−25VC	V21	28-Lead Molded SOJ	
	CY7C192−25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192−25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C192−35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C192−35VC	V21	28-Lead Molded SOJ	
	CY7C192−35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192−35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C192−45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C192−45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

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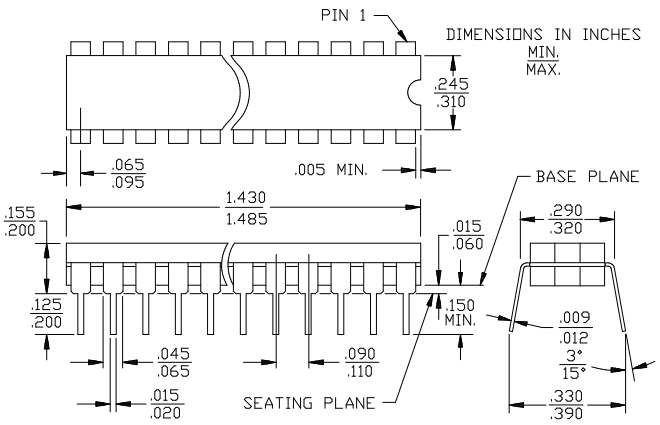
Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

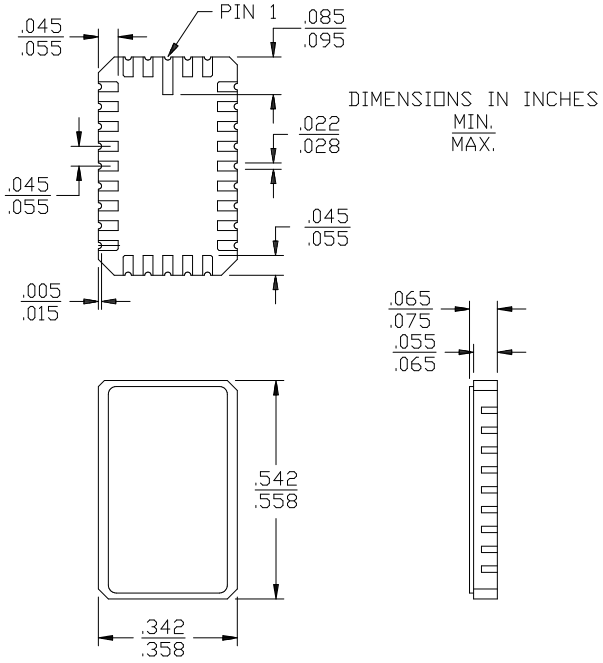
Note:
15. CY7C191 only

Package Diagrams

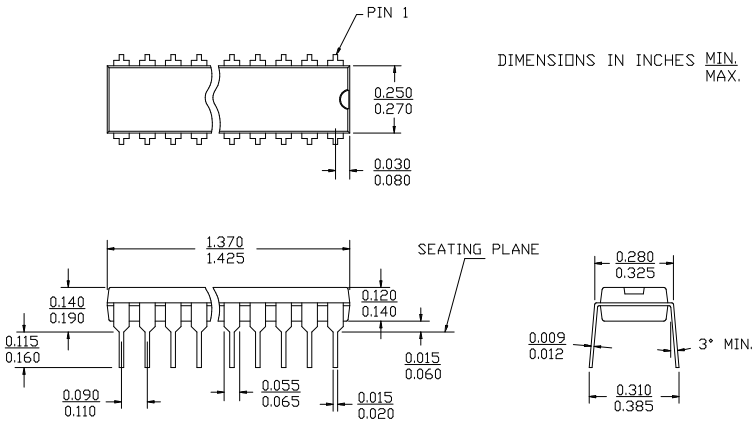
28-Lead (300-Mil) CerDIP D22
MIL−STD−1835 D−15 Config. A



28-Pin Rectangular Leadless Chip Carrier L54
MIL−STD−1835 C−11A



28-Lead (300-Mil) Molded DIP P21



Package Diagrams (continued)

28-Lead Molded SOJ V21