CY7C193

32K x 8 Synchronous SRAM

Features

- **Synchronous 32K x 8 SRAM**
- **Supports 33-MHz 486 cache systems with zero wait states**
- **Clock-to-output time**
  — 20 ns into 30 pF
- **Synchronous self-timed write**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{OE}$ feature**

Functional Description

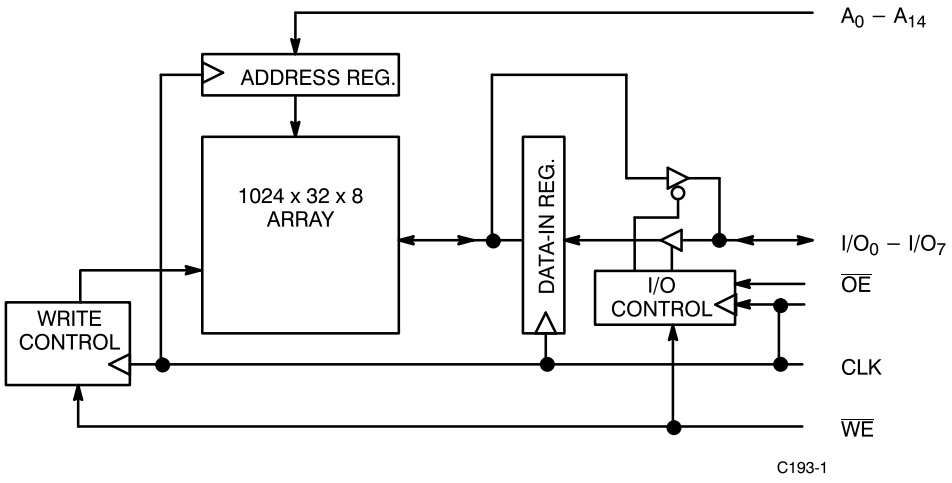
The CY7C193 is a synchronous 32K x 8 SRAM designed to allow zero-wait-state cache designs, both write back and write through, in microprocessor-based systems with 33-MHz bus speeds. The SRAM has a fast clock-to-output time of 20 ns into a load of 30 pF. The address, data, and $\overline{WE}$ signals are all synchronous, while the $\overline{OE}$ signal is asynchronous.

If $\overline{WE}$ is sampled HIGH at the rising edge of CLK (signifying a read cycle), the address is captured in the on-chip address register. The data is then driven out a maximum of 20 ns later (if the load on the data lines is 30 pF) allowing ample time for the data to be set up to the next rising edge of the clock in a 33-MHz cache system. If the load on the data lines is less than 30 pF, the clock-to-output time will be faster than 20 ns. See the derating curve at the end of the datasheet for details. The output data can also be controlled asynchronously by $\overline{OE}$. The data I/O lines will switch from outputs to inputs (i.e., to the high-impedance state) within 7 ns of $\overline{OE}$ going HIGH. Valid data will be driven back out within 10 ns of $\overline{OE}$ going LOW again.

If the $\overline{WE}$ signal is sampled LOW at the rising edge of CLK (signifying a write cycle), the address is captured in the on-chip address register and the data to be written is captured in the data-in register. The CY7C193 then performs a synchronous self-timed write of the data to the specified location. The data I/O lines should be put into the high-impedance state by bringing $\overline{OE}$ HIGH before the data to be written is driven in to the SRAM.

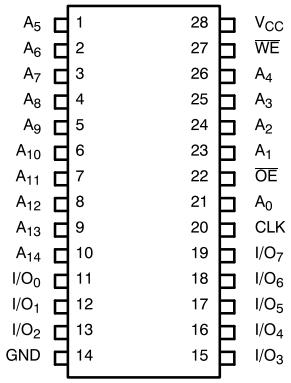
Although the CY7C193 is ideally suited for 33-MHz 486-based cache systems, it is very useful in many other applications as well. The synchronous address and data interface, along with the synchronous self-timed write feature, simplify designs of almost any system.

Logic Block Diagram



Pin Configuration

DIP/SOJ
Top View



Selection Guide

		7C193–20
Maximum Access Time (ns)		20
Maximum Operating Current (mA)	Commercial	160

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage ..... − 0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

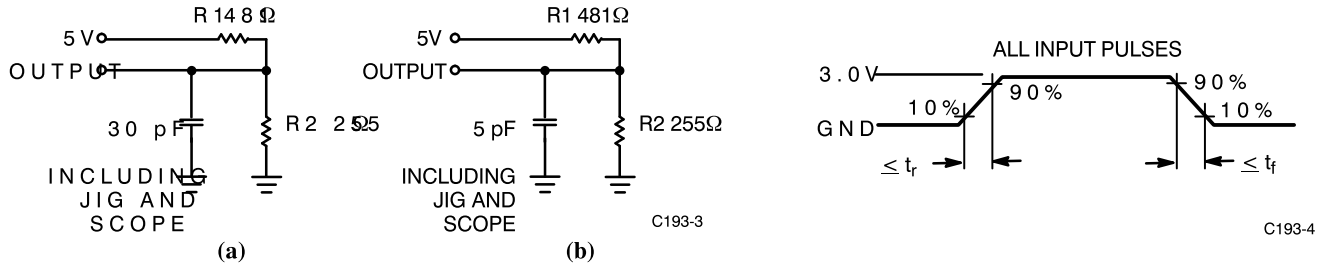
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C193−20		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−5	+5	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		160	mA

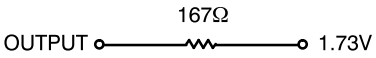
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[1, 3]

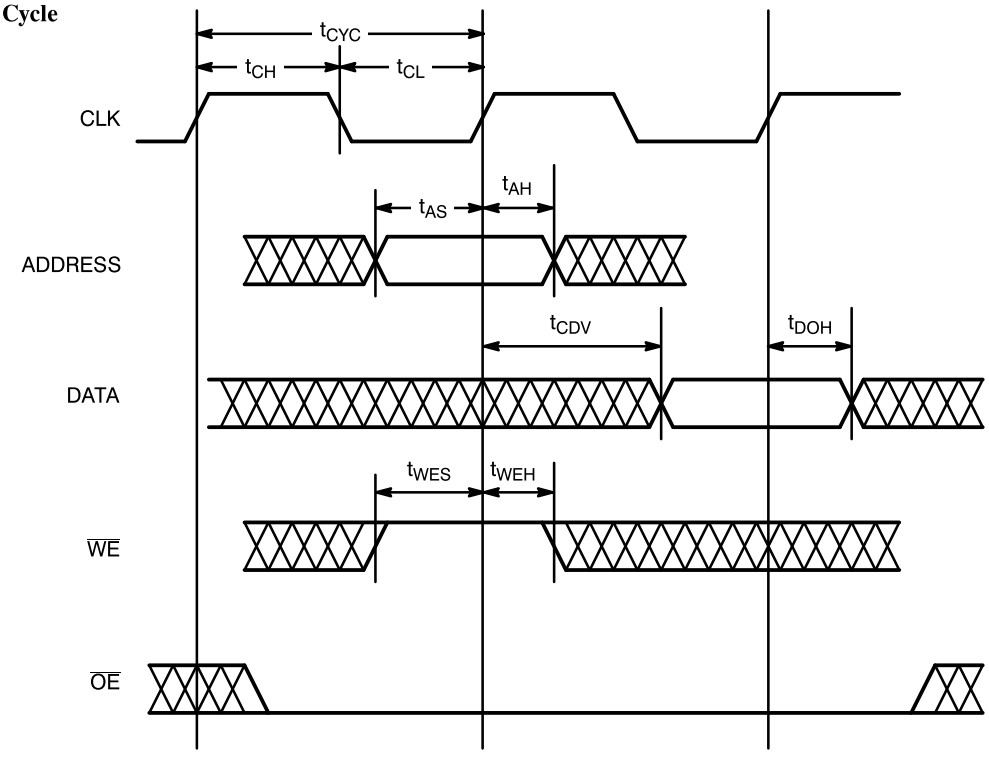
Parameter	Description	7C193–20		Unit
		Min.	Max.	
t_{CYC}	Clock Cycle Time	30		ns
t_{CH}	Clock Pulse Width High	11		ns
t_{CL}	Clock Pulse Width Low	11		ns
t_{CDV}	Clock Rise to Data Output Valid		20	ns
t_{DOH}	Data Output Hold after Clock Rise	3		ns
t_{AS}	Address Setup Before Clock Rise	5		ns
t_{AH}	Address Hold After Clock Rise	1		ns
t_{WES}	$\overline{WE}$ Setup Before Clock Rise	5		ns
t_{WEH}	$\overline{WE}$ Hold After Clock Rise	1		ns
t_{DS}	Data Input Setup Before Clock Rise	5		ns
t_{DH}	Data Input Hold After Clock Rise	1		ns
t_{DOE}	$\overline{OE}$ Low to Output Valid		9	ns
t_{HZOE}	$\overline{OE}$ High to Output High-Z[4, 5]		7	ns
t_{WEHZ}	$\overline{WE}$ Sampled Low to Output High-Z[4]		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[5]	0		
t_{CLZ}	Clock Rise to Low-Z	8		

Notes:

3. Test conditions assume signal transition time (t_r, t_f) of 3 ns or less, timing reference level of 1.5V, input pulse level of 0 to 3.0V, and outputs loading per specified I_{OH}/I_{OL}, outputs loaded with 30 pF per (a) in AC Test Loads and Waveforms.
4. t_{HZOE} and t_{WEHZ} are specified with 5 pF capacitive load per (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZOE} is less than t_{LZOE} and t_{WEHZ} is less than t_{CLZ} for any given device.

Switching Waveforms

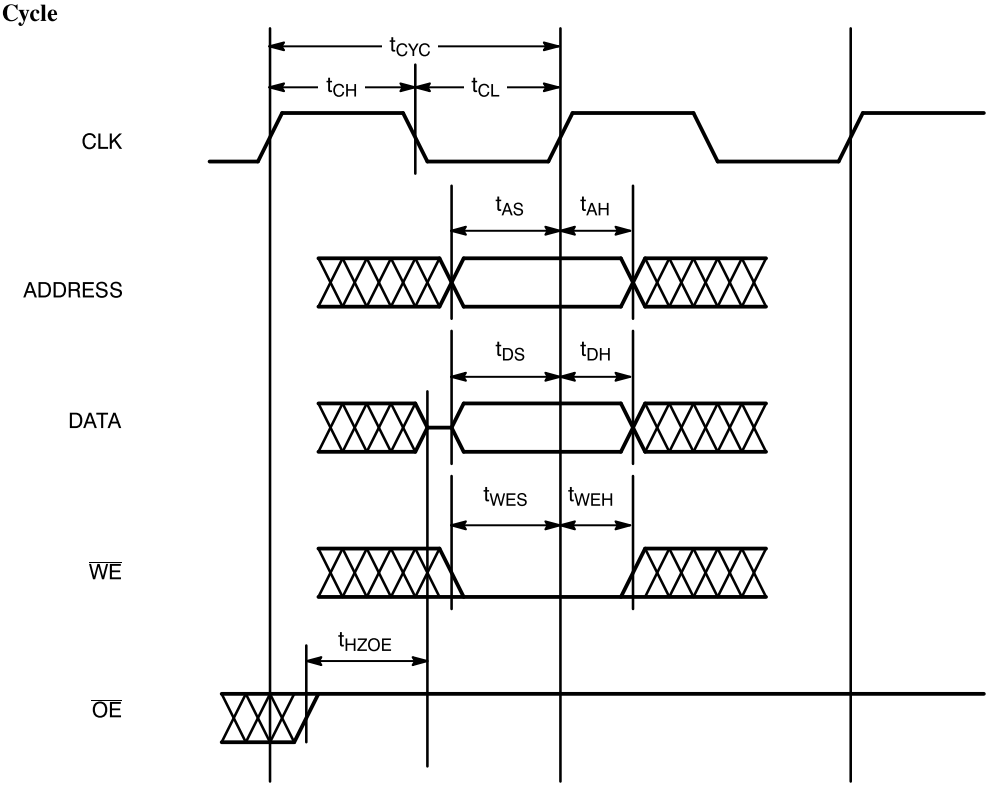
Read Cycle



C193-5

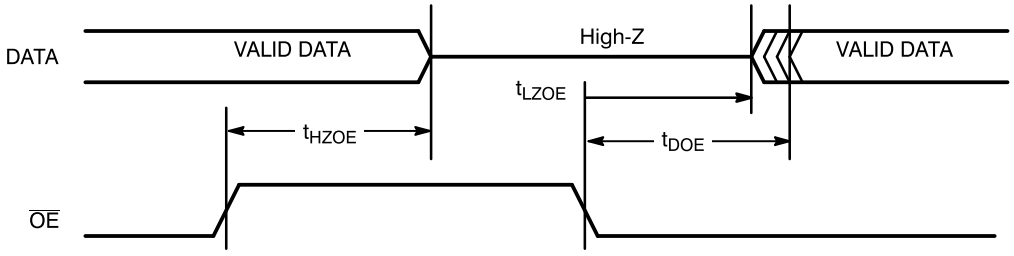
Switching Waveforms (continued)

Write Cycle



C193-6

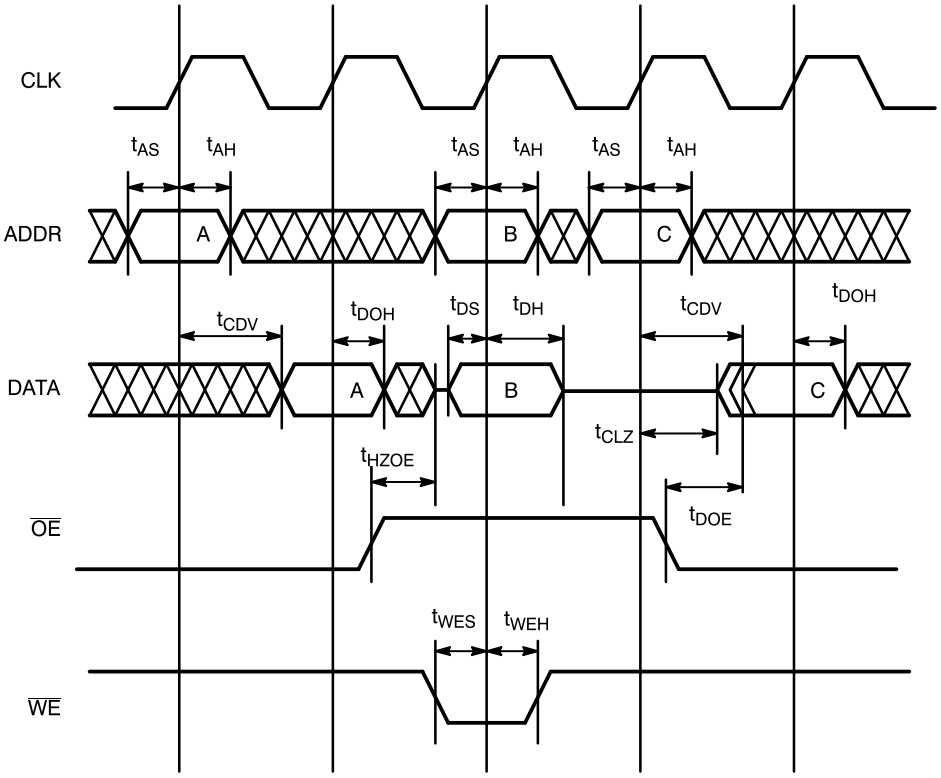
OE Timing



C193-7

Switching Waveforms (continued)

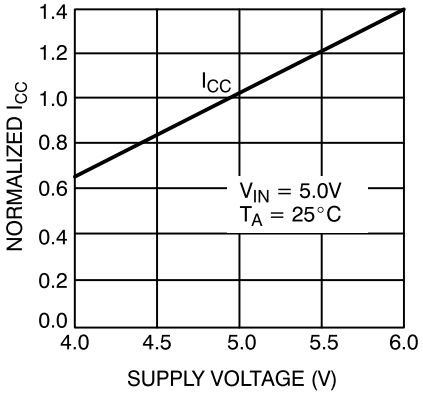
Read-Write-Read Timing



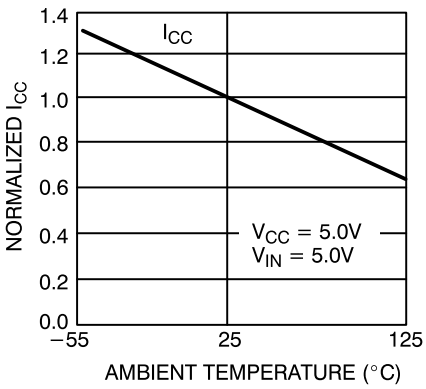
C193-8

Typical DC and AC Characteristics

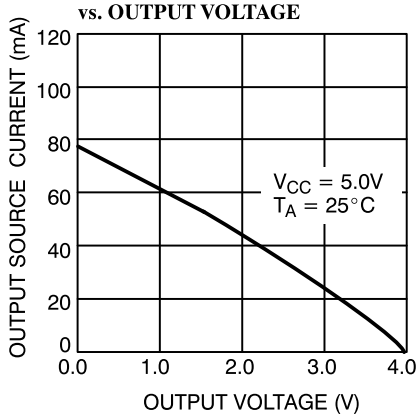
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



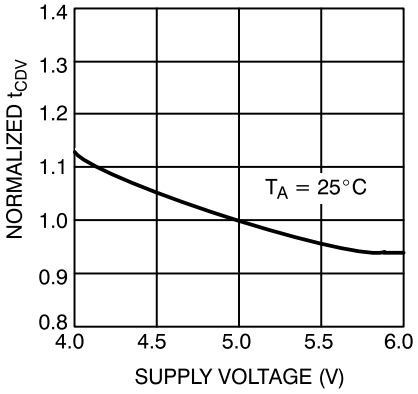
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



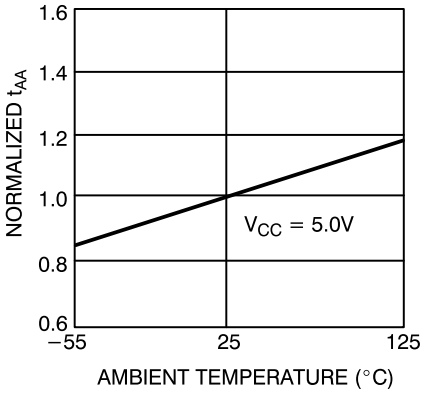
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



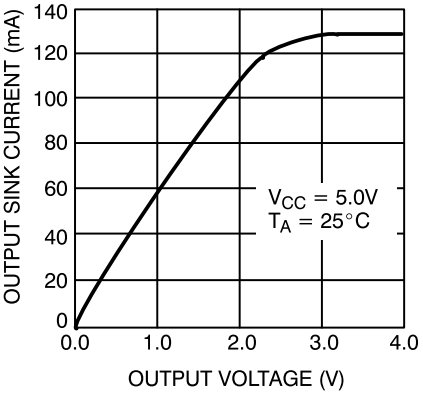
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



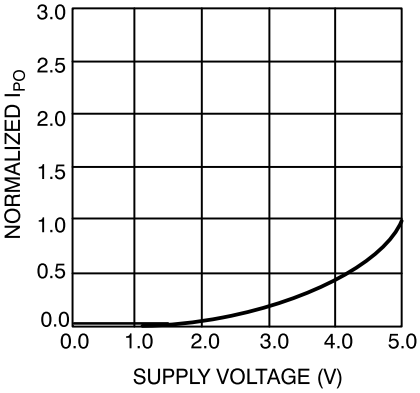
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



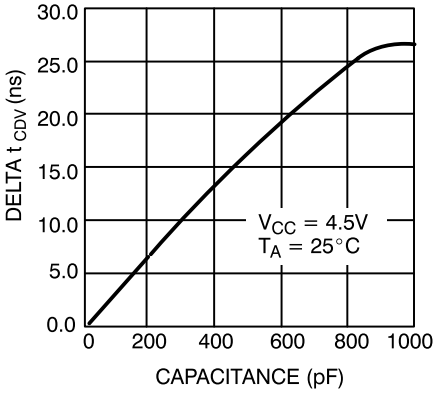
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



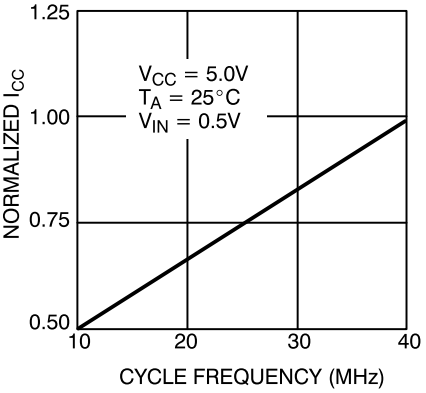
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



CY7C193

Ordering Information

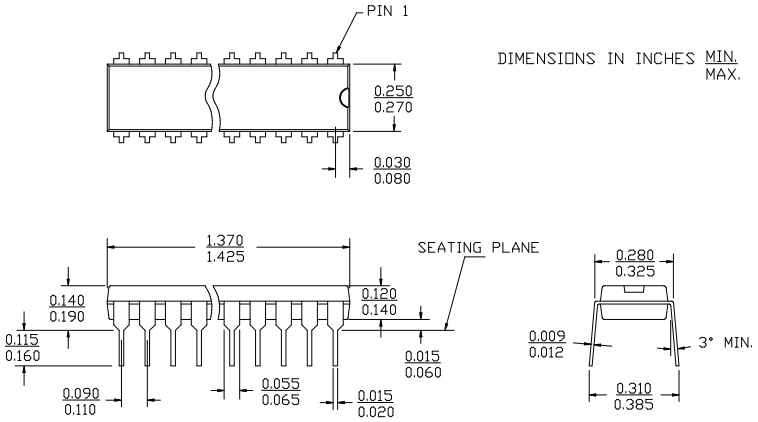
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C193−20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C193−20VC	V21	28-Lead Molded SOJ	

Shaded area contains preliminary information.

Document #: 38−00254−A

Package Diagrams

28-Lead (300-Mil) Molded DIP P21



28-Lead (300-Mil) Molded SOJ V21