CY7C199

32K x 8 Static RAM

Features

- **High speed**
  — 12 ns
- **Fast t_{DOE}**
- **CMOS for optimum speed/power**
- **Low active power**
  — 880 mW
- **Low standby power**
  — 165 mW
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

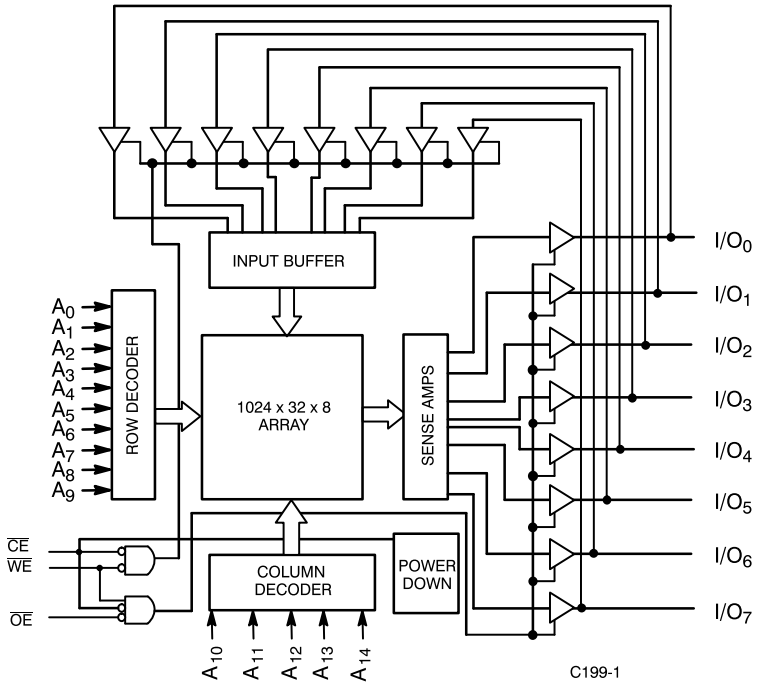
Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

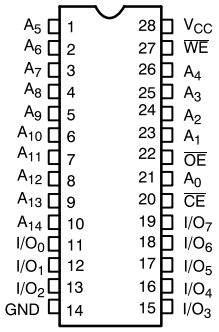
Logic Block Diagram



C199-1

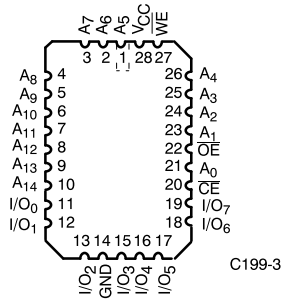
Pin Configurations

DIP/SOJ
Top View



C199-2

LCC
Top View



C199-3

Pin Configurations (continued)

TSOP
Top View

C199-4

Selection Guide

		7C199−10	7C199−12	7C199−15	7C199−20	7C199−25	7C199−35	7C199−45
Maximum Access Time (ns)		10	12	15	20	25	35	45
Maximum Operating Current (mA)	Com'l	160	160	155	150	150	140	
	L		130	110	100			
	Mil			180	170	150	150	150
	L			150	130			
Maximum Standby Current (mA)		30	30	30	30	30	25	25
	L		20	20	15			

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions	7C199−10		7C199−12		7C199−15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−5	+5	−5	+5	−5	+5	μA

Shaded area contains preliminary information.

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.

Electrical Characteristics Over the Operating Range[3] (continued)

Parameter	Description	Test Conditions		7C199−10 Min.	7C199−10 Max.	7C199−12 Min.	7C199−12 Max.	7C199−15 Min.	7C199−15 Max.	Unit
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Com'l		160		160		155	mA
			L				130		110	
			Mil						180	
			L						150	
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = f_{MAX}			30		30		30	mA
			L				20		20	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, f = 0	Com'l		10		10		10	mA
			L				100		100	μA
			Mil						15	mA
			L						5	

Shaded area contains preliminary information.

Electrical Characteristics Over the Operating Range[3] (continued)

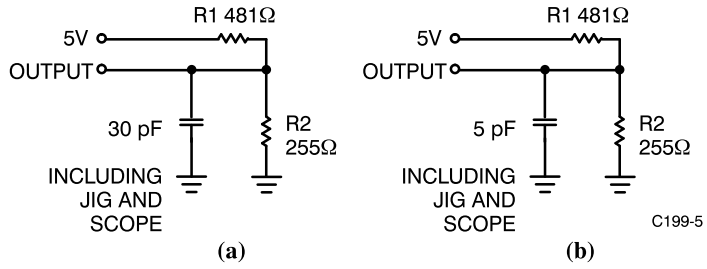
Parameter	Description	Test Conditions		7C199−20 Min.	7C199−20 Max.	7C199−25 Min.	7C199−25 Max.	7C199−35, 45 Min.	7C199−35, 45 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		−5	+5	−5	+5	−5	+5	μA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{CC}$, Output Disabled		−5	+5	−5	+5	−5	+5	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$	Com'l		150		150		140	mA
			L		100					
			Mil		170		150		150	
			L		130					
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, f = f_{MAX}			30		30		25	mA
			L		15					
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, f=0	Com'l		15		15		15	mA
			L		100					μA
			Mil		15		15		15	mA
			L		5					mA

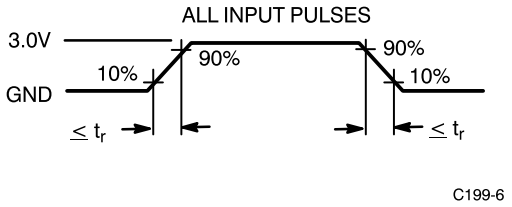
Note:
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance[5]

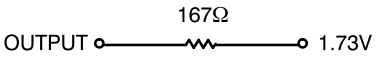
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms[6]





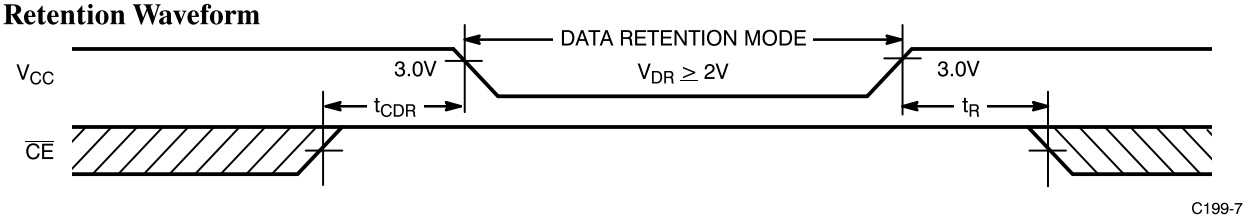
Equivalent to: THÉVENIN EQUIVALENT



Data Retention Characteristics Over the Operating Range (L version only)

Parameter	Description		Conditions[7]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l	$V_{CC} = V_{DR}$ = 2.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		10	µA
		Mil			100	
t_{CDR}[5]	Chip Deselect to Data Retention Time			0		ns
t_R[5]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform



Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. $t_r \leq 3$ ns for the −12 and −15 speeds. $t_r \leq 5$ ns for the −20 and slower speeds.

Switching Characteristics Over the Operating Range[3, 8]

Parameter	Description	7C199−10		7C199−12		7C199−15		7C199−20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		7		9	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		5		5		7		9	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		5		5		7		9	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE[11, 12]										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		9		10		15		ns
t_{AW}	Address Set-Up to Write End	7		9		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		9		15		ns
t_{SD}	Data Set-Up to Write End	5		8		9		10		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]		5		7		7		10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		3		3		3		ns

Shaded area contains preliminary information.

Notes:

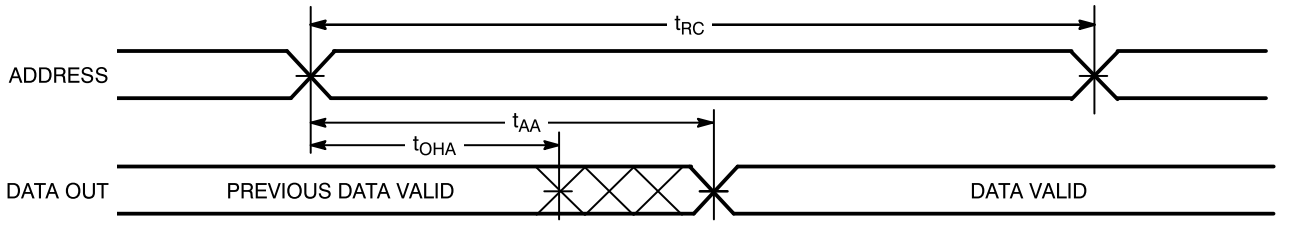
8. Test conditions assume signal transition time of 3 ns or less for −12 and −15 speeds and 5 ns or less for −20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics Over the Operating Range[3, 8] (continued)

Parameter	Description	7C199−25		7C199−35		7C199−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		16		16	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 10]		11		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9 ,10]		11		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
WRITE CYCLE[11, 12]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	18		22		22		ns
t_{AW}	Address Set-Up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		22		22		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]		11		15		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	3		3		3		ns

Switching Waveforms

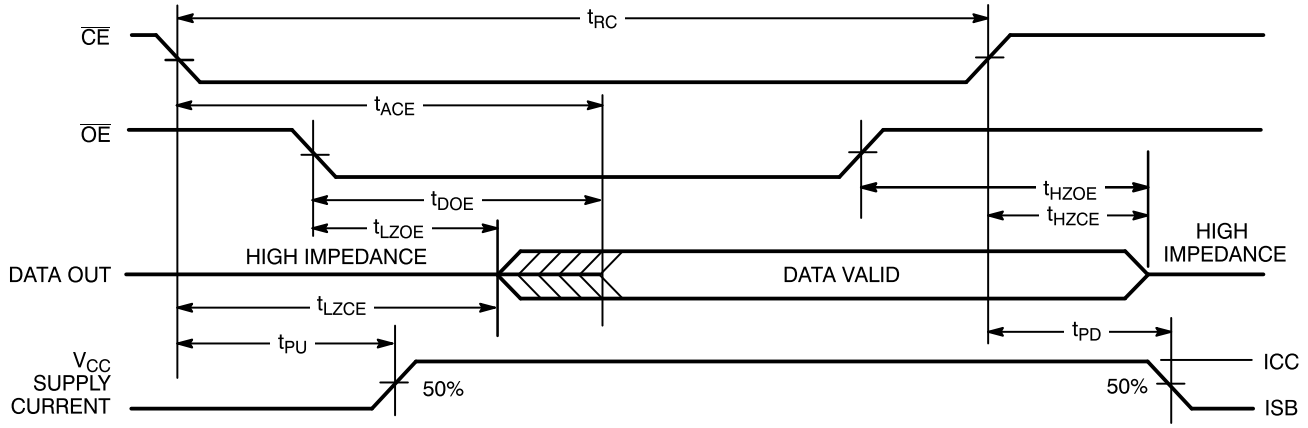
Read Cycle No. 1[13, 14]



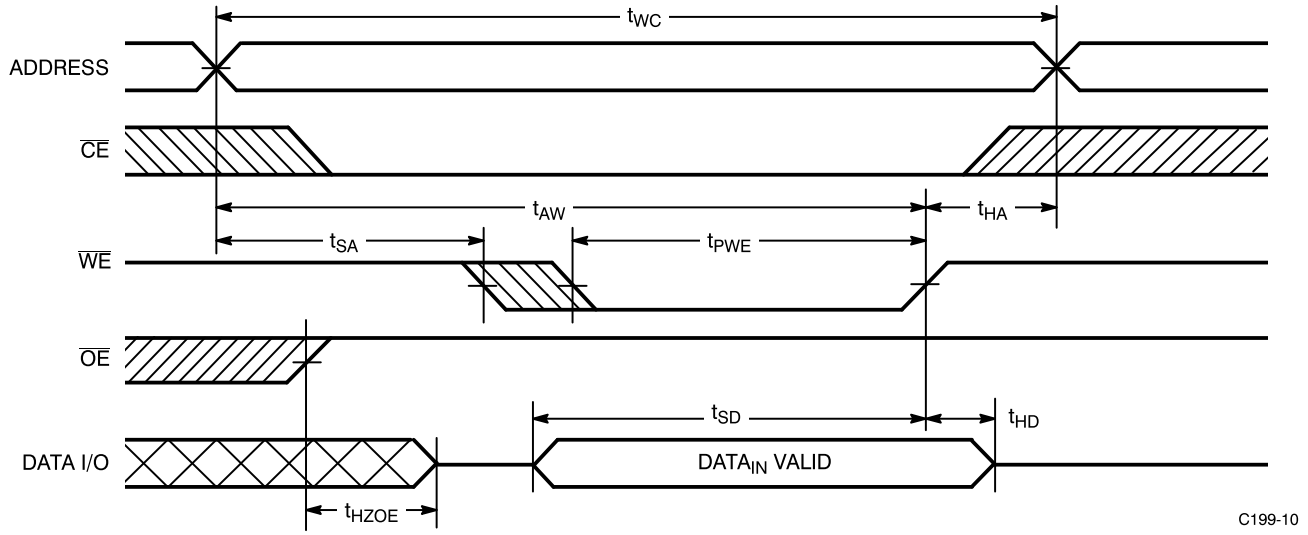
Notes:
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

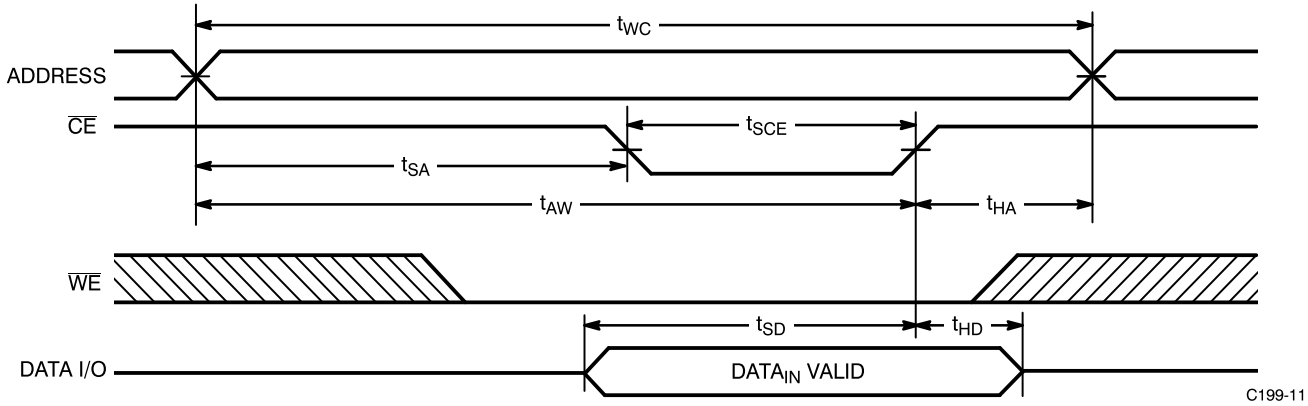
Read Cycle No. 2[14, 15]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[11, 16, 17]



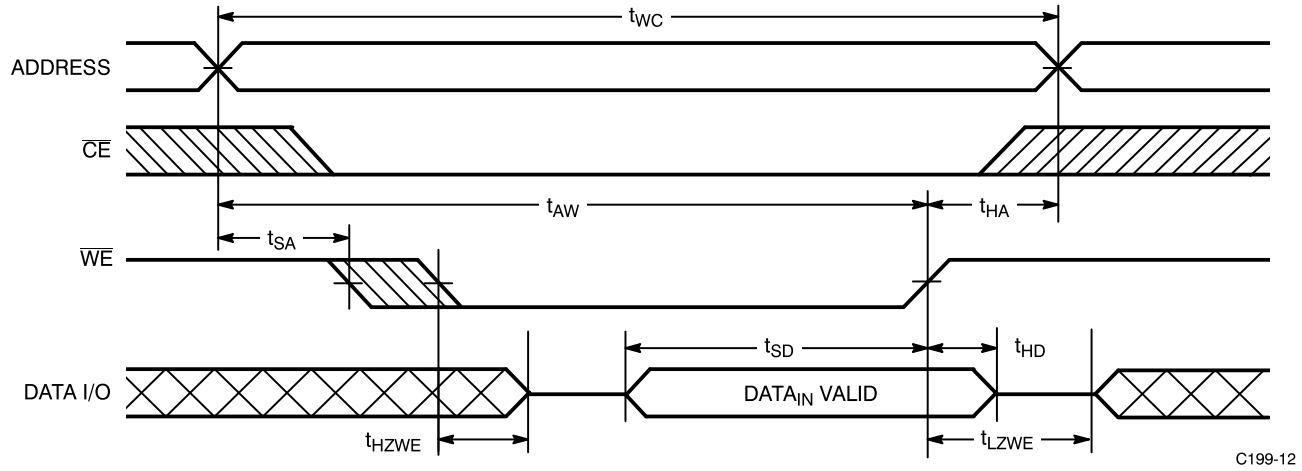
Write Cycle No. 2 ($\overline{CE}$ Controlled)[11, 16, 17]



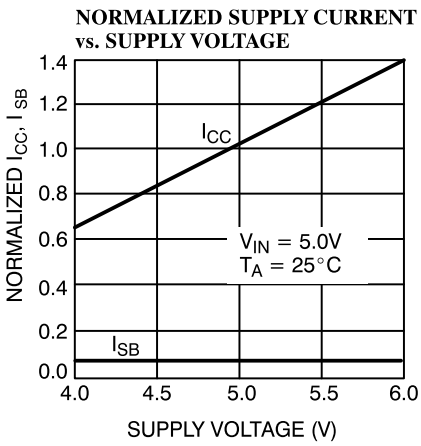
Notes:
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

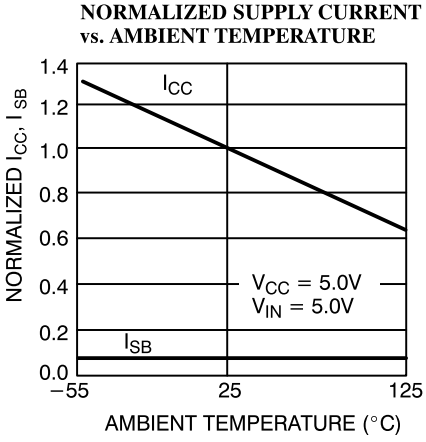
Switching Waveforms (continued)

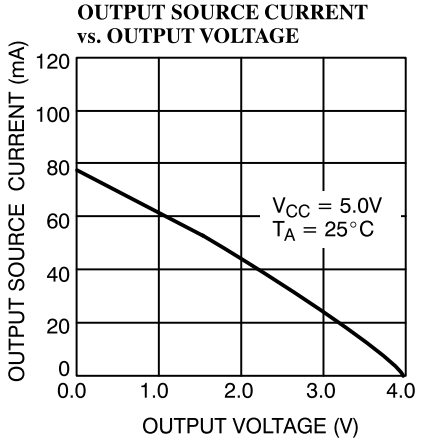
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[12, 17]

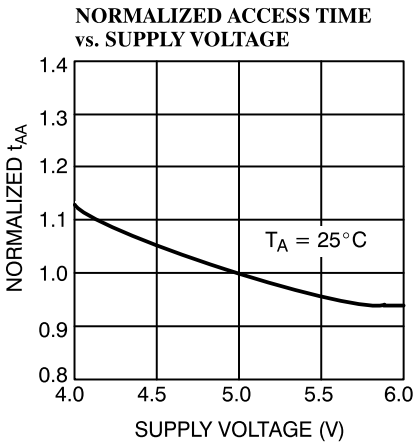


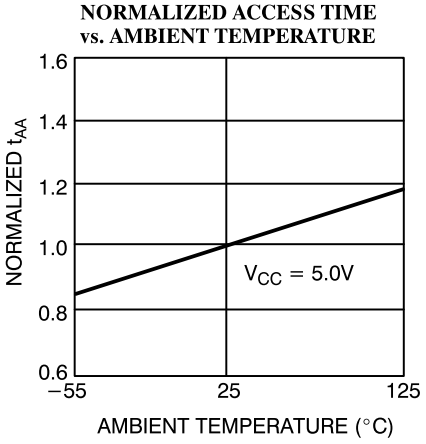
Typical DC and AC Characteristics

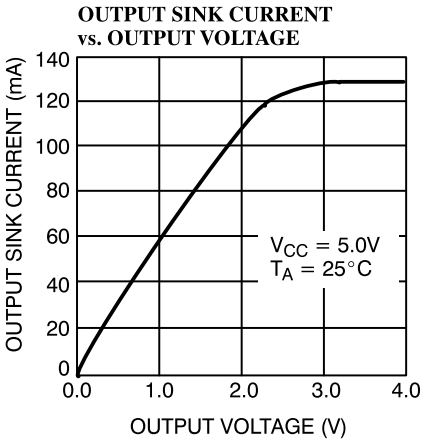






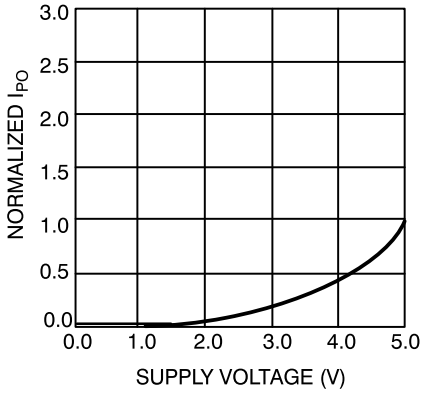




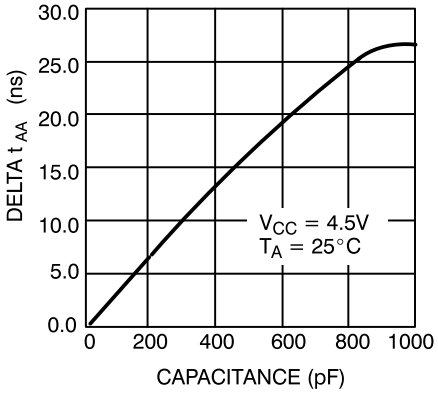


Typical DC and AC Characteristics (continued)

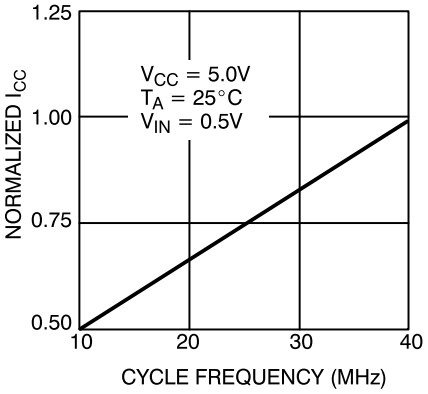
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C199−10VC	V21	28-Lead Molded SOJ	Commercial
12	CY7C199−12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L−12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199−12VC	V21	28-Lead Molded SOJ	
	CY7C199L−12VC	V21	28-Lead Molded SOJ	
	CY7C199−12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L−12ZC	Z28	28-Lead Thin Small Outline Package	
15	CY7C199−15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L−15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199−15VC	V21	28-Lead Molded SOJ	
	CY7C199L−15VC	V21	28-Lead Molded SOJ	
	CY7C199−15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L−15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199−15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L−15DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199−15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L−15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199−20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L−20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199−20VC	V21	28-Lead Molded SOJ	
	CY7C199L−20VC	V21	28-Lead Molded SOJ	
	CY7C199−20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L−20ZC	Z28	28-Lead Thin Small Outline Package	

Shaded area contains preliminary information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C199−20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L−20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199−20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L−20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199−25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199−25VC	V21	28-Lead Molded SOJ	
	CY7C199−25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199−25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199−25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199−35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199−35VC	V21	28-Lead Molded SOJ	
	CY7C199−35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199−35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199−35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199−45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199−45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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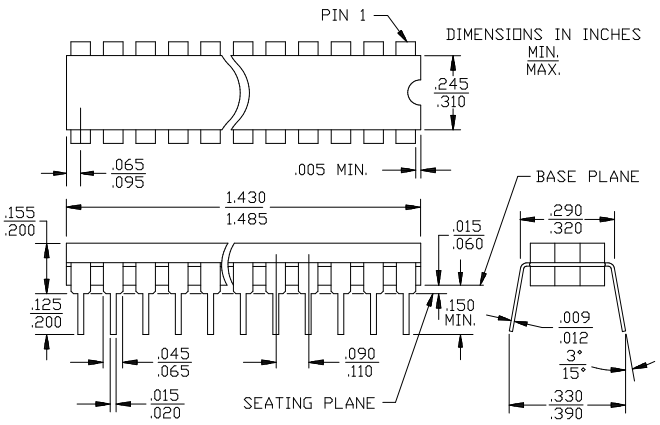
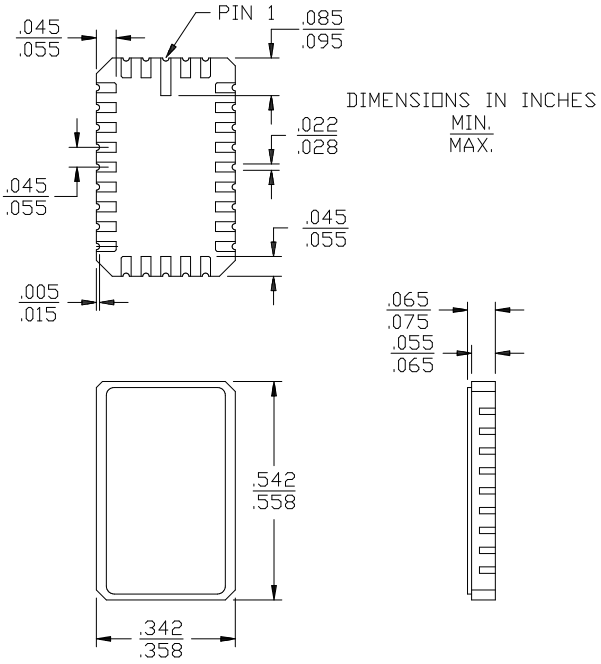
Package Diagrams

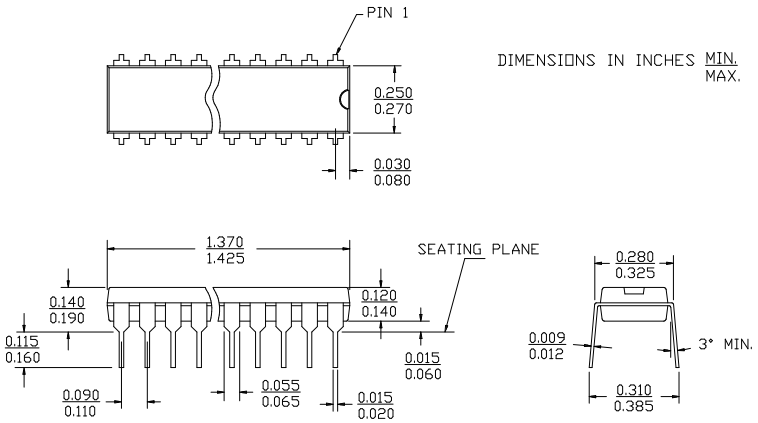
28-Lead (300-Mil) CerDIP D22
MIL−STD−1835 D−15 Config. A



28-Pin Rectangular Leadless Chip Carrier L54
MIL−STD−1835 C−11A

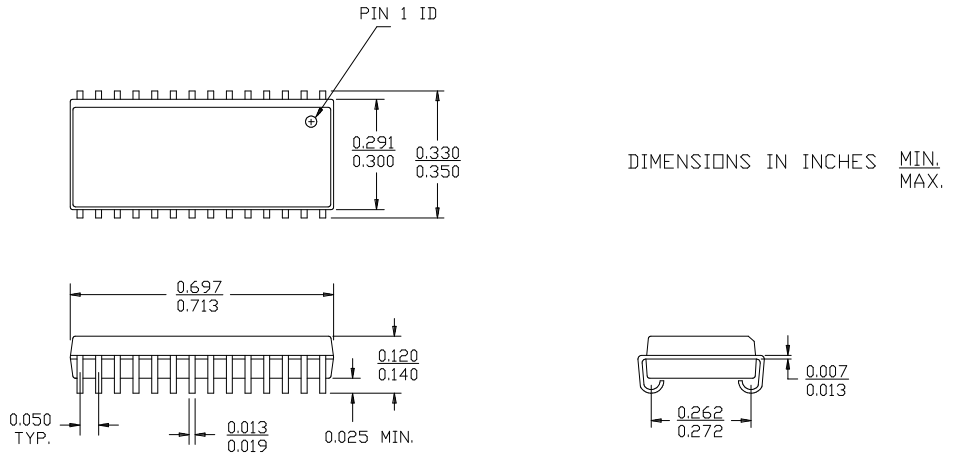


28-Lead (300-Mil) Molded DIP P21



Package Diagrams (continued)

28-Lead (300-Mil) Molded SOJ V21



28-Lead Thin Small Outline Package Z28