Using the CY7C964 with VIC

The CY7C964 is a flexible collection of byte-wide (8-bit) transceivers, latches, counters, multiplexers, and comparators that provide VMEbus interface designs with a low-cost alternative to PLDS, ASICs, or discrete logic devices. It is based on a standard cell design that incorporates patented line drivers for reduced ground bounce and high-noise immunity.

The CY7C964 is a companion part to the Cypress VIC068A and VIC64 VMEbus Interface Controller devices. It is compatible with all operating modes of either device, including dual address path, block transfers, block transfer initialization cycles, local DMA control, and D64 64-bit VMEbus block transfers (when used in conjunction with the VIC64). Signal naming conventions correspond directly to the VIC068A/VIC64 buffer control signals and the CY7C964 can be directly connected to these signals. The device can also be used as a generic interface building block. CY7C964s are cascadable allowing easy interfacing to any width bus. By combining multiple logic functions into one discrete part, the CY7C964 saves board space and reduces power consumption.

The CY7C964 has two main operating modes, byte width and word width. The byte-width configuration of the device has 8 local address, 8 local data, 8 VMEbus address, and 8 VMEbus data signals. In the byte-width modes, two methods are available for loading the VMEbus master block transfer address counters. This counter is loaded using the nominal VIC block transfer initiation cycle, or alternatively from the local data bus. Loading the VMEbus master block transfer counter from the local data bus decouples the board's local address map from that of the VMEbus. This allows boards that consume a great deal of local address space to still be able to view the entire VMEbus address region. More information on both of the VMEbus master block transfer address counter initialization techniques is provided in the following sections.

In word-width mode the local and VMEbus data signals change to 16-bit address or data paths. This mode expands all of the features of the device to 16 bits in width, with the exception of the D64 multiplexer. This multiplexer is disabled in word-width mode. Since protocols such as block transfer initiation cycles remain compatible in word-width mode, the device becomes useful as a 16-bit bus interface block for non-VMEbus applications.

CY7C964 Features

- Directly connects to VIC068A or VIC64
- Internal counters for block transfers
- Internal multiplexers for D64 block transfers
- Internal comparators for address decoding
- Supports VIC068A/VIC64 dual address path option
- Supports cascadable operation
- Directly drives VMEbus address and data
- Directly drives local address and data bus signals
- Reduces components for compact board design
- Low power requirements
- Available in 64-pin QFP

CY7C964 Block Diagrams

The CY7C964 is an array of optimally controlled counters, comparators, general registers, and multiplexers. A small amount of state logic is also present within the device. This state logic monitors bus cycles that are issued to the device and places the component in the appropriate mode. The state logic is implemented as an asynchronous rather than a synchronous sequential state machine. These hidden internal-state or configuration bits are set and cleared automatically by monitoring the arrival times of various input signals.

The configuration bits, and other input signals to the device, select the operating mode (byte width or word width), as well as the initialization method for the internal VMEbus master and local block transfer counters. The block diagrams in *Figures 1*, *2*, and *3*, show an equivalent internal representation of the device for each operational mode.

Byte-Width Mode I

In this mode, the CY7C964 operates as a conventional byte-width slice of VIC compatible interface logic. The device conforms to the standard VIC block transfer initiation cycle and includes multiplexers for D64 block transfer operations and comparison logic for VMEbus address decoding.

Counters C1, C2, and C3, latch L8, and multiplexers S3 and S5 form the core of the block transfer address generation logic. C1 is the local master block transfer address counter, C2 is the VMEbus slave block transfer address counter, and C3 is the VMEbus

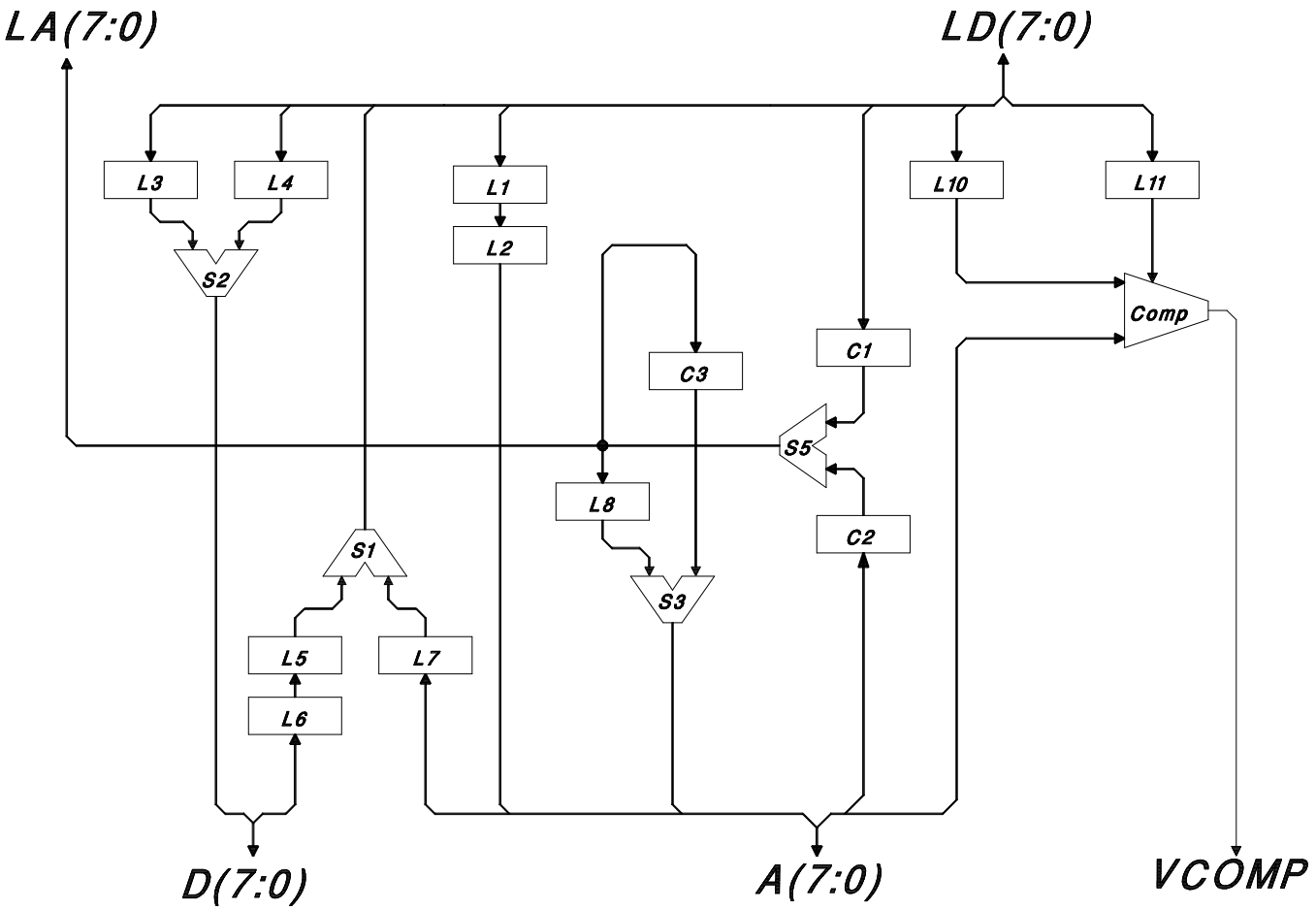

Figure 1. CY7C964 Byte-Width Mode I Block Diagram

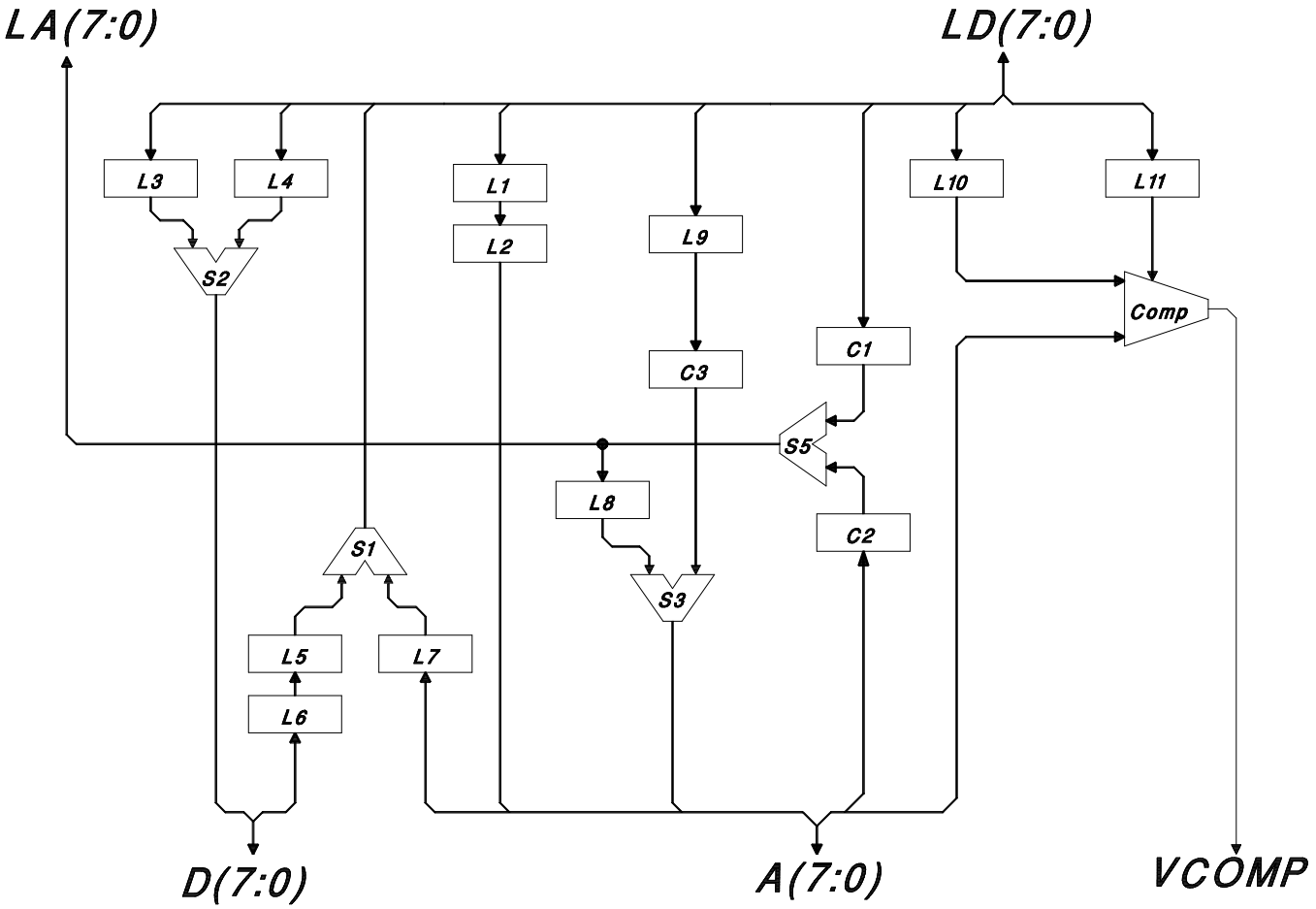

Figure 2. CY7C964 Byte-Width Mode II Block Diagram

master block transfer address counter. As shown in the block diagram, counter C1 loads from the local data bus LD[7:0], C3 loads from the local address bus LA[7:0], and counter C2 loads from the VMEbus address bus A[7:0]. Multiplexer S5 selects the source for the local address either through C2 (which is also used for single cycle operations) or C1. Latch L8 and multiplexer S3 provide the support for the Dual Address Path feature. Single cycle VMEbus master transfers can occur using L8 during the interleave periods of master block transfers without corrupting the contents of C3.

Latches L10, L11, and comparator COMP form the VMEbus address comparison logic. L11 is the Address Mask register that enables and disables bits of the address comparator. L10 is the Address Comparison register which contains an 8-bit value that is matched against A[7:0]. When the enabled bits of L10 match the corresponding signals of A[7:0], the VCOMP* output is asserted (Low). Writing 1's to all bits of L11 disables the comparison logic. In this case all values of A[7:0] match, causing the VCOMP output to be asserted continuously. Loading comparison register L10 clears and enables all bits of the mask register L11. Therefore, during system initialization, comparison register L10 must be loaded first, then bits can be disabled within mask register L11.

Latches L1, L2, L3, and L4, and multiplexer S2 combine to form a high performance D64 block transfer data pipeline and multiplexer. During D64 block transfer operations data is fetched from local memory and transferred to latch L1. A second memory fetch is required to assemble the 64-bit word. This data is stored in L3. When L3 is updated, the data in L1 is moved to L2. This allows the VIC

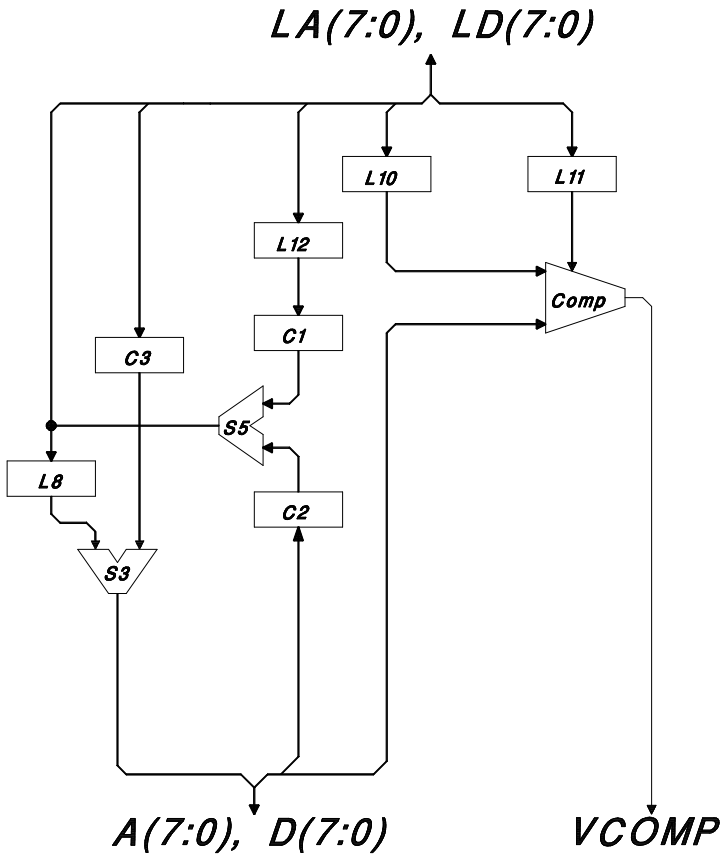

Figure 3. CY7C964 Word Width Mode Block Diagram

to prefetch the next word of information from local memory while the VMEbus D64 data transfer operation is in progress.

Latches L5, L6, L7 and multiplexer S1 form the VMEbus D64 block transfer data demultiplexer. Data is latched from the VMEbus into latches L6 and L7, simultaneously. The data is then moved to the local data bus through multiplexer S1.

This is the nominal operating mode of the CY7C964. Control signals connect to the corresponding buffer control signal on the VIC, with the exception of the DENIN* and DENIN1* inputs. Refer to the following section, Interfacing to the VIC64 and VIC068A, and to the *VIC64/CY7C964 Design Notes* for additional information on DENIN*, DENIN1*, and other control signals.

Byte Width Mode II

This mode is nearly identical to the previous byte-width mode with one exception. The VMEbus master block transfer counter, C3, loads from the local data bus LD[7:0] rather than the local address bus LA[7:0]. The main benefit of this operating mode is that the entire VMEbus address space is available for data transfers. Loading C3 from the local address bus may preclude some addresses from the VMEbus, because they are being decoded locally. For example if EPROM is located at address 0x00000000, this address may not be accessible across the VMEbus. Using the CY7C964 in this mode requires performing one additional bus cycle during the block transfer initiation.

The CY7C964 operates in byte-width mode if the BLT* and MWB* input signals on the CY7C964 are swapped. In other words, the MWB* signal on the

VIC connects to the BLT* input on the associated CY7C964s. The same rule applies for the BLT* output on the VIC. It connects to the MWB* input on the CY7C964s. The CY7C964 monitors the arrival time of these two signals and expects to load the master block transfer counter from the local data bus LD(7:0) if BLT* is asserted prior to MWB*. Swapping these two signals does not change the operation of any other feature on the device, however, there are two things to consider when using this mode.

The address decode signal that drives MWB* on the CY7C964 connects to the BLT* output on the VIC. This signal should be driven with an open collector or three-state device to allow the VIC to control the signal during block transfer operations.

Block transfer initiation cycles also change. The VMEbus master block transfer address counter loads from the local data bus one cycle before the actual block transfer initiation cycle. The subsequent cycle is a typical block transfer initiation cycle with the local data bus containing the local DMA address. The local address bus is ignored by the CY7C964s during this cycle, but not by the VIC. The low-order byte of the local address bus LA[7:0] must contain the correct VMEbus master block transfer address. This is necessary because the VIC cannot be programmed to load the VMEbus master block transfer address from the local data bus. For more information on Byte Width Mode II refer to the *VIC64/CY7C964 Design Notes*.

Word-Width Mode

The second main operating mode of the CY7C964 is the word-width mode. This mode of the device works well for VMEbus address control functions. All of the address related functions (local master block transfer counter, C1, VMEbus slave block transfer counter, C2, VMEbus master block transfer counter C3, and the address comparison logic) expand to 16 bits. The address and data buses on the part combine to form two 16-bit buses. A high-drive-strength, 16-bit bus and a medium-drive-strength bus are formed from A[7:0], D[7:0] and LA[7:0], LD[7:0] respectively. D[7:0] and LD[7:0] are the least significant sections of each of these buses.

In this mode one additional latch (L12), is located between the local address bus and local master block transfer counter, C1. This latch allows the local master block transfer counter to be loaded from the local address bus prior to loading the VMEbus master block transfer counter, C3. This is necessary since both the VMEbus master block transfer counter, C3, and the local master block transfer counter, C1, are loaded from the same local address bus. When counter C3 loads during the block transfer initiation cycle, the contents of latch L12 are moved to counter, C1.

All other functions available in this mode operate in a similar manner as in the byte width mode. For further information on this mode and detailed timing information refer to the *VIC64/CY7C964 Design Notes*.

Interfacing to the VIC64 and VIC068A

Previously, interfacing the VIC068A to the VMEbus required a significant amount of LSI and MSI devices. With the advent of 64-bit VMEbus block transfers and the VIC64, the external discrete device count for a full functional interface implementation expanded. The CY7C964 has been developed to combat this problem by incorporating the functions of much of this external logic into a single package. Use of the CY7C964 shortens system design, debug, and manufacturing cycle times. This removes the burden of performing worst-case and critical timing analysis on the VMEbus and VIC buffer control sections of a system design. Local control signals other than those directly connected to the VIC64 or VIC068A have been kept to a minimum. *Figure 4* shows a full function D64 VMEbus interface implemented using the CY7C964, VIC64 and all VMEbus interface local support logic. This example interface features:

- Dual Path Address Operation
- Slave BLT Cycles During Master BLT Interleave
- Software Programmable Slave VMEbus Address
- Write Posting
- VIC Mail Box Interrupt Messaging Support

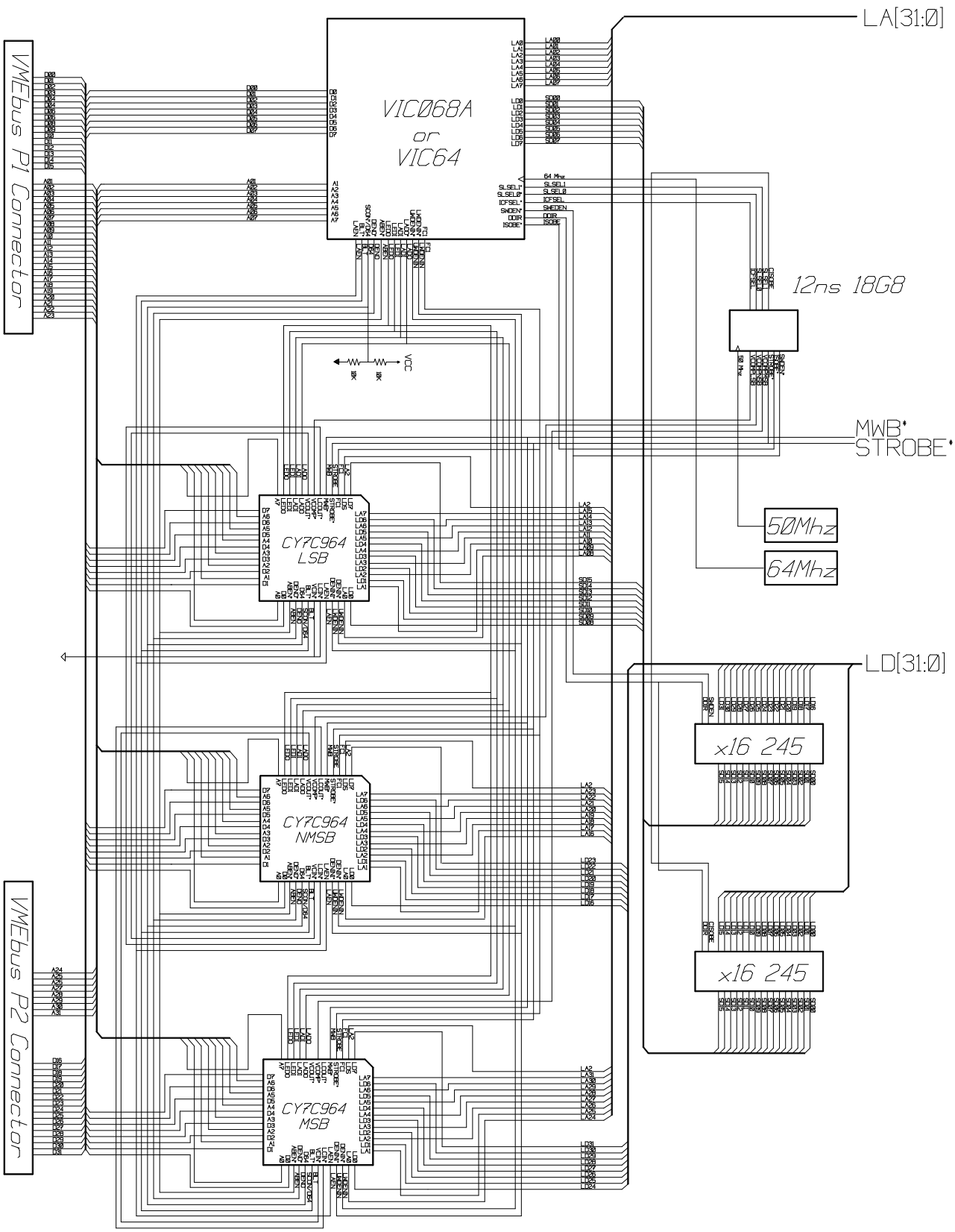

Figure 4. CY7C964/VIC VMEbus Interface

The interface can be dissected into 5 functional sections for the purpose of discussion. These sections are:

- VMEbus Signal Group
- VIC Buffer Control Signal Group
- CY7C964 Local Signal Group
- CY7C964 Address Comparison Group
- Local Data Swap Buffer Logic

The focus of this application note is the CY7C964. Each of the interface functional sections are examined from this perspective. The CY7C964s are referred to as the LSB (Least Significant Byte), NMSB (Next Most Significant Byte), and MSB (Most Significant Byte) device depending on the segment of the VMEbus that they control. The LSB controls VMEbus address and data signals [15:8], NMSB [23:16], and MSB [31:24]. This interface uses the CY7C964s in the byte width mode I as address and data controllers. All of the information contained within this section pertains to this mode of operation. For additional information on the signals described within this section consult The *VMEbus Specification (IEEE 1014)* and/or the *Cypress Semiconductor VIC068A/VAC068A User's Guide*

VMEbus Signal Group

This group includes the VMEbus address and data signals.

D[7:0]. VMEbus compatible data signals that directly connect to VMEbus P1 and P2 connectors.

A[7:0]. VMEbus compatible address signals that directly connect to VMEbus P1 and P2 connectors.

Each CY7C964 provides support for 8 bits of VMEbus address and data. Three CY7C964s are necessary for 32-bit (D32/D64) interface applications. The A[7:0] and D[7:0] transceivers on the CY7C964 furnish a high drive strength allowing direct connection to the respective address and data signals on the VMEbus backplane. With the VIC068A or VIC64 controlling the CY7C964s, all VMEbus worst case timing and drive strength requirements are met for all types of data transfer operations.

VIC Buffer Control Signal Group

This group includes all of the VIC buffer control signals.

LADO. Latch Address Out, directly connects to VIC LADO on all CY7C964s.

LADI. Latch Address In, directly connects to VIC LADI on all CY7C964s.

LEDO. Latch Enable Data Out, directly connects to VIC LEDO on all CY7C964s.

LEDI. Latch Enable Data In, directly connects to VIC LEDI on all CY7C964s.

ABEN*. VMEbus Address Bus Enable, directly connects to VIC ABEN on all CY7C964s.

DENO. Data Enable Output, directly connects to VIC DENO on all CY7C964s.

D64. D64 Block Transfer Mode Enable, directly connects to VIC64 SCON/D64 pin on all CY7C964s. This input should be tied Low on all CY7C964s when using VIC068A.

BLT*. Block Transfer Enable, directly connects to VIC BLT on all CY7C964s.

LAEN. Local Address Enable, directly connects to VIC LAEN on all CY7C964s.

DENIN*. Primary Data Enable In, directly connects to VIC UWDENIN* on NMSB and MSB CY7C964s, and directly connects to VIC LWDENIN* on LSB CY7C964.

DENIN1*. Companion Data Enable In, directly connects to VIC LWDENIN* on NMSB and MSB CY7C964s, and directly connects to VIC UWDENIN* on LSB CY7C964.

A major design-time savings is realized when using the CY7C964s because all of these signals directly connect to the VIC or are hardwired to a steady state value. The buffer control interface is simple and straight forward, with the minor exception that the connection of UWDENIN* and LWDENIN* control signals from the VIC are swapped to the DENIN* and DENIN1* on the LSB CY7C964.

CY7C964 Local Signal Group

The CY7C964 local signal group consists of the VMEbus and local block transfer counter count-enable daisy-chains.

LCIN*. Local address counter Count enable IN. On the LSB CY7C964 tie this input Low. On the NMSB device directly connect this signal to the LCOUT* of LSB device. For the MSB CY7C964 connect this input to the LCOUT* of the NMSB device.

LCOUT*. Local address counter Count enable OUT. On the LSB CY7C964, connect this output to the NMSB LCIN* input. On the NMSB CY7C964, connect this output to the MSB LCIN* input. For the MSB device do not connect this output.

VCIN*. VMEbus address counter Count enable IN. On the LSB CY7C964 tie this input Low. On the NMSB device directly connect this input to the VCOUT* of LSB device. For the MSB CY7C964 connect this input to the VCOUT* of the NMSB device.

VCOUT*. VMEbus address counter Count enable OUT. On the LSB CY7C964, connect this output to the NMSB VCIN* input. On the NMSB CY7C964, connect this output to the MSB VCIN* input. For the MSB device, do not connect this output.

These signals enable the local and VMEbus higher order address counters, two local address counters, a master block transfer, a slave block transfer, and a single VMEbus address counter. The local address counters share the LCIN*/LCOUT* count enable daisy-chain. These signals are multiplexed within the CY7C964 and enable the proper counter depending on the current state of the interface. The VCIN*/VCOUT* daisy-chain is dedicated to the VMEbus address counter on the device. When the VCIN* or LCIN* inputs are held Low, counting is enabled for the appropriate counters within the device. The VCIN* and LCIN* signals do not advance the counters; these signals just enable counting. The counters increment when these signals are active and the proper increment count control logic sequence occurs. The VIC advances the address counters at the proper time during VMEbus and local DMA block transfer operations.

CY7C964 Address Comparison Signal Group

The CY7C964 address comparison signal groups consists of the local signals that are associated with the internal VMEbus address comparators. FC1, MWB*, and LDS also are used to control other functions on the CY7C964. Refer to the *VIC64/CY7C964 Design Notes* for more information on these signals.

FC1. Function Code 1 signal, directly connects on all CY7C964s to the local signal that drives the VIC FC1.

MWB*. Module Wants VMEbus, directly connects on all CY7C964s to the local signal that drives the VIC MWB*.

LDS. Load Register Select, directly connects to LA2 for systems with 32-bit local bus. Refer to the following text for additional information.

STROBE*. Latch Register Control. A chip select like signal that selects the CY7C964 internal comparator mask and comparison registers.

VCOMP*. VMEbus Address Comparator Output. The comparator output signal from the CY7C964 address comparator. This signal asserts Low if the a pattern on address signals A[7:0] matches the programmed values of the comparison logic.

The implementation of this group of CY7C964 signals is application specific. The MWB* and FC1 signals are included in this section because they are locally generated signals required by the VIC. These two signals differ slightly from their companions on the VIC. On the CY7C964 the MWB* and FC1 signals are inputs. On the VIC, MWB* is also an input, but FC1 is a bidirectional signal that can be driven by the VIC. These signals on the CY7C964 can be directly connected to their respective local signals on VIC.

The CY7C964s contain a high-performance programmable VMEbus address equality comparator. This comparator is controlled by two internal write-only registers: a mask and a compare register. The mask register enables and disables bits of the

comparator and the compare register stores the data pattern which inputs are compared against. VCOMP* is the active Low comparator match output signal. VCOMP* is driven Low by the CY7C964 if the bit pattern on A[7:0] matches the associated enabled bits of the compare register. Loading the mask register bits with 0's enables the corresponding bits of the compare register. Loading bits of the mask register with 1s places bits of the compare register in a don't care or match-on-anything state. If all bits of the mask register are loaded with 1s, the compare register matches everything, causing VCOMP* to always be driven Low. These registers are loaded by supplying the proper data on LD(7:0) and address on MWB* and LDS signals. The STROBE* input is used to qualify the address and latch the data into the proper internal register. *Figures 5*and *6* and *Table 1* show the waveforms and timing conditions needed to load the compare and mask registers. The mask register is cleared (all bits enabled), when the compare register is loaded.

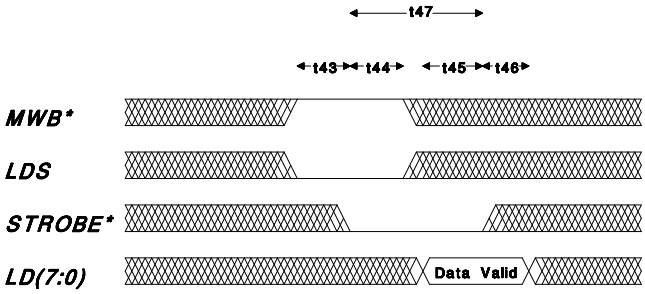

Figure 5. Mask Register Load Cycle

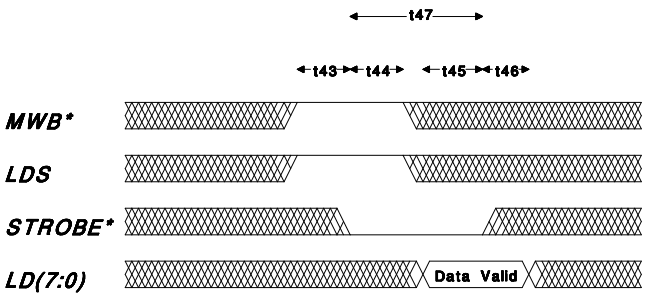

Figure 6. Compare Register Load Cycle

Table 1. Compare Register Load Cycle Times

Para	Description	Min.	Max.	Unit
t43	MWB*, LDS set-up time to STROBE* falling edge	0		ns
t44	MWB*, LDS hold time after STROBE* falling edge	5		ns
t45	LD(7:0) set-up time to STROBE* rising edge	5		ns
t46	LD(7:0) hold time after STROBE* rising edge	5		ns
t47	STROBE* minimum pulse width	10		ns

Therefore it is important to load the compare register first, then load the mask register as desired.

This load cycle operates as follows. The state of LDS and MWB* are latched on the falling edge of STROBE*. The data is loaded into the selected register on the rising edge of STROBE*. MWB* must be held inactive (High) during comparator register loading. The state of LDS selects the register to load. If LDS is High during the cycle the compare register is loaded; if LDS is Low the data is written to the mask register. This load cycle can be generated by decoding a separate address region or chip select signal for the CY7C964 comparator registers.

For applications with a 32-bit local data bus it is desirable to load all three CY7C964s in parallel by having the host processor perform a 32-bit write cycle to the address region that activates STROBE*. The select signal for the address region is connected to the STROBE* input on all three CY7C964s. The 8 bits of data on the lowest order section of the local data bus LD[7:0] do not matter to the VIC, as long as the VIC CS* signal remains inactive during this write cycle. Boards that use this style of interface should connect LDS to LA2, thereby decoding the mask register at the Base Address of the address region and the compare register at the Base Address + 4. LDS also controls the operation of the D64 block transfer data multiplexer/demultiplexer. Systems with 32-bit local

data buses should connect local address signal LA2 to LDS for proper operation of the D64 data multiplexer/demultiplexer logic.

The mask and compare registers can be set to select any contiguous address region on the VMEbus. These registers do not preload and can power up in any state. It is advisable to initialize these registers as soon as possible in the system boot sequence. The CY7C964 comparator output signal VCOMP*, supplies the result from the equality compare logic. VCOMP* drives Low when the input matches the loaded comparator conditions.

The CY7C964 VCOMP* signal is not directly compatible with the VIC SLSEL0* and SLSEL1* slave select signals. The short (10 ns) address setup time to AS* active for VMEbus slave boards does not meet the worst case compare out delay of the CY7C964 VCOMP* signal. Combining this with the potential output glitching that can occur with an asynchronous comparator can cause problems for the VIC. It is recommended that the VCOMP* signal be externally filtered prior to being used with the VIC SLSEL0* or SLSEL1* signals. Most applications will require some external comparison logic to combine the VCOMP* signals from the NMSB and MSB devices, furnishing finer grained VMEbus decoding.

The interface example in *Figure 4* uses a 12-ns 18G8 to perform these functions and to disable the VMEbus slave select signals to the VIC until the CY7C964 comparator control registers have been initialized. Using this PLD allows the interface to decode three different VMEbus addresses regions:

- VMEbus A32 for local access – VIC SLSEL0*
- VMEbus A24 for local access – VIC SLSEL1*
- VMEbus A16 for mailbox interrupt – VIC ICFSEL*

Figure 7 shows the PLD ToolKit design file for this device. The two VIC slave select signals (SLSEL0* and SLSEL1*) can be used to conveniently decode two VMEbus address regions. SLSEL0* selects if the NMSB CY7C964 becomes TRUE. SLSEL1* requires both NMSB and MSB comparators to evaluate TRUE.

A 50-MHz clock and the D registers within the 18G8 are used to build a simple digital filter that removes any glitches that may occur on the three CY7C964 VCOMP* signals.

As mentioned previously, the comparators within the CY7C964s are always active and they power up in an unknown state. The PLD includes an ENABLE signal which disables the SLSEL0*, SLSEL1*, and ICFSEL* signals to the VIC until the first access is made to one of the comparator control registers. Adding the ENABLE function to this PLD guarantees that the VIC slave select signals cannot become active until the one of the comparator control registers has been initialized.

There is a potential problem that can occur when loading the CY7C964 comparator control registers. The local data bus isolation buffer, which is necessary to allow data swapping, is normally disabled by the VIC. This causes a problem during CY7C964 register initialization cycles because the VIC only enables the local data bus isolation buffers during VIC or VMEbus accesses. The PLD solves this problem by providing conditioning logic for the ISOBE* signal. In the PLD design file in *Figure 7,* a signal named CISOBE* is generated. CISOBE* asserts (Low) enabling the isolation buffer if the VIC ISOBE* is asserted or the CY7C964 STROBE* input is asserted. SWDEN* was added to the equation for completeness, however, it may not be necessary in many designs. There are obviously many other implementations for control of the VIC isolation buffers. One implementation is shown here, but the best method for control of this signal is application specific and left to the designer.

Local Data Swap Buffer Logic

Local Data Swap Buffer logic is a requirement for all 32-bit local bus designs that want to be able to perform 8- or 16-bit transfers. The swap buffer moves data to and from the lower section of the VMEbus D[15:0] to the upper segments of the local bus D[31:16]. VMEbus requires that all 8- and 16-bit data transfers be performed on the D[15:0] section of the bus. The CY7C964s work properly with the VIC controlled swap buffer.

```
C18G8;

CONFIGURE;

CLK_50Mhz(node=1),
LSBCOMP(node=2),
NSBCOMP(node=3),
MSBCOMP(node=4),
STROBE(node=5),
BD_RESET(node=6),
ISOBE(node=7),
SWDEN(node=8),

ENABLE(node=12, noreg, iop),
SEL(node=13),
DSEL(node=14),
CISOBE(node=15, noreg, iop),
SLSEL1(node=17, noreg, iop),
SLSEL0(node=18, noreg, iop),
ICFSEL(node=19, noreg, iop),

EQUATIONS;

/CISOBE    =   <OE>
               <SUM> /ISOBE
               +     /STROBE *  SWDEN;

/ENABLE    =   <OE>
               <SUM>  BD_RESET * /STROBE
               +      BD_RESET * /ENABLE;

/SEL       =   <OE>
               <SUM>  /LSBCOMP * /ENABLE *  BD_RESET
               +      /NSBCOMP * /ENABLE *  BD_RESET
               +      /MSBCOMP * /ENABLE *  BD_RESET;

/DSEL      =   <OE>
               <SUM>  /SEL * /LSBCOMP * /ENABLE *  BD_RESET
               +      /SEL * /NSBCOMP * /ENABLE *  BD_RESET
               +      /SEL * /MSBCOMP * /ENABLE *  BD_RESET;

/ICFSEL    =   <OE>
               <SUM>  /DSEL * /LSBCOMP * /ENABLE * BD_RESET;

/SLSEL0    =   <OE>
               <SUM>  /DSEL * /NSBCOMP * /ENABLE * BD_RESET;

/SLSEL1    =   <OE>
               <SUM>  /DSEL * /MSBCOMP * /NSBCOMP * /ENABLE *  BD_RESET;
```

Figure 7. PLD ToolKit™ Design File For 18G8 PLD

Summary

The CY7C964 is a high-performance byte or word width slice of VIC compatible VMEbus logic. Using the CY7C964 in conjunction with the VIC068A or VIC64 shortens design cycle time, reduces component count, reduces interface real estate requirements, and overall design risk. For further information on the local VIC interface and more detailed timing information in the CY7C964 refer to the *VIC068A/VAC068A User's Guide* and the *VIC64/CY7C964 Design Notes.*