ADVANCED INFORMATION

CYM9651/2/3
CYM9654/5

Raceway Interlink Modules

Features

- **High-Performance module family**
- **Converts existing VMEbus chassis into Raceway fabric**
- **160 MByte/second per port data transfers**
- **Uses P2 connections**
- **CYM9652 provides a 4-slot Raceway fabric**
- **CYM9653 provides an 8-slot Raceway fabric**
- **CYM9654 provides a 12-slot Raceway fabric**
- **CYM9655 provides a 16-slot Raceway fabric**
- **CYM9651 provides a single-slot connection for expansion purposes**

Introduction

Cypress's Raceway Interlink Modules bring embedded supercomputing performance to real-time VME-based systems. As a backward-compatible upgrade, Raceway Interlink transforms the topology of an existing VMEbus chassis from a single transaction bus to a scalable real-time fabric capable of over 1 Gbyte/sec of aggregate bandwidth.

Interlink modules add interboard bandwidth to VME-based systems by providing multiple, concurrent, high-speed communication paths between VME boards interfaced to the Raceway Interlink standard. In addition to increased bandwidth, Raceway Interlink offers low latency and priority control, essential to real-time applications.

The Raceway Interlink standard is published and maintained by VITA (VMEbus and Futurebus International Trade Association). The VITA standards organization (VSO) has ratified the Raceway Interlink Specification which defines the data link protocol and the physical interface definition for the high performance extension to the VMEbus standard.

Mechanically, the Raceway Interlink Modules mount on the backplane of a VME chassis similar to industry-standard VSB backplane modules. Electrically, these modules are connected to the VME slots through the P2 chassis backplane connector.

Raceway Interlink Modules implement the Raceway interconnect fabric, using the Cypress CY7C965 Raceway Crossbar device and appropriate clock and interface circuitry.

The CY7C965 Raceway Crossbar is a six-port crossbar implemented in a single low-power device. The crossbar can perform three simultaneous transfers of 160 megabytes/sec for a total of 480 megabytes/sec and can broadcast to five ports at an aggregate of 800 megabytes/sec. Each of the Interlink Modules uses the CY7C965 to implement a fat tree topology for interconnecting a different number of VMEbus slots. For more details see the CY7C965 data sheet.

In addition to scalable, high throughput and bandwidth, the Raceway Interconnect Fabric is also designed to meet low-latency real-time data transfer requirements. The Interlink Modules support priority interrupt and adaptive routing, features which optimize the already high performance capabilities of the modules.

It is simple to get data on and off the Raceway fabric, Cypress PLDs may be used to add the routing overhead to the data blocks. Application notes are available from your local sales office.

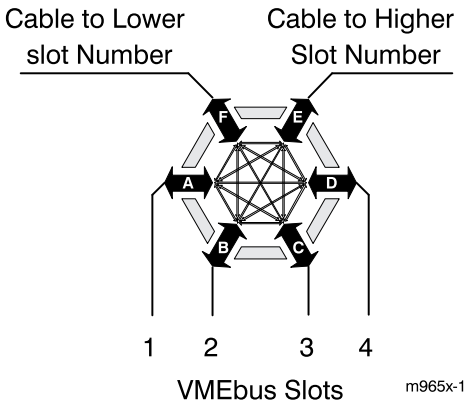

Figure 1. CYM9652 Architecture

CYM9652 Interlink Module

The CYM9652 is a single Raceway Interlink Module that spans four VME slots. The CYM9652 has two connectors for expansion to other interlink modules. *Figure 1* shows the architecture of the CYM9652.

CYM9653, CYM9654 and CYM9655 Modules

The CYM9653, CYM9654, and CYM9655 modules are designed for larger VMEbus-based multicomputer applications. These devices share a common crossbar network topology that provides a high interconnection bandwidth by exploiting parallel Raceway paths.

The parallel paths on the interlink module, used to support a given set of concurrent data transfers, may be automatically selected by the Raceway Crossbars. In this mode, if one path is already busy with a transfer, the free path is automatically selected by the crossbar logic. This is called "adaptive routing" and is described in detail in the next section.

It can be seen from *Figures 2*, *3*, and *4* that the architecture is expandable. Using ribbon cables, two or more modules may be joined together to create more-complex configurations.

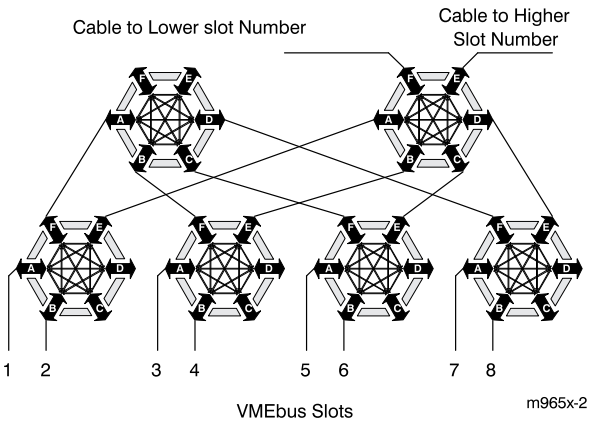

Figure 2. CYM9653 Architecture

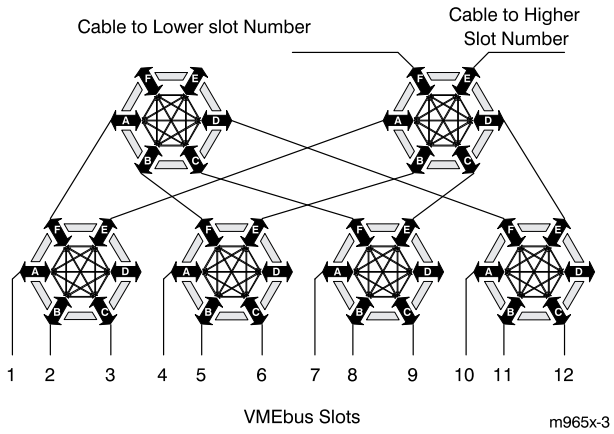

Figure 3. CYM9654 Architecture

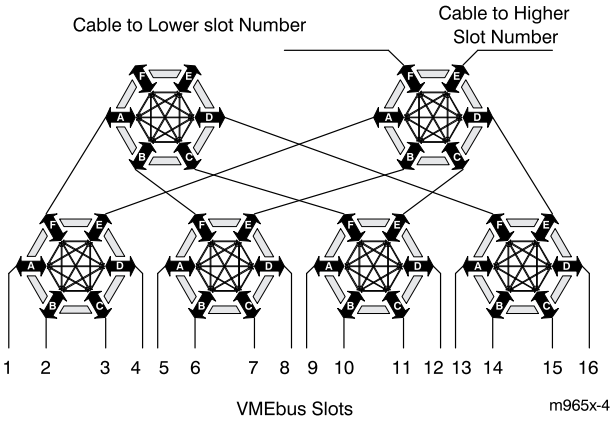

Figure 4. CYM9655 Architecture

Adaptive Routing

Adaptive Routing is the default data path option with the CYM9653, CYM9654, and CYM9655 devices. Adaptive Routing is a unique feature of the CY7C965 Raceway Crossbar. The fabric of interconnected crossbars automatically chooses a free path in the event that a requested path is blocked by a higher-priority transfer.

Adaptive Routing with the Interlink CYM9653, CYM9654, and CYM9655 modules is an feature that frees the programmer from the details of path routing. Distributed matrix transpose or "corner turn" applications, for example, achieve very high interprocessor communication bandwidth by utilizing this feature.

Path Priorities

High priority transfers can be programmed to preempt lower priority transfers, ensuring deterministic message transfer time regardless of lower priority internode traffic. This is a feature of the CY7C965 Raceway Crossbar's protocol: the initiating masters of data transfers embed a priority code into the header, which is latched into each participating crossbar. When a route is requested that includes a higher priority code, the crossbar itself sends a "kill" request to the lower priority master. Upon receiving this "kill" request, the master will cleanly relinquish control of the path, allowing the higher priority data transfer to take place. When the higher priority transfer has completed, the path will be available for the low priority connection to progress from the point at which it was interrupted.

CYM9651 Module

The CYM9651 is a single VME slot interlink module. It consists of a one-slot connector containing clocking circuitry and a 40-conductor ribbon cable. This module can be used to connect a Raceway VME board to either another interlink module, such as the CYM9652, CYM9653, CYM9654, or CYM9655, or to another single CYM9651 device.

The CYM9651 gives the system designer additional configuration flexibility in two ways. First, two CYM9651 devices can be connected with an ribbon cable to create a low-cost, low-end connection between two Raceway Interlink-compatible VME boards. Secondly, CYM9651 modules can be used to expand other interlink modules by one or two slots. The VME slots connected with CYM9651s may be adjacent VME slots or may separated by up to four VME slots. *Figure 5* illustrates two configurations using CYM9651 devices.

Performance of Interlink Modules

When quantifying the system performance of the Raceway Interlink Modules, three important parameters typically need to be evaluated: Raceway node-to-node effective transfer performance as a function of transfer size, total peak aggregate transfer rate, and transfer latency.

The peak aggregate performance of interlink modules is defined as the total available bandwidth of the interconnection system on the interlink module. This is the sum of the maximum number of simultaneous interboard transfers, and in general assumes the shortest paths for all transfers (no path longer than one crossbar). The peak bi-section performance gives a measure of the capability to transfer data across longer paths. It could be viewed as the bandwidth available for nodes at one end of the fabric trying to talk to nodes at the other end. The peak broadcast bandwidth is calculated assuming one node acting as the source, and all other nodes acting as the destination. The peak rates are shown in *Table 1*. They assume that the expansion connectors are unused.

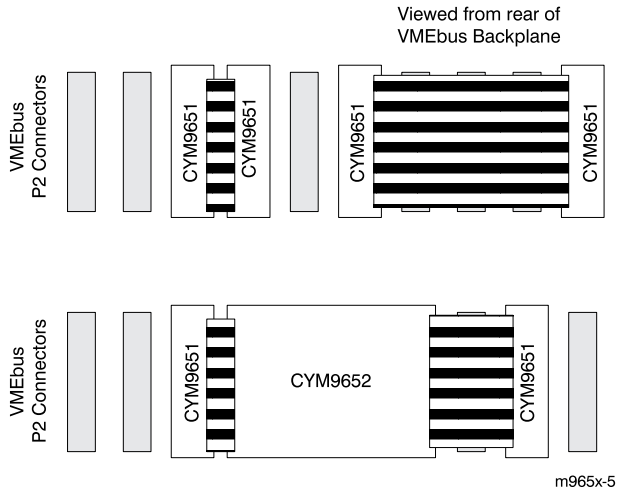

Figure 5. Use of CYM9651 Modules

Table 1. Performance Figures (MByte/second)

Module	Peak Aggregate Bandwidth	Peak Bi-Section Bandwidth	Peak Broadcast Bandwidth
CYM9652	320	320	480
CYM9653	640	640	1120
CYM9654	960	640	1760
CYM9655	1280	640	2400

Transfer Latency

Latency is critical in real-time embedded systems in which the processor is an element in a real-time control loop.

The Raceway Crossbar chips have extremely low latency. Each crossbar connection takes approximately 125 nanoseconds. From a system design standpoint, the latency to connect transfers, including preempting lower priority transfers, and remote memory access time, is approximately two microseconds for large systems. Once the Raceway path is established, data is transferred at memory rates. For sequential transfers, this is 160 Mbytes/sec. Because Raceway offers software selectable transfer priorities, deterministic response times within a few microseconds can be designed into applications that require minimal latencies.

Broadcast

The Interlink modules support broadcast. Broadcast is a feature of the Raceway Interconnect Fabric that can be used to increase the performance of applications that require multiple CPU boards to use the same data. Broadcast takes advantage of the Raceway Interconnect Fabric's ability to route data to multiple crossbar ports simultaneously, allowing data to be transmitted to many boards with a single transfer. Peak broadcast bandwidth is shown in *Table 1*.

Typical applications make use of the Raceway broadcast capability in one of two ways:

3. Sending the same data from an external interface to multiple processor boards.
4. Transmitting data that resides on a single board to a group of boards.

The source of the broadcast has the choice of sending the data to subsets of the node population: the Raceway protocol allows the use of a broadcast accept field which the responding slaves use to determine whether to capture the broadcast or not. For more details consult the CY7C965 Raceway Crossbar data sheet.

Physical Description

Raceway Interlink Modules attach to the unused P2 "wire wrap posts" (3 rows of 36 pins on the P2 connector approximately 1/2 inch in length) of a VME chassis. Industry-standard chassis can be ordered with these pins, also called VSB pins (electrically only rows A and C are used).

Raceway Interlink Modules are attached to the VME P2 connectors in the chassis by a two-level mechanical connection involving two printed circuit boards (PCBs) as shown in *Figure 6*. Two boards eliminate the need for high force connection to the P2 wire posts when mounting large interlink devices. All interlink modules thus consist of two or more boards. The first of these is a low-profile module, with high-insertion-force connectors spanning one or four VME slots. These plug onto the P2 connector wire posts on the backplane of the chassis. The low-profile module contains low-insertion-force connectors that mate with the component board. The component board, which primarily consists of crossbar ASICs and signal layers, is connected by a low-insertion-force attachment to the first board(s). The CYM9655, for example, has four high-insertion boards, each spanning four slots. A single, 16-slot PCB board with crossbars is attached to the four boards. The complete assembly is low profile and requires 1.8 inches of clearance from the chassis backplane. An additional 0.6 inches is required for natural convection of air for cooling.

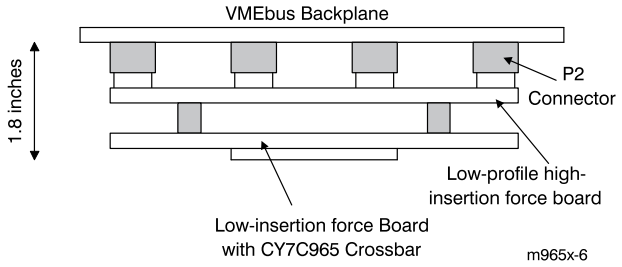

Figure 6. Mechanical Drawing of Modules

Interlink Configuration Rules

There are several rules for configuring systems with interlink modules.

Single Interlink Modules on Backplane

- Interlink modules require that the VME chassis contain standard "wire wrap" posts with shrouds on the P2 connector of the backplane.
- Appropriate clearance must be provided between the P2 wire post and the back panel of the chassis enclosure (see *Figure 6*).
- Not all VME/Raceway slots must be filled with boards (i.e., slots can be skipped).
- Boards inserted in VME/Raceway slots must have a valid Raceway interface or have rows A and C of the P2 connector unused.

Additional Rules Apply Only to Configurations with Multiple Interlinks

- Multiple interlink modules can be mounted on the backplane with or without expansion cables.
- A maximum of four slots may be skipped between interlinks when connecting two or more interlink modules together. (This rule ensures proper electrical characteristics under all allowable environmental conditions.)
- A maximum of four interlink modules may be used per chassis.
- A CYM9652, CYM9653, CYM9654, or CYM9655 module may be expanded to both the lower and higher numbered VME slots by CYM9651 or CYM9652 modules.
- Loop back connections are not allowed, i.e., connecting the two end connectors of an interlink together (or for a series of interlink modules, the end connectors cannot be looped back and connected together).
- Interlink expansion cables may not span separate VME backplanes, (i.e., connection of interlink cables across "split" VME backplanes or between chassis is not supported).

Connector Pin Assignments

Each interlink module has several connectors intended to mate with the P2 VMEbus Backplane connectors. The standard three-row P2 connector assignment is shown below in *Table 2*. The newer five-row connectors may be found in some backplanes. These may be compatible with the Interlink modules, though this is implementation-dependant. These have additional rows labelled Z and D: these rows are not used by the Interlink modules.

Table 2. Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
A1	XCLKI	B1	+5 Volts	C1	XRESETIO
A2	GND	B2	GND	C2	Reserved
A3	XBIO09	B3		C3	XSYNCI
A4	XBIO08	B4		C4	GND
A5	GND	B5		C5	XBIO07
A6	XBIO06	B6		C6	GND
A7	GND	B7		C7	XBIO11
A8	XBIO10	B8		C8	GND
A9	XBIO04	B9		C9	STROBEIO
A10	GND	B10		C10	REPLYIO
A11	XBIO05	B11		C11	GND
A12	XBIO03	B12	GND	C12	REQI
A13	GND	B13	+5 Volts	C13	REQO
A14	RDCONIO	B14		C14	GND
A15	Reserved	B15		C15	XBIO02
A16	GND	B16		C16	XBIO01
A17	XBIO00	B17		C17	GND
A18	XBIO15	B18		C18	XBIO12
A19	GND	B19		C19	XBIO25
A20	XBIO24	B20		C20	GND
A21	XBIO31	B21		C21	XBIO29
A22	GND	B22	GND	C22	XBIO30
A23	XBIO28	B23		C23	GND
A24	XBIO27	B24		C24	XBIO26
A25	GND	B25		C25	XBIO23
A26	XBIO22	B26		C26	GND
A27	XBIO20	B27		C27	XBIO19
A28	GND	B28		C28	XBIO21
A29	XBIO18	B29		C29	GND
A30	XBIO17	B30		C30	XBIO16
A31	GND	B31	GND	C31	XBIO14
A32	XBIO13	B32	+5 Volts	C32	GND

Specifications

Electrical/Mechanical

	CYM9651	CYM9652	CYM9653	CYM9654	CYM9655
Power (Watts)	0.5	1.75	10	13	13
Weight (oz.)	2	5	14	20	26
Dimensions (in.)	0.76 x 3.74	3.12 x 3.54	6.32 x 3.54	9.52 x 3.54	12.72 x 3.54

Module height from the VME backplane is 1.8 inches (see *Figure 6*).

Reliability

	Commercial* MTBF (hours)
CYM9651	2,740,000
CYM9652	600,000
CYM9653	549,000
CYM9654	380,000
CYM9655	330,700

(* @ 25C) Calculated using MIL−STD−217F

Operating Conditions

Parameter	Commercial Modules
Temperature Range (operating)	−20˚C to 50˚C
Temperature Range (non-operating)	−40˚C to 85˚C
Shock (Operating) (11 ms half sine Mil−810)	15G
Vibration (Operating) Sweep (Mil−5400)	Curve IIa & IIb (2.5G max)
Vibration Random (Mil−810)	3G rms
Humidity (non-condensing)	10 to 90% RH
Altitude (operating pressure)	0 to 10,000 feet

Related Documents

CY7C965 Raceway Crossbar Datasheet

Ordering Information

CYM9651	Single-slot Interlink extension module
CYM9652	4-slot Interlink Module with two expansion connections
CYM9653	8-slot Interlink Module with two expansion connections
CYM9654	12-slot Interlink Module with two expansion connections
CYM9655	16-slot Interlink Module with two expansion connections

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