RACEway Products from Cypress Semiconductor

Cypress Semiconductor now offers RACEway interconnect system developers an independent source for Interlink modules, crossbar chips, and RACEway on-ramp components compliant with the RACEway Interlink standard.

The RACEway Interlink standard is published and maintained by VITA (VMEbus and Futurebus International Trade Association). The VITA standards organization (VSO) has ratified the RACEway Interlink Specification which defines the data link protocol and the physical interface definition for the high-performance extension to the VMEbus standard.

RACEway Crossbar CY7C965

- 160 Mbyte per second per path Block Transfer Rates
- Six bidirectional ports
- Non-blocking architecture
- 361-pin CBGA package
- Implements Open Bus Standard (VITA 5−1994)
- Building Block for Scaleable Networks
- Preemptable prioritized transactions
- Adaptive Routing support

The CY7C965 RACEway Crossbar implements in one device the RACEway open standard for cross point interconnect (VITA 5−1994). The RACEway standard allows multiple processor systems to communicate using a crossbar technology that supports very high aggregate data transfer rates. Applications for the RACEway Crossbar include high-performance multiprocessing systems, and distributed processing systems. The RACEway Crossbar can be used in backplane-based applications or as switch elements on single boards.

The RACEway Crossbar can be connected in many different system configurations. In its simplest configuration, the Crossbar is used to interconnect six RACEway nodes using a single crossbar. Higher complexity systems may require the implementation of a large fabric of interconnected Crossbars.

RACEway Interlink Modules

- CYM9652 provides a 4 slot RACEway fabric
- CYM9653 provides an 8 slot RACEway fabric
- CYM9654 provides a 12 slot RACEway fabric
- CYM9655 provides a 16 slot RACEway fabric
- CYM9651 provides a single slot connection for expansion purposes

Cypress's RACEway Interlink Modules bring embedded supercomputing performance to real-time VME-based systems. As a backward-compatible upgrade, RACEway Interlink transforms the topology of an existing VMEbus chassis from a single transaction bus to a scaleable real-time fabric capable of over 1 Gbyte/sec of aggregate bandwidth. Interlink modules add interboard bandwidth to VME-based systems by providing multiple, concurrent, high-speed communication paths between VME boards interfaced to the RACEway Interlink stan-

dard. In addition to increased bandwidth, RACEway Interlink offers low latency and priority control, essential to real-time applications.

Mechanically, the RACEway Interlink Modules mount on the backplane of a VME chassis similar to industry-standard VSB backplane modules. Electrically, these modules are connected to the VME slots through the P2 chassis backplane connector. RACEway Interlink Modules implement the RACEway interconnect fabric, using the Cypress CY7C965 RACEway Crossbar device and appropriate clock and interface circuitry.

RACEway On-ramp: PitCREW

- Used to interface between FIFOs and the RACEway protocol.
- Drives/receives a RACEway port directly.
- Is programmed from the RACEway.
- Has a DMA engine capable of moving data between a local FIFO and the RACEway.
- Moves data at 160 MByte/sec peak and 140 MByte/sec sustained throughput.
- Able to write DMA status to RACEway for polling or mailbox interrupt.
- 144-pin, 8K gate Cypress CY7C387A FPGA.

PitCREW is an I/O data port for RACEway. It defines a simple FIFO interface local data port which is slave to its RACEway port. The PitCREW has an internal DMA engine which moves blocks of data between RACEway nodes and its FIFO port. This DMA engine is set in motion by commands received over the RACEway port. Data move instructions can be issued directly to the PitCREW RACEway port, or caused to be fetched by the PitCREW in a linked list fashion from memory associated with a RACEway node. All the logic required to control data movement between FIFOs and the RACEway resides in this device.

pASIC is a trademark of Quicklogic.

RACEway On-ramp: PitCREWjr

- Used to interface between FIFOs and the RACEway protocol.
- Drives/receives a RACEway port directly.
- Simple master control, automatic slave response.
- Moves data at 160 MByte/sec peak and 140 MByte/sec sustained throughput.
- Implemented in a Cypress CY7C384A, a 2K gate 100-pin FPGA.

PitCREWjr is a simple full-duplex on-ramp to the RACEway fabric. The device has a standard RACEway port and FIFO port. The controller functions either as a RACEway slave, moving data between RACEway and local FIFOs or as a RACEway master, again moving data between RACEway and local FIFOs. It connects to and drives a RACEway interlink port directly providing all required handshaking and control signaling. PitCREWjr's local FIFO port consists of a 32-bit bidirectional data bus and control signals for moving data between PitCREWjr and industry-standard FIFO components. The PitCREWjr has no programmable internal registers. Internal PitCREWjr state machines assemble and disassemble the route, address, and data long words embedded in the RACEway protocol. RACEway mastering is accomplished by controlling a single input signal.

Mercury Computer RIC−RINO Component Files

Data files are available for the RIC−RINO RACEway on-ramp chipset developed by Mercury Computer. This chipset is superseded by the PitCREW RACEway On-ramp for new designs. The two necessary items are a PROM file for the data path EPLD definition and a .CHP file for a CY7C384A pASIC which replaces the FPGA specified by Mercury. These files are provided on request.