4.6

CY7C964 Alternate BLT Initiation Operation for VIC068A and VIC64

Another method of loading the VMEbus block transfer address counters exists within the CY7C964. This method has been placed within its own section of the document because it is not completely compatible with the VIC block transfer initiation cycle.

The CY7C964 determines the source for loading the VMEbus master block transfer counter C3 by monitoring the arrival sequence of the MWB* and BLT* signals. For typical block transfer initiation cycles, the assertion of MWB* occurs prior to the assertion of the BLT*. The VMEbus master block transfer counter C3 loads from the local address pins, LA[7:0], as described within section 4.5.5.

Reversing the arrival order of these two signals changes the operation of the device. This is done at system design time by swapping the BLT* and MWB* inputs to the CY7C964. For proper operation, these signals must continue to operate in the same manner as they do on the VIC, even though they are no longer connected to the associated input pins on the CY7C964 which have the same name. Swapping these signals on the device changes the way that the VMEbus master block transfer counter C3 is loaded. In this mode it loads from the local data bus via latch L9. All other functions within the device operate in the same manner as described in Chapter 4.5.

Loading C3 is accomplished with a local cycle similar to the cycles needed to load the mask and compare registers. This cycle operates as follows: LDS is driven High, (most likely this signal is connected to LA2), the MWB* input pin of the CY7C964 is driven Low, (this pin is actually connected to the open collector BLT* output of the VIC), and STROBE is asserted. The local data bus should be driven to the appropriate value for the address to load into the C3 counters. STROBE is deasserted and the data is latched into L9 within the CY7C964. The local address decode signal used to assert MWB* on the CY7C964, (BLT* on the VIC), must be a three-state or an open-collector output. This signal must not be driven High or the VIC will be unable to perform block transfers.

A normal master block transfer initiation cycle is then performed, with one minor exception. The lower 8 bits of address LA[7:0] which are controlled by the VIC, must contain the

desired lower address. This is needed because the VIC operates in the typical block transfer initiation mode. The upper address LA[31:8] will be ignored by the CY7C964s during the initiation cycle.

This mode of operation allows the VMEbus master block transfer address counters to be loaded independent of the VMEbus address. This has advantages in some designs, but C3 cannot be used to source single cycle transfer addresses. This limitation should be considered while performing the design analysis to use this mode.

Table 4−14. Master Block Transfer Local Address Counter Operation

Logic	Functional Description	Operational Description	Required Condition	Parameter
L9	Select register	LDS, MWB* valid to STROBE falling edge	LDS=1, MWB*=0	Set-up t43
				Hold t44
	Load register	LD[7:0] valid to STROBE rising edge		Set-up t45
				Hold t46
	Minimum pulse width	STROBE		t46

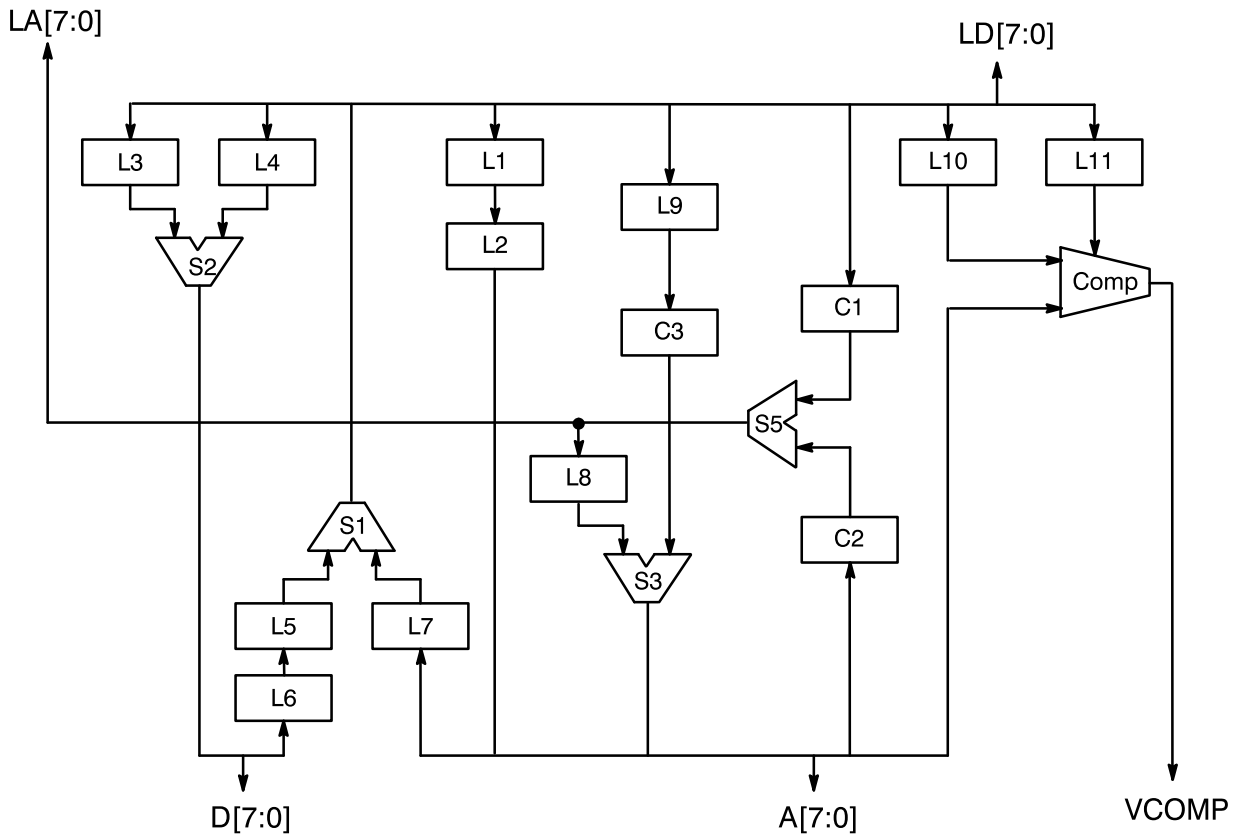

Figure 4−8. CY7C964 Alternate BLT Operation Block Diagram