4.8

AC Performance Specifications

Parameter	Description	Min. All Grades[1]	Max. (Com'l)	Max. (Ind)	Max. (Mil)	Unit	Comment
t1	LA[7:0] to A[7:0] propagation delay[2]		15	16	18	ns	
t2	LD[7:0] to D[7:0] propagation delay		16	17	19	ns	
t3	A[7:0] to LA[7:0] propagation delay		17	18	20	ns	
t4	D[7:0] to LD[7:0] propagation delay[2]		19	20	22	ns	
t5	LD[7:0] to A[7:0] propagation delay[2]		19	20	22	ns	D64=1
t6	A[7:0] to LD[7:0] propagation delay[2]		19	20	22	ns	D64=1
t7	ABEN* active to A[7:0] output enable delay[2]		11	11	12	ns	
t8	DENO* active to D[7:0] output enable delay[2]		14	15	16	ns	
t9	ABEN* active to D[7:0] output enable delay		14	15	17	ns	D64=1
t10	D64 active to D[7:0] output enable delay[2]		13	14	15	ns	ABEN*=0
t11	LAEN active to LA[7:0] output enable delay[2]		10	11	12	ns	
t12	DENIN* active to LD[7:0] output enable delay		15	16	18	ns	
t13	DENIN1* active to LD[7:0] output enable delay[2]		18	19	21	ns	D64=1
t14	D64 active to LD[7:0] output enable delay[2]		18	19	21	ns	DENIN1*=0
t15	ABEN* inactive to A[7:0] High-Z output disable delay[2]		8	10	12	ns	
t16	DENO* inactive to D[7:0] High-Z output disable delay[2]		12	14	15	ns	
t17	ABEN* inactive to D[7:0] High-Z output disable delay[2]		12	14	15	ns	D64=1
t18	D64 inactive to D[7:0] High-Z output disable delay[2]		14	15	16	ns	ABEN*=0
t19	LAEN inactive to LA[7:0] High-Z output disable delay[2]		13	14	15	ns	

Parameter	Description	Min. All Grades[1]	Max. (Com'l)	Max. (Ind)	Max. (Mil)	Unit	Comment
t20	DENIN* inactive to LD[7:0] High-Z output disable delay[2]		14	16	18	ns	
t21	DENIN1* inactive to LD[7:0] High-Z output disable delay[2]		14	16	18	ns	D64=1
t22	D64 inactive to LD[7:0] High-Z output disable delay[2]		19	21	24	ns	DENIN1*=0
t23	A[7:0] to VCOMP* High-to-Low propagation delay		18	19	21	ns	
t24	A[7:0] to VCOMP* Low-to-High propagation delay		16	17	19	ns	
t25	LD[7:0] set-up time to LEDO rising edge	7				ns	
t26	LD[7:0] hold time after LEDO rising edge	0				ns	
t27	LEDO minimum pulse width	7				ns	
t28	LD[7:0] set-up time to DENO* falling edge	0				ns	LEDO=0
t29	LD[7:0] hold time after DENO* falling edge	7				ns	LEDO=0
t30	DENO* minimum pulse width	10				ns	
t31	D[7:0] set-up time to DENIN* falling edge	5				ns	DENIN1*=0, LEDI=0
t32	D[7:0] hold time after DENIN* falling edge	5				ns	DENIN1*=0, LEDI=0
t33	DENIN* minimum pulse width	10				ns	
t34	D[7:0] set-up time to DENIN1* falling edge	5				ns	
t35	D[7:0] hold time after DENIN1* falling edge	5				ns	
t36	DENIN1* minimum pulse width	10				ns	
t37	D[7:0], A[7:0] set-up time to LEDI rising edge	7				ns	
t38	D[7:0], A[7:0] hold time after LEDI rising edge	0				ns	
t39	LEDI minimum pulse width	10				ns	
t40	LA[7:0] set-up time to LADO rising edge	5				ns	
t41	LA[7:0] hold time after LADO rising edge	5				ns	
t42	LADO minimum pulse width	10				ns	
t43	MWB*, LDS set-up time to STROBE falling edge	0				ns	

Parameter	Description	Min. All Grades[1]	Max. (Com'l)	Max. (Ind)	Max. (Mil)	Unit	Comment
t44	MWB*, LDS hold time after STROBE falling edge	5				ns	
t45	LD[7:0] set-up time to STROBE rising edge	5				ns	
t46	LD[7:0] hold time after STROBE rising edge	5				ns	
t47	STROBE minimum pulse width	10				ns	
t48	Local master block transfer address counter C1 LD[7:0] set-up time before MWB* falling edge	0				ns	BLT*, LAEN=0
t49	Local master block transfer address counter C1 LD[7:0] hold time after MWB* falling edge	5				ns	BLT*, LAEN=0
t50	Master block transfer local address counter C1 LD[7:0] set-up time to BLT* falling edge	0				ns	MWB*, LAEN=0
t51	Master block transfer local address counter C1 LD[7:0] hold time after BLT* falling edge	5				ns	MWB*, LAEN=0
t52	LCIN* set-up time to MWB* falling edge	5				ns	BLT_STATE, LAEN, FC1=1
t53	LCIN hold time after MWB* or BLT* falling edge	0				ns	BLT_STATE, LAEN, FC1=1
t54	MWB*, BLT* falling edge to LA[7:0] propagation delay		21	22	25	ns	BLT_STATE, LAEN, FC1=1
t55	MWB*, BLT* falling edge to LCOUT* propagation delay		24	25	28	ns	BLT_STATE, LAEN, FC1=1
t56	LCIN* to LCOUT* propagation delay[2]		17	18	20	ns	BLT_STATE, LAEN, FC1=1
t57	BLT*, MWB* minimum pulse width	10				ns	
t58	Slave block transfer local address counter C2, A[7:0] set-up time to D64 rising edge	5				ns	LADI=0
t59	Slave block transfer local address counter C2, A[7:0] hold time after D64 rising edge	5				ns	LADI=0
t60	Slave block transfer local address counter C2, A[7:0] set-up time to LADI rising edge	5				ns	D64=0
t61	Slave block transfer local address counter C2, A[7:0] hold time after LADI rising edge	5				ns	D64=0
t62	LCIN* set-up time to LADI rising edge	8				ns	D64=1

Parameter	Description	Min. All Grades[1]	Max. (Com'l)	Max. (Ind)	Max. (Mil)	Unit	Comment
t63	LCIN* hold time after LADI rising edge	0				ns	D64=1
t64	LADI rising edge to LA[7:0] valid propagation delay		15	16	18	ns	D64=1, FC1=0
t65	LADI rising edge to LCOUT* valid propagation delay		20	21	24	ns	D64=1, FC1=0
t66	LADI minimum pulse width	10				ns	
t67	Master block transfer VMEbus address counter LA[7:0] set-up time to MWB* rising edge	5				ns	BLT_STATE=1, BLT_INIT=1
t68	Master block transfer VMEbus address counter LA[7:0] hold time after MWB* rising edge	5				ns	BLT_STATE=1, BLT_INIT=1
t69	LADO falling edge to A[7:0] valid propagation delay		23	24	27	ns	BLT_STATE, DUAL_PATH=1, BLT_INIT=0
t70	LADO rising edge to A[7:0] valid propagation delay[2]		24	25	28	ns	BLT_STATE=1, DUAL_PATH=0, BLT_INIT=0
t71	LADO falling edge to VCOUT* valid propagation delay		26	27	30	ns	BLT_STATE, DUAL_PATH=1, BLT_INIT=0
t72	LADO rising edge to VCOUT* valid propagation delay[2]		30	33	36	ns	BLT_STATE, DUAL_PATH=0, BLT_INIT=0
t73	LADO minimum High or Low pulse width	10				ns	
t74	LDS rising edge to LD[7:0] valid propagation delay[2]		20	21	24	ns	D64=1
t75	LDS falling edge to LD[7:0] valid propagation delay		20	21	24	ns	D64=1
t76	D64 rising edge to LD[7:0] valid propagation delay[2]		21	22	24	ns	
t77	D64 falling edge to LD[7:0] valid propagation delay		21	22	24	ns	
t78	D64 rising edge to D[7:0] valid propagation delay[2]		16	16	18	ns	
t79	D64 falling edge to D[7:0] valid propagation delay[2]		19	19	21	ns	
t80	D64 rising edge to A[7:0] valid propagation delay[2]		15	16	18	ns	BLT_STATE=0
t81	D64 falling edge to A[7:0] valid propagation delay[2]		16	17	19	ns	BLT_STATE=0

Parameter	Description	Min. All Grades[1]	Max. (Com'l)	Max. (Ind)	Max. (Mil)	Unit	Comment
t82	D64 rising edge to A[7:0] valid propagation delay[2]		19	19	22	ns	BLT_STATE=1
t83	D64 falling edge to A[7:0] valid propagation delay		20	21	23	ns	BLT_STATE=1
t84	ABEN* falling edge to A[7:0] valid propagation delay[2]		11	11	12	ns	BLT_STATE=1
t85	FC1 rising edge to LA[7:0] valid propagation delay[2]		14	15	17	ns	
t86	FC1 falling edge to LA[7:0] valid propagation delay		17	18	20	ns	
t87	FC1 falling edge to LCOUT* valid propagation delay[2]		17	18	20	ns	
t88	FC1 rising edge to LCOUT* valid propagation delay		17	18	20	ns	
t89	LADO set-up time to MWB*, BLT* rising edge	0				ns	BLT_STATE=1
t136	LADO hold time after MWB*, BLT* rising edge	7				ns	BLT_STATE=1
t137	BLT* set-up time to MWB* falling edge	5				ns	
t90	BLT* hold time after MWB* falling edge	5				ns	
t131	LD[7:0] to DENO* falling edge set-up	5				ns	
t132	LD[7:0] after DENO* falling edge	5				ns	
t133	LCIN* hold time after BLT* falling edge	5				ns	