4.9
Pin Description

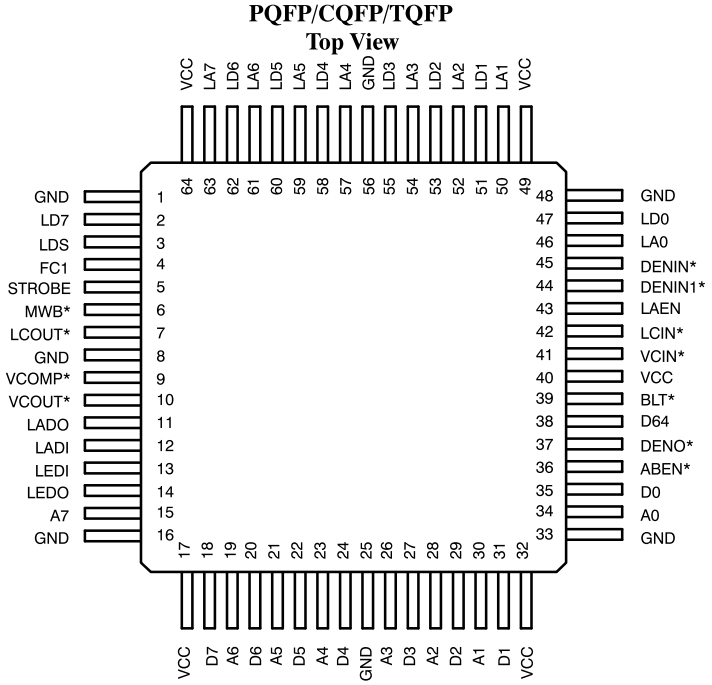
4.9.1 Pin Definitions

QFP Pin No.	PGA Pin No.	Signal Name	Type	Description
1	E1	GND	Power	Ground
2	L2	LD7	Three-state I/O	Local data transceiver 7
3	K3	LDS	Input	Register select bit
4	L3	FC1	Input	Function code 1 control signal
5	K4	STROBE	Input	Comparator register load control signal
6	L4	MWB*	Input	Module wants VMEbus control signal
7	K5	LCOUT*	Output	Local address counters carry out signal
8	L5	GND	Power	Ground
9	K6	VCOMP*	Output	VMEbus address comparator out signal
10	L6	VCOUT*	Output	VMEbus address counter carry out signal
11	K7	LADO	Input	Latch address out control signal
12	L7	LADI	Input	Latch address in control signal
13	K8	LEDI	Input	Latch enable data in control signal
14	L8	LEDO	Input	Latch enable data out control signal
15	K9	A7	Three-state I/O	High drive address transceiver 7
16	A3	GND	Power	Ground
17	A2	V_{CC}	Power	V_{CC}
18	K11	D7	Three-state I/O	High drive data transceiver 7
19	J10	A6	Three-state I/O	High drive address transceiver 6
20	J11	D6	Three-state I/O	High drive data transceiver 6
21	H10	A5	Three-state I/O	High drive address transceiver 5
22	H11	D5	Three-state I/O	High drive data transceiver 5
23	G10	A4	Three-state I/O	High drive address transceiver 4

QFP Pin No.	PGA Pin No.	Signal Name	Type	Description
24	G11	D4	Three-state I/O	High drive data transceiver 4
25	L9	GND	Power	Ground
26	F11	A3	Three-state I/O	High drive address transceiver 3
27	E10	D3	Three-state I/O	High drive data transceiver 3
28	E11	A2	Three-state I/O	High drive address transceiver 2
29	D10	D2	Three-state I/O	High drive data transceiver 2
30	D11	A1	Three-state I/O	High drive address transceiver 1
31	C10	D1	Three-state I/O	High drive data transceiver 1
32	K10	V_{CC}	Power	V_{CC}
33	B10	GND	Power	Ground
34	A10	A0	Three-state I/O	High drive address transceiver 0
35	B9	D0	Three-state I/O	High drive data transceiver 0
36	A9	ABEN*	Input	High drive address bus enable signal
37	B8	DENO*	Input	High drive data bus enable signal
38	A8	D64	Input	D64 mode enable control signal
39	B7	BLT*	Input	Block transfer control signal
40	B2	V_{CC}	Power	V_{CC}
41	B6	VCIN*	Input	VMEbus address counter count enable signal
42	A6	LCIN*	Input	Local address counter count enable signal
43	B5	LAEN	Input	Local address enable control signal
44	A5	DENIN1*	Input	Data enable in 1 control signal
45	B4	DENIN*	Input	Data enable in control signal
46	A4	LA0	Three-state I/O	Local address transceiver 0
47	B3	LD0	Three-state I/O	Local data transceiver 0
48	F10	GND	Power	Ground
49	A7	V_{CC}	Power	V_{CC}
50	B1	LA1	Three-state I/O	Local address transceiver 1
51	C2	LD1	Three-state I/O	Local data transceiver 1
52	C1	LA2	Three-state I/O	Local address transceiver 2
53	D2	LD2	Three-state I/O	Local data transceiver 2
54	D1	LA3	Three-state I/O	Local address transceiver 3

QFP Pin No.	PGA Pin No.	Signal Name	Type	Description
55	E2	LD3	Three-state I/O	Local data transceiver 3
56	L10	GND	Power	Ground
57	F2	LA4	Three-state I/O	Local address transceiver4
58	F1	LD4	Three-state I/O	Local data transceiver 4
59	G2	LA5	Three-state I/O	Local address transceiver 5
60	G1	LD5	Three-state I/O	Local data transceiver 5
61	H2	LA6	Three-state I/O	Local address transceiver 6
62	H1	LD6	Three-state I/O	Local data transceiver 6
63	J2	LA7	Three-state I/O	Local address transceiver 7
64	J1	V_{CC}	Power	V_{CC}
	K2	GND	Power	Ground
	K1	V_{CC}	Power	V_{CC}
	B11	GND	Power	Ground
	C11	V_{CC}	Power	V_{CC}

4.9.2 Pin Configurations



68-Pin Ceramic PGA
Bottom View