Glossary

245 7400-family part type that is an 8-bit (octal) bus transceiver with controls for direction and enabling of drivers.

543 7400-family part type that is an 8-bit (octal) bus transceiver with controls for latch enable, output enable, and direction flow.

68K A Motorola 68000, 68010, 68020, 68030 or 68040 microprocessor.

accelerated mode A mode of operation where the VIC068A will continuously assert the PAS* signal for the duration of a DMA operation. The VIC068A expects the DSACK* signal to be continuously asserted for the duration of the DMA operation as well.

arbitration timeout A timeout that occurs when no module responds to a VMEbus bus grant.

assertion The forcing of a signal to its TRUE state.

base address The starting point of an address region defined by the mask register.

block transfer length The total length, in bytes, of a block transfer. In terms of the VIC068A, a block transfer may or may not contain more then one burst.

block transfer w/DMA A VIC068A block transfer mode in which the VIC068A obtains local bus mastership and performs a VMEbus block transfer utilizing DMA on the local bus.

boundary crossing The crossing of a 256-byte local or VMEbus boundary during a block transfer.

buffer control signals VIC068A signals which control the operation of external address and data latches/buffers.

burst length The length, in VMEbus transfers, of a VMEbus block transfer burst. In terms of the VIC068A, there may or may not be more then one burst per block transfer.

byte An 8-bit unit of data.

clock-tick interrupt An optional, periodic interrupt issued by the VIC068A.

daisy-chain A type of VMEbus signal in which a signal level is propagated from board to board starting from slot 1 and ending with the last occupied slot.

data size The size of a VMEbus data transfer independent of the physical bus size (byte, word, etc.).

deadlock In the context of the VIC068A, this is a condition where the local bus requires the use of the VMEbus and the VMEbus requires the use of the local bus. In this condition, the VIC068A requires the current local bus master remove its bus tenure to let the VMEbus access proceed.

deassertion The forcing of a signal to its FALSE state.

DMA Direct Memory Access. With the VAC068A, this refers to either DMA to the VMEbus or DMA to another interface controller.

DMAAT0 Module-based DMA Transfer Access Timing. The data acquisition timing the VIC068A uses for the first transfer of a module-based DMA transfer. This timing is programmed in bits 3–0 in the SSiCR1.

DMAAT1 Module-based DMA Transfer Access Timing. The data acquisition timing the VIC068A uses for the second and subsequent transfers of a module-based DMA transfer. This timing is programmed in bits 7–4 in the SSiCR1.

DST The local data strobe minimum assertion timing. This timing is programmed in bit 4 of the LBTR.

dual-path A mode of operation which allows a single-cycle master operation to be performed by the VIC068A during interleave periods.

fair requester A VMEbus requester who waits until all requests on its particular VMEbus request level are inactive before requesting the VMEbus.

Force EPROM A VAC068A mode of operation that asserts EPROMCS* after reset.

global switch A local interrupt issued by a VMEbus module to multiple VMEbus slaves.

IMAC Indivisible Multiple Address Cycle.

initiation cycle The local cycle which initiates a VMEbus block transfer with local DMA.

interleave period The period of time between block transfer bursts.

interprocessor communication facilities
Various VIC068A register and facilities available by VMEbus accesses.

IPL Interrupt priority level.

ISAC Indivisible Single Address Cycle

local (local side) Resources that connect to the non-VMEbus signals of a VIC068A or VAC068A.

longword (lword) A 32-bit unit of data.

mail box An area of memory reserved for passing messages.

mask The comparison of only selected address bits for the purpose of specifying a range of don't-care conditions.

master block transfer A mode of operation where the VIC068A performs a VMEbus block transfer.

master read The act of transferring data from a VMEbus slave to a VMEbus master.

master write The act of transferring data from a VMEbus master to a VMEbus slave

master write posting A VMEbus master operation where the VIC068A captures outgoing VMEbus write data and acknowledges the local side immediately. This removes the VMEbus access time from local resources.

MBAT0 Master Block Transfer Access Timing. The data acquisition timing the VIC068A uses for the first transfer of a master block transfer with local DMA. This timing is programmed in bits 3–0 in the SSiCR1.

MBAT1 Master Block Transfer Access Timing. The data acquisition timing the VIC068A uses for the second and subsequent transfers of a master block transfer with local DMA. This timing is programmed in bits 7–4 in the SSiCR1.

module A VMEbus circuit card.

module-based DMA A mode of operation where the VIC068A transfers data from one local resource to another utilizing DMA.

module switch A local interrupt issued by a VMEbus module to a single VMEbus slave.

MOVEM block transfer A VIC068A block transfer mode in which the local resource maintains local bus mastership while having the VIC068A perform transfers using block transfer protocol on the VMEbus.

non-accelerated mode A mode of operation where the VIC068A will toggle the PAS* signal for each transfer of a DMA operation. The VIC068A expects the DSACK* signal to toggle for each transfer of the DMA operation as well.

port size The physical size of the VMEbus modules data bus (D8, D16, D32, etc.)

pseudo cycle A block transfer with local DMA, initiation cycle

redirection Re-mapping VMEbus slave select address ranges to a specific local chip select output.

region An area of memory defined by one of three boundary registers in the VAC068A.

rescinding output A three-state output which is first driven High before it is three-stated.

RMC	An indivisible read-modify-write cycle.
SAT	Slave Access Timing. The data acquisition timing the VIC068A uses while performing a slave transfer. This timing is programmed in bits 3-0 in the SSiCR1.
SBAT0	Slave Block Transfer Access Timing. The data acquisition timing the VIC068A uses for the first transfer of a slave block transfer. This timing is programmed in bits 3-0 in the SSiCR1.
SBAT1	Slave Block Transfer Access Timing. The data acquisition timing the VIC068A uses for the second and subsequent transfers of a slave block transfer. This timing is programmed in bits 7-4 in the SSiCR1.
self-access	A condition where the VIC068A, as the VMEbus master, has selected itself as the VMEbus slave.
slave block transfer	A mode of operation where the VIC068A is slave to a VMEbus block transfer.
slave read	The act of transferring data from a VMEbus slave to a VMEbus master.
slave write	The act of transferring data from a VMEbus master to a VMEbus slave
slave write posting	A VMEbus operation where the VIC068A captures incoming VMEbus write data and acknowledges the VMEbus immediately. This removes the local access time from VMEbus resources.
transfer timeout	A timeout that occurs when no module responds with an acknowledge to a data transfer.
turbo	A mode of operation in which the VIC068A reduces certain delays including set-up times.
UART	Universal Asynchronous Receiver Transmitter.
VAC068A	VMEbus Address Controller.
valid slave select	A fully qualified request for slave operations.
VIC068A	VMEbus Interface Controller.
VITA	VMEbus International Trade Association.
VSB	VMEbus Subsystem Bus.
word	A 16-bit unit of data.