How to Use This Book

This guide provides the hardware and software designer with detailed information on the Cypress Semiconductor VMEbus Interface Products. It may also be used to provide detailed information regarding existing off-the-shelf VMEbus modules that utilize the Cypress line of interface products.

This document is not intended to instruct the reader on VMEbus standards and protocol. First-time VMEbus designers and users requiring such information are encouraged to refer to the VMEbus specification (ANSI/VITA−1−1994).

Throughout this specification, specific conventions are used when referring to VMEbus signals, terms, and register bit and bit fields.

- The terms High or H are used to specify actual $>V_{IH}$ or $>V_{OH}$ levels. The terms Low or L are used to specify actual $<V_{IL}$ or $<V_{OL}$ levels.
- Active Low signals are followed by an asterisk (*).
- Active High signals, clock signals, and address/data buses do not have an asterisk.
- The terms *assertion* and *deassertion* are used to indicate the forcing of a signal to a particular state. Assertion means forcing a signal to its TRUE or active state. Deassertion refers to forcing a signal to its FALSE or inactive state. These terms are used independent of the actual voltage levels represented.
- Address and data buses (or portions thereof) are referred to using a bus[MSB:LSB] format. For example, the entire VMEbus data bus is referred to as D[31:0].
- An individual bit of an address or data bus is referred to using a bus[bit] format. For example, bit 0 of the local address bus is referred to as LA[0] or, where space was restrictive, LA0.
- When referring to address and data buses with a user-specific limit, a "+" character is used to indicate the limit. For example, to refer to the range from LA bit 0 to some user-specified or unknown limit, the term LA[+:0] is used. LA bit 31 to a lower user-specified or unknown limit is referred to as LA[31:+].
- When referring to one or more related signals or registers containing numbers, the lowercase letter "i" is used to indicate the signal(s). For example, when referring to one or

more of the VMEbus bus request signals (BR3*, BR2*, BR1*, and/or BR0*), the term BRi* is used. When referring to the SS0CR0 and/or the SS1CR0 register, the term SSiCR0 is used.

- When referring to a specified group of signals ending in a number, a slash (/) is used to separate the signals. For example, when referring to the SIZ1 and SIZ0 signals, the term SIZ1/0 is used.
- Specific bits of a register are referred to in a register[bit] format. Ranges of bits are referred to in a register[upper:lower] format.
- Setting register bit or bits refers to writing a 1 (one) into the respective bits.
- Clearing register bit or bits refers to writing a 0 (zero) into the respective bits.
- The term *module* refers to a VMEbus circuit board. Depending on the context, module may or may not imply a VMEbus circuit board.
- The terms *local* or *local side* refer to CPU, memory, or other resources that connect to the non-VMEbus signals of the VMEbus interface device.
- The terms *master write* and *slave write* both imply a VMEbus write operation where data is transferred from a VMEbus master to a VMEbus slave. *Master read* and *slave read* both imply VMEbus read operations where data is transferred from a VMEbus slave to a VMEbus master.
- All hexadecimal values are preceded by a dollar sign ($).
- The term *byte* is used to indicate 8 bits. The term *word* is used to indicate 16 bits. The terms *longword* and *lword* are used to indicate 32 bits.
- The term 68K is used to indicate a member of the Motorola CISC family of microprocessors (i.e., MC68000 through MC68040).
- The letter “T” is used to indicate the clock input period.
- The term *rescinding* is used to indicate a three-state output that is driven High before it is three-stated. See section 1.11.4.
- The letters “L” and “H” are used to indicate a High or Low value driven *by* the VMEbus interface device. The numbers “1” and “0” are used to indicate a High or Low value driven *to* the VMEbus interface device.