3.8
DRAM Control Description

3.8.1 Overview

The CY7C960 contains a high-performance DRAM controller, developed to take advantage of DRAMs operating in Fast Page Mode. By using Fast Page Mode devices, VMEbus MBLT transfer rates of 80 Mbyte per second are attainable with DRAM RAS*-access times of 70 ns. With appropriate buffering on the DRAM address and control signals, 16 Mbytes of DRAM can be directly accommodated (using 4-Mbit devices). With minimal external decoding logic generating multiple RAS*/CAS* signals, larger memory arrays can be controlled. When higher capacity DRAM devices become readily available, the memory arrays increase accordingly.

The CY7C960 is configured by the user to work with local DRAM during the initialization sequence. This configuration determines the function of several pins (RAS*, CAS*, ROW, COL, and REGION3/CS2). RAS* and CAS* provide the well-known address strobe signals for the DRAM array, ROW and COL provide address enable signals for strobing the row and column addresses into the DRAM array. If DRAM mode is selected during the configuration sequence, then the REGION3/CS2 pin becomes the CS2 output: 8 regions are available in DRAM mode requiring only three REGION decode inputs.

Figure 3−26 shows an example of the use of the DRAM control signals. ROW enables the upper bits of the local address bus to be latched in the DRAM by RAS*. COL enables the lower address bits to be latched by the use of the Data Byte Enable signals. In the example chosen, the DBE signals are connected to the CAS* inputs of the DRAMs, and the CY7C960 has been programmed to provide refresh timing on the DBE pins (DBE Refresh Enabled)

The LACK input may be used to acknowledge DRAM cycles. If LACK is tied Low, then the cycle is self timed using the programmed values for CAS* assert and CAS* precharge. The user may prevent DRAM CAS* bursts by the use of the LACK signal. This is done

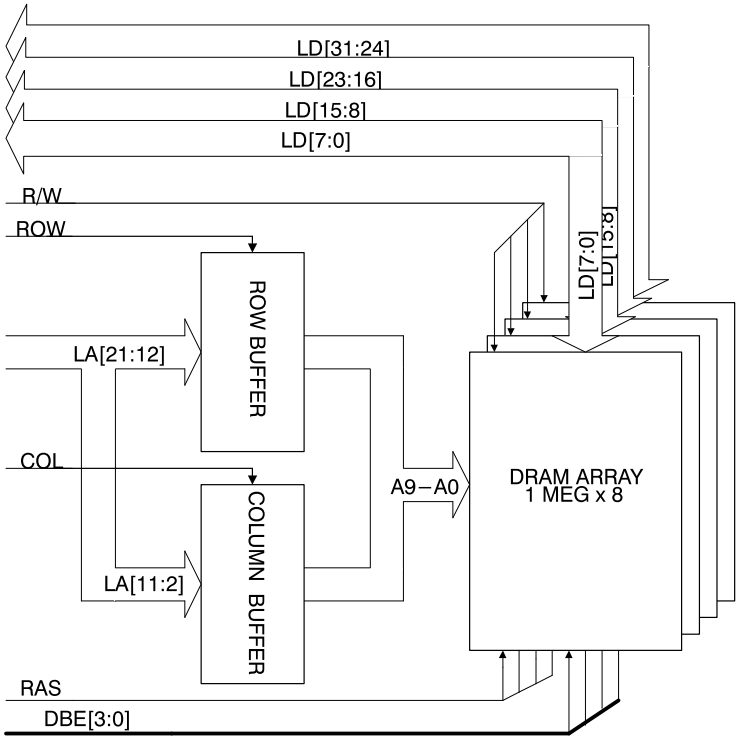

Figure 3–26. DRAM Signal Usage

by maintaining LACK High until the DRAM CAS* burst is to be permitted. Once LACK is driven Low and CAS* is asserted by the CY7C960, the DRAM access is no longer affected by LACK until RAS* deasserts, signaling the end of the current access (useful in dual-port applications to hold off VMEbus accesses to DRAM).

3.8.2 Types of DRAM

The CY7C960 controls Fast Page Mode DRAMs. This is an industry standard mode of operation. For 80 Mbyte/second burst transfer rate, 70-ns (RAS*-access) devices, or faster, should be used. The CY7C960 can be configured to operate with a wide range of DRAM timings. For example, if an 80-MHz clock is applied to the device the range of timings is given below. If a lower frequency is used the times scale as shown in the AC Timings Specification (see Chapter 3.12).

The access time of a page-mode DRAM is determined by two factors: the time from application of RAS* to the data becoming available, and the time from application of CAS*. The fastest method for getting bursts of data out of or into memory is to maintain RAS*

Low, and cycle CAS*. The access time for the first cycle is determined mainly by the RAS* access time, but subsequent cycles are shorter, determined by the CAS* access time. The amount of data that can be transferred in one burst is bounded by the size of the DRAM's row. When a row boundary is encountered it is necessary to reassert RAS, and hence another long cycle occurs.

3.8.3 VMEbus Implications

VMEbus transfers match DRAM Page Mode Accesses quite closely. When AS* is asserted the first cycle is generally longer than subsequent cycles, especially if the transaction involves an address broadcast cycle. For optimizing the slave's performance, RAS* is driven whenever AS* goes LOW. This starts the page mode cycle to the DRAMs. If the VMEbus transaction is not intended for the CY7C960, then RAS* is deasserted, and no DRAM cycle occurs. If the transaction is directed to the CY7C960, and the cycle type is enabled for the Region being addressed, then a DRAM cycle occurs. The programmable delays for DRAM cycle timing are then used as the cycle progresses. The first cycle therefore uses the RAS*/CAS* Delay parameter to ensure that the RAS* access time for the DRAM is met, and CAS* assert and precharge time parameters ensure that the shorter CAS* access time is used for subsequent cycles.

When a VMEbus boundary is encountered (256 byte for BLT, 2048 byte for MBLT), the address is rebroadcast by the VMEbus master. This causes AS* to cycle, which in turn causes RAS* to cycle. This ensures that no problems occur due to overflowing a page boundary in the DRAM, as the local address is aligned to the VME address. Put another way, the maximum number of transfers that can occur between RAS* cycles is 256. Even the smallest page mode DRAMs have page lengths that are a multiple of this number, so a page boundary in the DRAM is guaranteed to correspond to an address boundary on the VMEbus. Therefore RAS* is guaranteed to cycle at DRAM page boundaries.

3.8.4 Refresh Cycles

The CY7C960 contains a refresh controller. The refresh period and function enable are set during device configuration. The controller can be enabled to generate CAS* before RAS*

Refresh cycles at preprogrammed intervals. The controller employs a hidden refresh strategy and is fully integrated into the response of the CY7C960 local interface. Each time a refresh interval expires, a burst of 4 CAS* before RAS* refresh cycles is scheduled. At the next opportunity a refresh burst will be generated. During DRAM accesses, refresh is allowed at double longword address boundaries. Refresh is blocked during burst accesses to I/O regions if the DBE refresh enable feature is enabled. Refresh is always allowed between slave accesses and does not interfere with transaction decoding. If refresh cannot occur before additional intervals expire, a proportional number of additional CAS* before RAS* cycles will be scheduled. Overflow and consequent loss of refresh control timing occurs if 256 intervals elapse without a refresh burst.

3.8.5 Refresh Timing

The CY7C960 DRAM control can be programmed by specifying 4 parameters which are part of the initialization bit stream. These 4 parameters are RAS*/CAS* Delay Time, CAS* Assert Time, CAS* Precharge Time, and RAS* Precharge Time. Each is a 3-bit eight valued field. *Table 3–7* relates the programmed values for three of the parameters to the timing diagram of *Figure 3–27*. CAS* Precharge Time (not shown) is used to adjust the minimum deassertion time between CAS* assertions during CAS* bursting. The DRAM timing is designed to support 60-ns fast page mode DRAM.

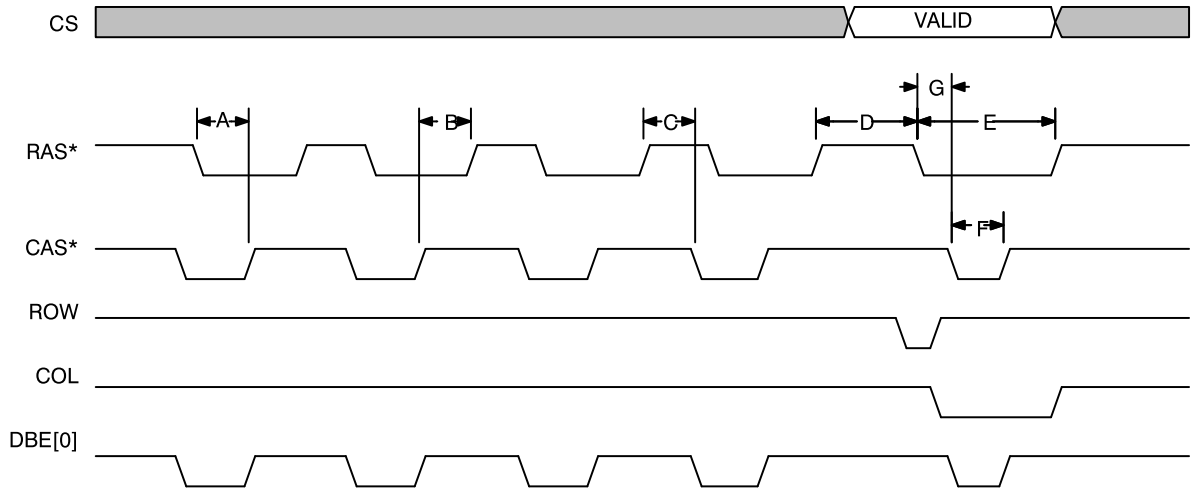

Figure 3–27. Programming DRAM Timing

Table 3−7. DRAM Timing

A	CAS* Assert Time − 1	2T − 9T
B	RAS* Precharge Time − 3	2T − 9T
C	RAS* Precharge Time − 3	2T − 9T
D	RAS* Precharge Time	5T − 12T
E	RAS* Precharge Time	5T − 12T
F	CAS* Assert Time	3T − 10T
G	RAS*/CAS* Delay Time	2T − 9T

3.8.6 DBE Refresh Enable Feature

Refresh control behavior is fundamentally affected by the DBE refresh enable feature of the CY7C960. If the feature is off, refresh is mutually exclusive with DRAM accesses, but is unrestricted when a DRAM access is not in progress. During I/O accesses, CAS* before RAS* refresh bursts can occur at any time with respect to access to I/O regions. R/W*, DBE, and CS* outputs are oblivious to activity on RAS* and CAS*. DRAM RAS* and CAS* signals can be connected directly to the CY7C960, while DRAM OE and WE signals must be gated with the CY7C960 COL signal to provide the distinction between DRAM access and DRAM refresh. The COL signal is inactive except during CAS* cycles of DRAM access.

If the DBE refresh enable feature is turned on, refresh will be mutually exclusive with DRAM accesses and I/O accesses. This is a necessary consequence of providing refresh CAS* behavior on the DBE signals. With the feature enabled, CS is deasserted and R/W* driven High during refresh bursts. This mode allows the use of CS signals to explicitly select DRAM and the use of DBE signals as byte addressable CAS signals. DRAM OE and WE can be gated by CY7C960 CS signaling. Where possible, the refresh occurs in parallel with user transactions such as I/O transactions with no DRAM enabled.

Figure 3−27 shows a refresh burst delaying a DRAM access with DBE Refresh Enable turned on. Note that R/W* (not shown) is High, and ROW and COL are inactive during the refresh burst. The four DBE signals (only one is shown) and CAS* toggle in concert with RAS* for four cycles. After a RAS* precharge time, row and column addresses are established and CS, R/W*, RAS*, CAS*, and DBE appropriate to the DRAM access are asserted.

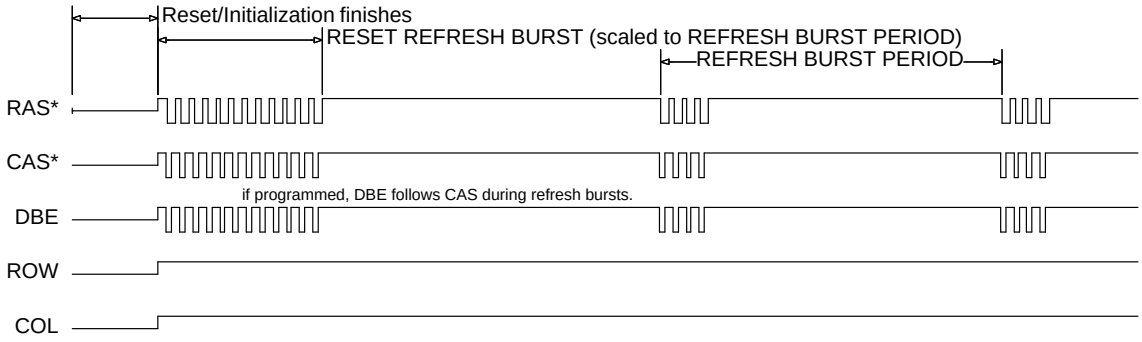

Figure 3−28. Refresh after Initialization

3.8.7 Refresh and Reset

If the CY7C960 is reset by a front panel switch, independently from the VMEbus SYSRESET*, a “Warm Reset” is supported whereby DRAM data is preserved across the reset period. The initialization sequence, whether Serial, Combo, or VMEbus method, is followed immediately by a DRAM Refresh burst of appropriate length. *Figure 3−28* illustrates this behavior. The actual length is calculated by the CY7C960 based upon the refresh timing parameters just loaded by the initialization sequence. The assumption is made that the DRAM was being refreshed normally up to the point that the local Reset signal was generated, so the CY7C960 calculates the number of refresh cycles needed based upon the time taken by the Serial Method of configuration (380 μsec). The reason for this is that the VMEbus method of configuration is faster under normal circumstances so the worst case for refresh purposes is Serial. Note however that if the VMEbus method is delayed substantially for any reason (for example Bus occupancy or bus tenure problems) then the refresh burst may not be sufficient to maintain DRAM contents. If warm reset is desired, the Serial configuration method is recommended.

During the extended refresh burst following a reset, the CY7C960 handles transactions normally. The user is cautioned that creating a local bus condition which blocks refresh after warm reset could overflow the refresh controllers hidden refresh counter which is limited to storing 256 refresh intervals.

Figure 3−29 shows the timing of the signals associated with a series of standard VMEbus transactions. The figure shows three back-to-back transactions: a LOCK cycle, an A64/D16 BLT, and an A24 Serial single cycle I/O transaction. The CY7C960 is configured as the re-

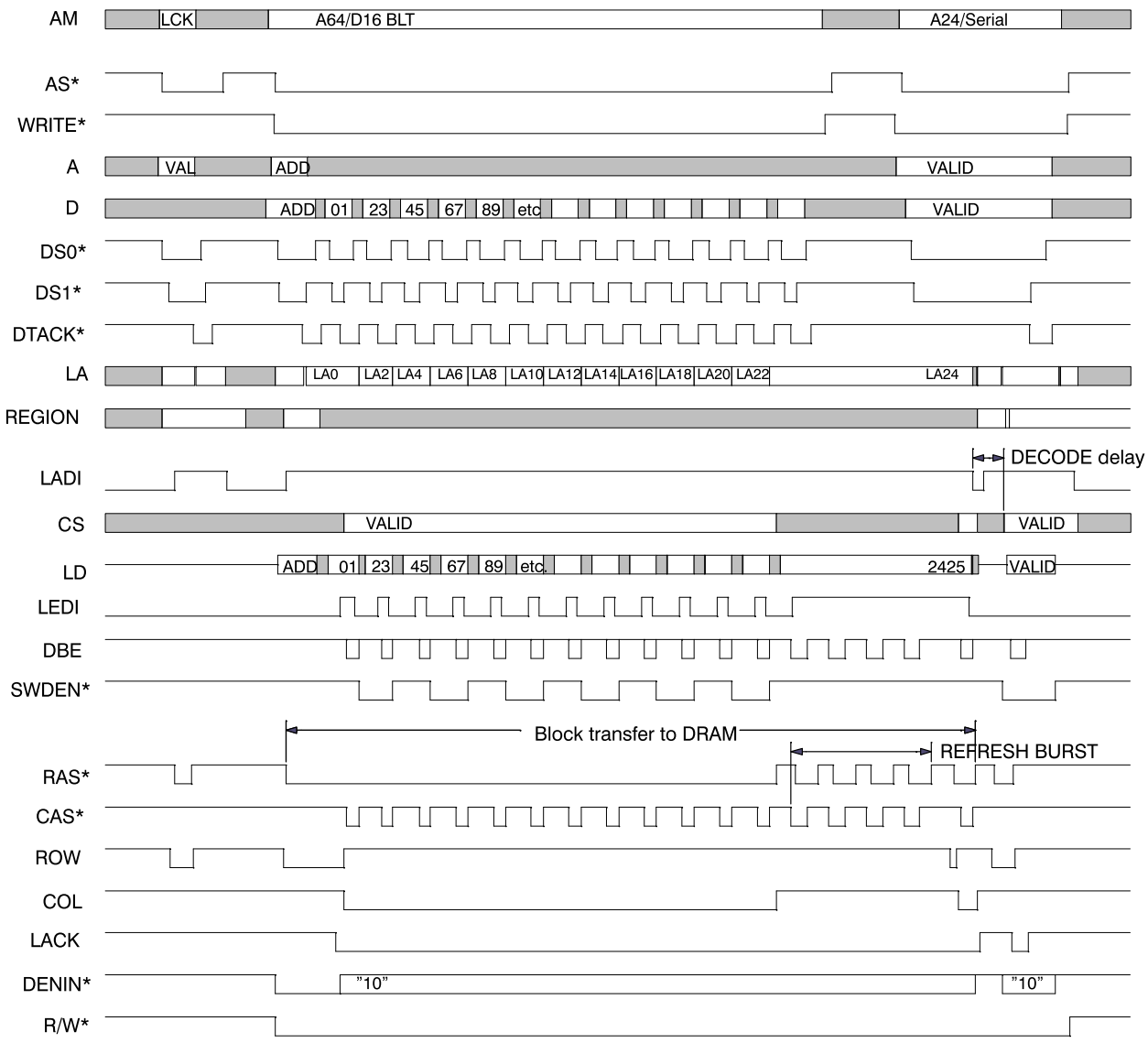

Figure 3−29. DRAM Transaction Timing

sponding slave to all three. The LOCK cycle is DTACKed, but no local activity takes place as the CY7C960 does not provide full LOCK support. The A64/D16 BLT write commences with an address broadcast cycle followed by 13 data beats. A refresh burst interrupts local bus activity, delaying the write of the last word. CY7C960 response to the I/O transaction is delayed until the local bus is ready. The A24 I/O transaction then completes.

The LOCK cycle illustrates DRAM mode RAS* behavior. RAS* will always assert in response to VMEbus AS* assertion when CY7C960 is ready, regardless of transaction decode status. This behavior speeds up response for transactions that are decoded. It generates a harmless RAS*-only refresh signaling for transactions that are not decoded. Local bus hold-

off always blocks RAS* assertion while LACK is deasserted. The CY7C961 should be used if full LOCK cycle support is desired.

The A64/D16 BLT write shows the posted nature of block writes. RAS* latches the flow-through address during the address broadcast. The CY7C960 latches data in the interface with the LEDI signal and drives DTACK* as it begins local bus write activity. The CS outputs are driven with the pattern appropriate for the Region being addressed. CS signals are set up to the CAS* burst and remain valid through a burst. SWDEN* and DBE signals indicate the bytes valid for each data cycle. The BLT progresses, with the CY7C960 incrementing local addresses, and providing CAS*, DBE, and SWDEN* appropriate to each DRAM access.

In the example illustrated, a DRAM Refresh occurs at the end of the BLT, prior to the completion of the last local write. ROW and COL signals go inactive, and the four CAS* before RAS* cycles occur. Then the CY7C960 drives the original ROW address on the local address bus and drives ROW and RAS* to relatch the ROW address in the DRAMs. Next, COL, CAS*, DBE, and SWDEN* are driven appropriately, and the posted data in the CY7C964s is written to DRAM.

While this delayed write is going on, the A24 Serial VMEbus cycle has commenced that is also addressed to the CY7C960 board. Note that the cycle is extended until the previous local activity, refresh and posted data, has completed. Then the VME cycle is DTACK'ed, the data is posted (it is another write operation), and the local signals are driven appropriately. In this case the single cycle is addressed to a Region where DRAM is disabled, so no CAS* occurs The chip select pattern is driven by the CY7C960 along with the correct DBE and SWDEN*.

Those developers familiar with VMEbus transactions will know of the challenge associated with handling multiplexed, posted Write transactions together with address boundary crossing, and high priority refresh cycles. The CY7C960 handles all possible cases without intervention or monitoring being necessary. For example, a refresh burst may preempt the local writing of the last 64-bit MBLT transaction posted prior to a 2K boundary crossing. The CY7C960 completes the refresh burst, but in parallel, the rebroadcast VMEbus address is signalled by AS* toggling and DS* going Low. This address broadcast cycle cannot be completed immediately: first CY7C960 drives RAS* to relatch the PREVIOUS page address which is still held on the local address bus by the CY7C964s. Next, two CAS* cycles occur in order to write the two 32-bit longwords that were posted from the 64-bit write. CY7C960

then goes through a complete decode cycle to ascertain whether the newly-broadcast VMEbus address is still in an enabled Region: if so it cycles RAS* to latch the NEW page address, in parallel, DTACKing the VMEbus address broadcast cycle. Then the block transfer continues normally.

3.8.8 Local Acknowledge Behavior

In some applications it may be desirable to delay DRAM cycles. In these cases, the local signal LACK is used. If LACK is Low, CAS* is asserted at the appropriate time. If LACK is High when RAS*/CAS* delay time expires, then CAS remains deasserted: when LACK goes Low CAS* is asserted. This provides a mechanism for holding off DRAM accesses if desired. Note that this operation is limited to the FIRST CAS* after RAS* is asserted, not a cycle-by-cycle basis. Anytime RAS* is asserted the opportunity to delay the cycle occurs.

If LACK is High for a considerable period of time, the refresh burst will become due. CY7C960 initiates the refresh burst. After the refresh burst is complete, the part continues awaiting the arrival of LACK. If LACK has gone Low during the refresh burst the cycle completes without further delay.

Figure 3−30 shows the use of LACK. An A32/D16 BLT Read commences: the CY7C960 determines that it is addressed and the transfer is enabled, and so drives the local signals appropriately. ROW and RAS* latch the ROW address in the DRAMs, and soon after SWDEN* is driven because of the need to swap byte lanes for the addressed data bytes. But the local circuitry cannot, for some reason, allow the access, and LACK remains High. Therefore, CY7C960 maintains ROW active, and does not drive COL, CAS*, or DBE until LACK has been driven Low by the local circuitry. Once LACK has gone Low, the BLT commences.

3.8.9 DBE Signal Behavior

The Data Byte Enable signals are used to indicate which local data bytes are active for the current cycle. They do not necessarily reflect the VMEbus data byte lanes being used for the transfer. For example, if a VMEbus D16 transfer is selected, and the most significant

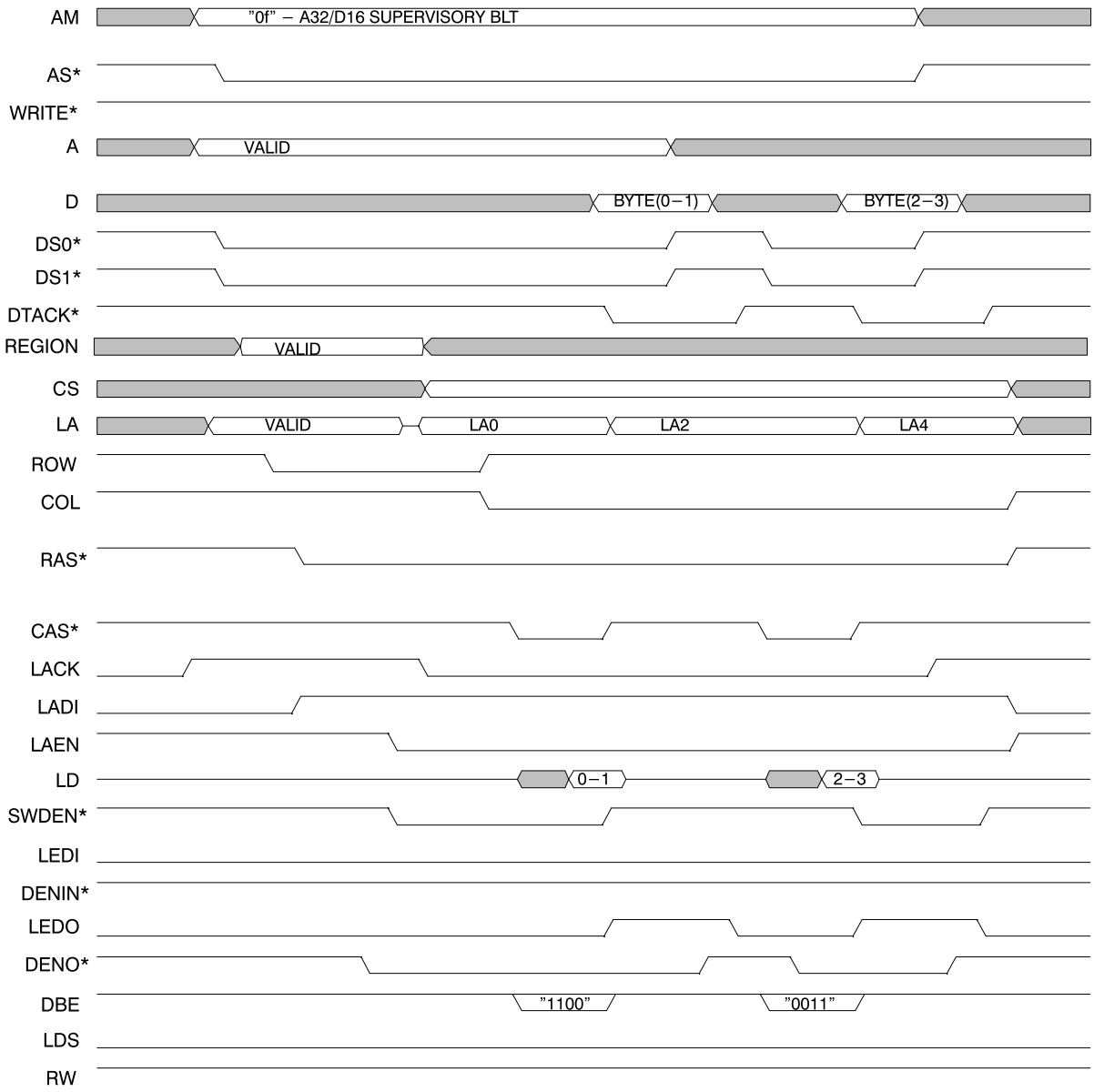

Figure 3–30. LACK in DRAM Cycles

two bytes, LD[31:16], are enabled onto the local bus by DBE[1:0], the VMEbus specification ensures that those two bytes are carried on D[15:0]. CY7C960 provides the SWDEN* signal for controlling a swap buffer if D8 or D16 transfers are required.

For DRAM cycles the timing of the DBE[3:0] signals is identical to CAS*. In some applications this means that the appropriate DBE pin can be connected to the CAS* input for one byte width of DRAM. For accesses to Regions where DRAM is not enabled, the DBE timing is taken from the programmed value for DBE Assert Time. See Chapter 3.9, I/O Control Description, for more details.

If DRAM refresh is enabled, then the DBE pins can be configured to provide the refresh burst if desired. If DBE Refresh is enabled during initialization, all four DBE pins carry the same refresh timing that is driven on the CAS* pin. If DBE refresh is disabled, then all four signals are not driven due to refresh.

3.8.10 Formal Signal Description

3.8.10.1 RAS*, CAS*, ROW, COL

RAS*, the DRAM Row Address Strobe, is an active Low signal that is used by the DRAM to latch the Row address internally. The falling edge of RAS* is timed with respect to the local address being driven by the CY7C964s so that there is sufficient set-up time prior to the falling edge for all commonly available DRAMs.

CAS*, the DRAM Column Address Strobe, is an active Low signal that is used by the DRAM to latch the column address internally. The falling edge of CAS* is timed with respect to the local address being driven by the CY7C964s so that there is sufficient set-up time prior to the falling edge for all commonly available DRAMs.

ROW, a signal provided by CY7C960 whose polarity is programmable, is intended to multiplex the row address signals to the address pins of the DRAM array prior to the falling edge of RAS*. ROW is set up 1 clock period before the falling edge of RAS*, and held 1 clock period beyond the falling edge of RAS* to guarantee that all common multiplexing circuitry has sufficient set-up and hold time.

COL, a signal provided by CY7C960 whose polarity is programmable, is intended to multiplex the column address signals to the address pins of the DRAM array prior to the falling edge of CAS*. COL is set up 1 clock period before the first falling edge on CAS*, and held active for the duration of the VMEbus transaction as appropriate.

Neither ROW nor COL become active for refresh bursts.

3.8.11 Programmable Features

3.8.11.1 Refresh Enable

A bit is set during initialization that enables refresh activity.

3.8.11.2 Cycle Timing

The following parameters are set during configuration: RAS* Precharge (min. 5, max 12 clocks); CAS* precharge (min. 1, max 8 clocks); CAS* assert (min. 3, max 10 clocks); RAS*/CAS* delay (min. 2, max 9 clocks)

With an 80-MHz clock, and 100-nsec RAS* access time DRAMs, an example would be RAS* precharge 7 clocks, CAS* precharge 1 clock, RAS*/CAS* delay 2 clocks, CAS* assert 3 clocks.

3.8.11.3 Refresh Period

CAS* before RAS* refresh cycles occur in bursts of 4. The timing is taken from the cycle timing just described. The time interval between bursts is programmable during configuration to be

$$(N \times 256) \times clockperiod$$

where N is a value between 1 and 255.

For example, if a DRAM was used with R rows requiring to be refreshed every t msec, then N would be found as follows

$$N = int\left(\frac{4}{R} \times \frac{t}{10^3} \times \frac{1}{256} \times \frac{1}{clockperiod}\right)$$

In the case of a 256 row device with a refresh period of 4 msec and a clock rate of 80 MHz, N turns out to be 19 (13hex). The period between bursts in this case would be seen to be about 61 μsec.

3.8.11.4 DBE Refresh

The DBE pins can be configured to provide the CAS* timing for refresh bursts. If this is not enabled, then the DBE pins do not toggle during refresh bursts.

3.8.11.5 DBE Polarity

The polarity of the DBE pins can be programmed as a group during initialization.

3.8.11.6 ROW, COL Polarity

The polarity of the ROW and COL pins can be programmed individually during initialization.