3.9
I/O Control Description

The CY7C960 has two basic modes of operation: DRAM mode and I/O mode. The user selects the mode during configuration. This section describes the I/O mode of operation.

In I/O mode the CY7C960 does not provide the timing signals required by DRAM, such as RAS*/CAS*. The pins that provide these signals in DRAM mode are therefore available for I/O functions in I/O mode, and are used as Chip Select Outputs.

The signals that form the Local I/O Mode Functionality are CS[5:0], LACK, and DBE[3:0].

Figure 3−31 shows the block diagram of the CY7C960 in I/O mode. It is, as may be expected, very similar to the block diagram of the DRAM/IO Mode (see Introduction). The DRAM control block is disabled, and hence does not appear in the figure, and the pins thus freed are reused as Chip Selects. One additional Region Input (REGION[3]) is provided in I/O mode, allowing 16 Regions to be individually configured.

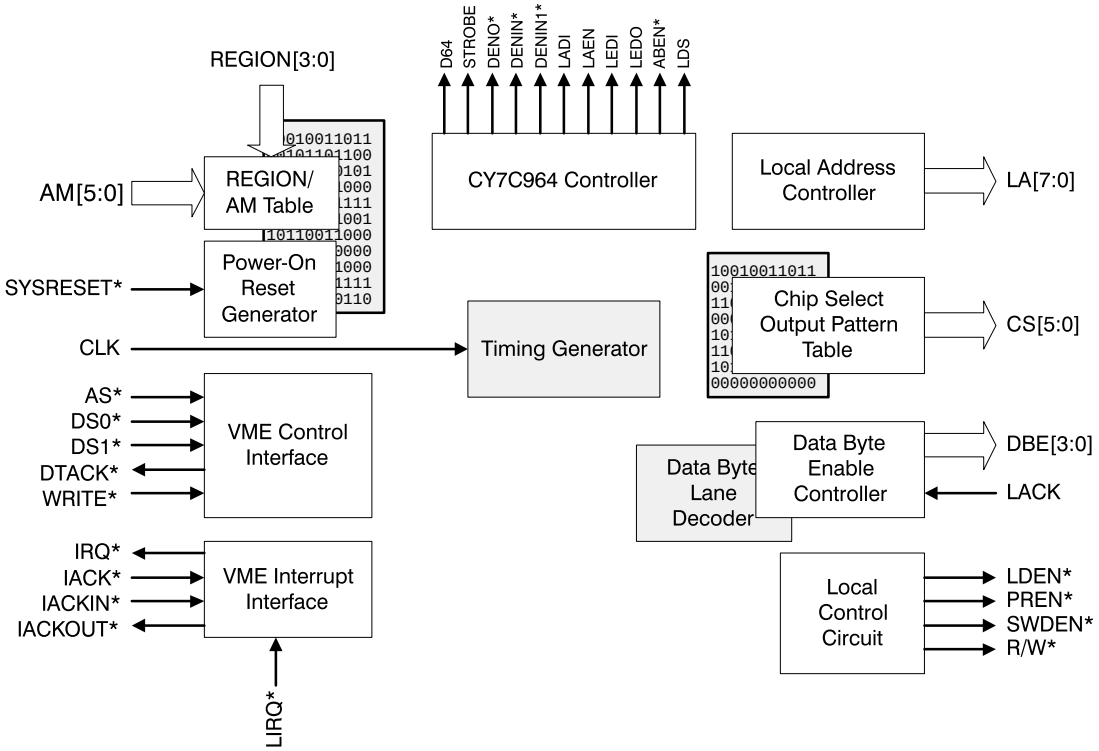

Figure 3−31. I/O Mode Block Diagram

3.9.1 Region Mapping

The CY7C960 introduces the concept of Region Mapping for I/O control. The CY7C960 provides up to 16 Regions when in I/O mode, selected by REGION[3:0]. The external Slave Address Map Decoder drives the REGION inputs in response to changes in the VMEbus address signals. When the CY7C960 detects the start of a valid transaction on the VMEbus (AM going Low) the REGION inputs are used to point into a table that contains entries for each possible VMEbus Transaction Type. The table entries are programmed during the initialization process, and are not adjustable after configuration is complete. If the VMEbus transaction is enabled in the table, then the CY7C960 proceeds. If the transaction is disabled then the CY7C960 takes no action and assumes that the VMEbus cycle is intended for another board. Further information is provided in the VMEbus Chapter.

This provides great flexibility in address mapping. For example, two separate VMEbus boards can occupy the same address in VMEbus space: one can react to 32/64 bit data transfers, the other can react to only 8/16 bit data transfers. Or one can selectively respond to block transfers, the other single cycles.

Each of the 16 Regions has a unique entry in the table, allowing for fine granularity in the Slave Address Map, and providing a wide range of options if the user cares to use them. If a simple Slave Address Map is desired, then the companion CY7C964 contains comparator circuitry which could be used, and the majority of the 16 possible regions could be selectively disabled.

Table 3–8 shows the use of the Region AM Code programming table. In this example, only transactions directed to Regions 0 through 4 could result in the CY7C960 driving DTACK*. Furthermore, only A64 supervisory block transfers, of any data width, are enabled in Region 0. The other Regions have different types of VME transaction enabled.

Table 3−8. Example of Region AM Code Enabling

REGION	A64	A40	A32	A24	A16	SUPER	NPRIV	PROG	DATA	BLT	LONG
0	✓					✓				✓	✓
1		✓					✓			✓	✓
2			✓			✓		✓			✓
3				✓			✓		✓		✓
4				✓	✓	✓					
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											

3.9.2 Chip Select Output Control

The six pins dedicated to I/O mode output, CS[5:0], can be configured during the initialization process in a flexible manner. Once the CY7C960 has detected that the VMEbus cycle is valid and enabled for the Region being addressed, then a pattern is driven from the Chip Select Outputs (CS[5:0]). The pattern is found in a table that contains entries for each possible Region, in a manner similar to the Region AM Code Enabling Table (*Table 3−8*). The entries are programmed during initialization and are not changeable after configuration is complete.

The user can select the polarity of each individual Chip Select Output to be High or Low true. This sets the output pattern when no VMEbus cycle has been decoded to drive the enabled Regions. In other words, this pattern is the relaxed state of the CS[5:0] pins. To effect a change in one or more of the 6 Chip Select pins, the appropriate bit or bits of the Chip Select Output Control Table (*Table 3−9*) entry (for the desired Region) are set. Any VMEbus transaction that is enabled for the Region it maps to will then cause that pattern to be driven from the CS[5:0] pins.

Table 3−9 provides an example of how the Chip Select Programming and Polarity may be set. The state of CS[5:0] after initialization becomes 000111, because the polarity field de-

termines the unselected state of the signals. Any transaction directed to Regions 8, or 12 through 15, will not result in a CS[5:0] change as no CS programming has been entered for those Regions. Regions 0 through 7 cause CS[2:0] patterned to be driven. Regions 9, 10, and 11 cause CS[5], CS[4], and CS[3] to change respectively.

Table 3−9. Example of Chip Select Output Control

REGION	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]
0						
1				✓	✓	✓
2				✓	✓	
3				✓		✓
4				✓		
5					✓	✓
6					✓	
7						✓
8						
9	✓					
10		✓				
11			✓			
12						
13						
14						
15						
Polarity	L	L	L	H	H	H

An access to Region 0 therefore would cause the pattern 000000 to be driven. Region 9 would cause 100111.

3.9.3 Chip Select Output Timing

3.9.3.1 Overview

When a valid VMEbus transaction is decoded that maps to a Region with a Chip Select Pattern enabled, the pattern is driven from the CS[5:0] pins after the VMEbus DSi* signal goes true. Then the appropriate DBE signals are driven. After either the self-timed delay or the LACK handshake, the VMEbus DTACK* is driven and the DBE pins are disabled. If the VMEbus transaction is a block transfer, the CS[5:0] pattern is maintained and the DBE pins

toggle interlocked with the VMEbus handshake mechanism. After the final transfer, signified by AS* going inactive, the CS[5:0] pins return to the relaxed state.

3.9.3.2 Read-Aheads

In VMEbus block read transactions, the CY7C960 optimises performance by performing read-ahead cycles whenever possible. Therefore, if the AS* signal is slow going inactive, an extra DBE cycle may occur. The data read locally is not passed to the VMEbus and the cycle completes as soon as the AS* signal goes inactive.

To guarantee that a read-ahead cycle will not occur, it is necessary to deassert AS* at the same time that DSi* is deasserted. This of course is a VMEbus master transaction, not under the control of the CY7C960.

3.9.3.3 Local Acknowledge Timing

The CY7C960 provides the option of handshaking local accesses, or having the access be self-timed. The LACK pin provides the handshake. The time period for the self-timed access is programmed during configuration to be a value between 3 and 18 clock periods. When a VMEbus access causes the local cycle to commence, Chip Select goes active followed by the appropriate DBE pins. The width of the DBE signal is controlled: after the expiration of the access time, if LACK is Low the cycle terminates. If LACK is High, the cycle is extended until LACK goes Low.

Therefore, if the user ties LACK Low, the width of the DBE pulse is determined only by the programmed value for the Region's CS Access Time field. Each Region can have a unique value for this field. The user may also choose to Handshake the cycles with LACK, in which case the minimum width is set by the Access time field, and the maximum time is determined by LACK.

Figure 3−32 provides an example of one of the most challenging VMEbus Transactions—the A40/MD32 Read-Modify-Write Cycle. Once the CY7C960 determines that the transaction is directed to a Region for which it is enabled, the address broadcast cycle is DTACKed and the Read cycle commences. The appropriate pattern is driven on the Chip Select signals. Two 16-bit local accesses are needed to construct the MD32 VMEbus transaction, and SWDEN* and DBE signals are driven appropriate to the address requested. Once the 32 bits of data are latched into the CY7C964s and enabled onto the VMEbus signals (A[15:1],

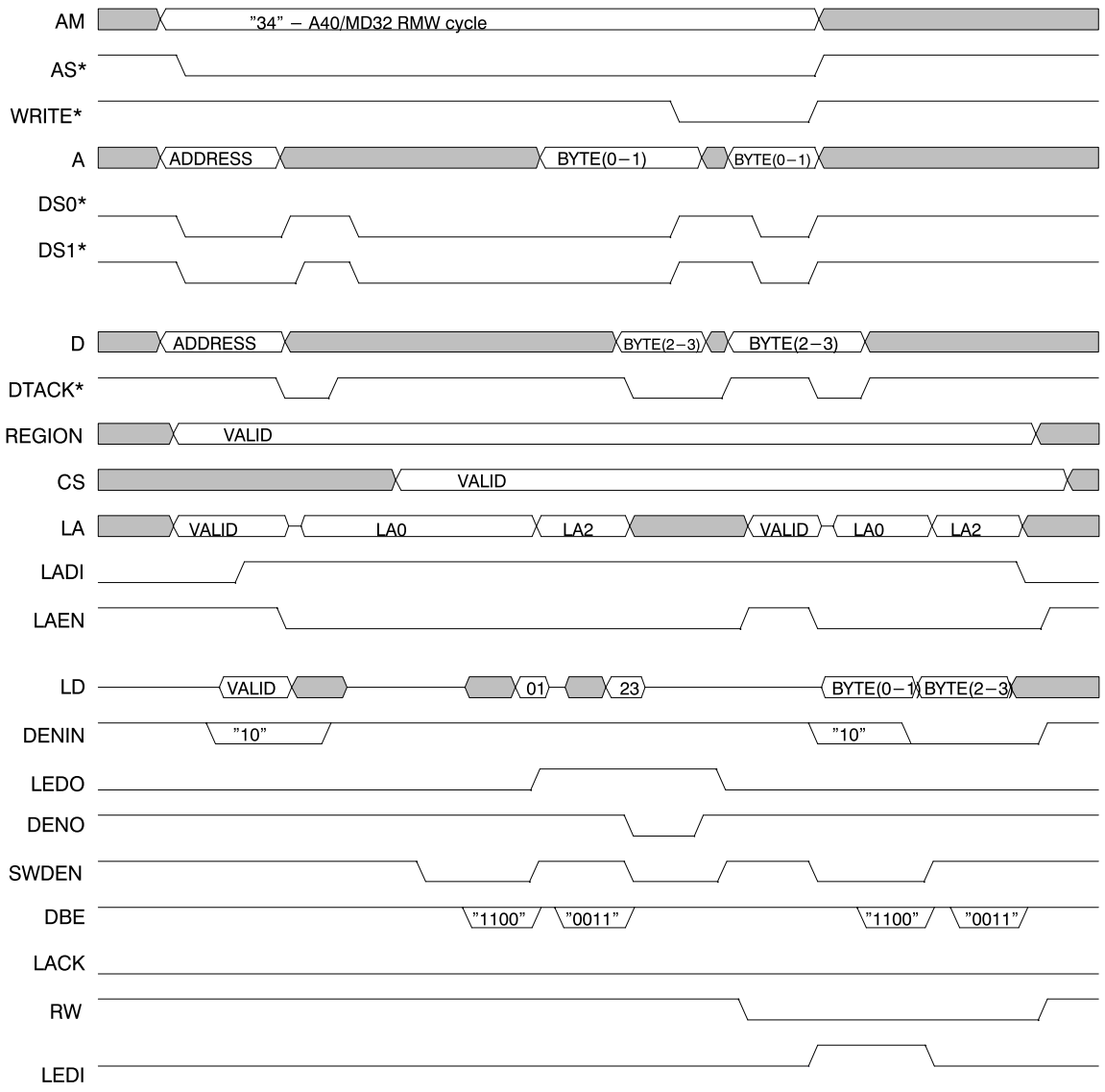

Figure 3–32. I/O Cycle Timing

LWORD*, and D[15:0]) the VMEbus DTACK* is driven. The WRITE* signal is toggled by the VMEbus master, signifying an RMW cycle. The CY7C960 responds to the subsequent DSi* assertion by latching the state of A[15:1], LWORD*, and D[15:0] in the CY7C964s, thus posting the data, and completing the VMEbus cycle by driving and releasing DTACK*. The local cycle continues by reasserting the previously-latched lower 24 bits of address on the local address bus and driving SWDEN* and DBE signals appropriately for the address to be written. Two local cycles occur to write the MD32 data.

Figure 3–33 shows an example of read-ahead operation. The transaction shown is an A32/D16 BLT, 2 transactions (4 bytes) long. In this example, DRAM is enabled for the Re-

gion being addressed so the DRAM control signals are shown in addition to the Chip Select signals. The two VMEbus Read Cycles are completed normally, and the local signals, SWDEN*, DBE, and Chip Selects are driven appropriately for the address being transferred. The 16-bit local data is driven on the correct VMEbus data signals (D[15:0]). After the second DTACK from the CY7C960, the VMEbus Master releases AS*, signifying the end of the block transfer. But meanwhile, the CY7C960 has provided another read sequence to the local circuitry. In this case, CAS* and DBE have been driven and the data has been presented by the local circuitry to the CY7C964 local data pins. When AS* is de-

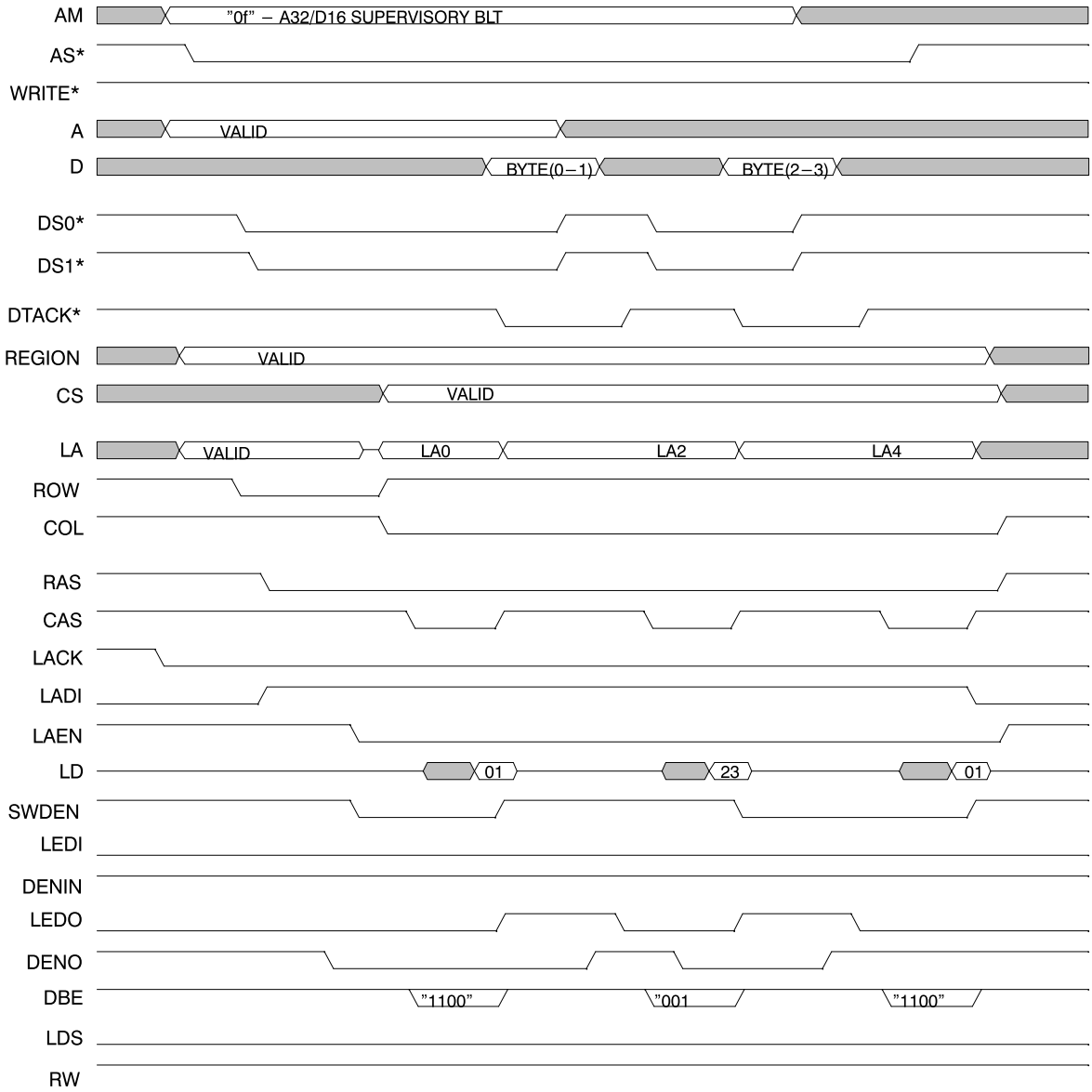

Figure 3–33. Example of Read-Ahead Timing

tected High, the CY7C960 simply drives all local controls inactive and terminates the local cycle with no ill effects.

3.9.4 Data Byte Enable Usage

Table 3−10 indicates which Data Byte Enable signals are active for all possible VMEbus Transactions. The polarity assumed for the DBE pins is LOW true.

Table 3−10. DBE Signal Truth Table

	DS1*	DS0*	LA1	LA0 (LWORD*)	DBE3	DBE2	DBE1	DBE0
Byte	0	1	0	1	1	1	1	0
	1	0	0	1	1	1	0	1
	0	1	1	1	1	0	1	1
	1	0	1	1	0	1	1	1
Word	0	0	0	1	1	1	0	0
	0	0	1	1	0	0	1	1
Longword	0	0	0	0	0	0	0	0
Unaligned	0	1	0	0	1	0	0	0
	1	0	0	0	0	0	0	1
	0	0	1	0	1	0	0	1

3.9.5 Using I/O In DRAM Mode

When the CY7C960 is configured for DRAM, three pins remain for use as Chip Select Outputs, CS[2:0]. When a transaction takes place that maps to a Region where DRAM is enabled the Chip Select output pattern for that Region is driven from CS[2:0]. The DBE pins are driven with timing appropriate for a DRAM access (CAS* timing parameters configured during initialization). When a transaction takes place that maps to a Region where DRAM is disabled, then the Chip Select pattern for that Region is driven from CS[2:0], and the DBE pins are driven with timing appropriate for an I/O access (DBE assert time configured during initialization).