# 5.1 Introduction to the VAC068A

## 5.1.1 Features Summary

When used with the VIC068A (VMEbus Interface Controller), the VAC068A (VMEbus Address Controller) forms a complete VMEbus master/slave interface solution. The VAC068A is intended for use solely with VIC068A. The following feature list is VAC068A specific but uses VIC068A implementations for items such as boundary crossing, dual-path, interprocessor communications facilities, and block transfers.

- Complete VMEbus and I/O DMA capability for 32-bit processors, including 42 programmable registers for configuration and control of:
  - — slave address decode
  - — UARTs
  - — programmable I/O signals
  - — local I/O
  - — interrupt source
- Provides complete local memory map decoding. Separate segments on local interface available for:
  - — DRAM
  - — VME Subsystem Bus (VSB)
  - — Shared Resource
  - — Local I/O
  - — EPROM
- Provides complete VMEbus memory map decoding. Separate segments are available for:
  - — two VMEbus slave decodes
  - — interprocessor communication facilities
- Supports block transfers over 256-byte boundaries:
  - — address counters for VMEbus A[31:8] and local LA[31:8]
  - — supports dual-path feature of the VIC068A

  - — supports implementation of the VSB interface
  - — includes local DMA capability
- Dual UARTs on chip:
  - — double buffered on transmit, quad-buffered on receive
  - — programmable baud rate from 300 to 9600 baud
- Miscellaneous:
  - — supports unaligned transfers
  - — programmable DSACKi* for local I/O
  - — programmable timer and interrupts
  - — programmable I/O signals (dual function)
  - — buffer control signals for direct connection to ’543s

## 5.1.2 General Description

The VAC068A is a programmable address decode controller and VMEbus DMA extension for the VIC068A. When used in conjunction with the VIC068A, the VAC068A maximizes performance of a master/slave VMEbus interface module. It also substantially reduces power consumption and board space when compared to discrete implementations. The VAC068A contains programmable registers that allow the user to easily define VMEbus address decoding. These are:

- A24 address space overlay register
- three programmable VMEbus boundary registers
- separate A16 address space with programmable D16 or D32 data size

The VAC068A reserves address space for local I/O resources, DRAM, and EPROM. Access to these address spaces forces the proper chip select signal on the VAC068A. The chip select outputs are CS*, IOSEL5−0*, DRAMCS*, and EPROMCS*. DRAM address space is hard coded to start at $0000 0000 to follow normal VMEbus address space conventions. Programmable address options also exist for the purpose of asserting VSB select (VSBSEL*) and shared resources chip select (SHRCS*).

The VAC068A contains address counters and control logic to allow for block transfer over 256-byte boundaries.

Additional features include 13 programmable input/output signals (PIO signals) that can be programmed for the following functions:

- 13 general-purpose I/O signals
- two serial I/O transmit and receive channels (A and B)
- three interrupt signals
- shared resource chip select
- I/O read and I/O write
- I/O selects 2−5 for slower 8-bit peripheral devices

Note: IOSEL0* and IOSEL1* have dedicated pins on the VAC068A.

The I/O selects have reserved address space and may use the local address bus or the IDbus. When the IDbus is used, programmable cycle end and DSACK control may be programmed in the corresponding DSACK control register.

Programmable DSACKi* control also exists for EPROM and shared resource selects. DSACKi*s may also be disabled if the user wishes to provide this function. There is also a programmable timer and interrupt mapping on either PIO7, PIO10, or PIO11 for the following interrupting functions:

- timer interrupt
- UART A and B interrupt
- mailbox interrupt
- PIO4, PIO7, PIO8, or PIO9

The VAC068A uses the VIC068A data direction (DDIR) and swapping signals (SWDEN*) for direction control and unaligned transfers.

The VAC068A connects directly to the local address bus LA[31:8] and the VMEbus address A[31:8] signals. It also connects to the local data bus through the IDbus ID[15:8]. VAC068A uses the IDbus to provide VMEbus data signal connection D[15:8], although external buffers and line drivers are required. The VIC068A directly drives the VMEbus data signals D[7:0], address signals A[7:1], and local address LA[7:1] and data signals D[7:0].

Both parts utilize Cypress's patented output drivers and were designed with high-performance standard cells using a 1-micron CMOS process. Thirteen ground and nine power pins are provided.