5.2

VAC068A Signal Descriptions

5.2.1 VMEbus Signals

A[31:8]

Drive: 64 mA (all)
Type: Three-state I/O

These are the VMEbus address signals.

AS*

Type: Input

This is the VMEbus address strobe signal. It responds to both VIC068A- and VMEbus-generated address strobes.

ID[15:8]

Drive: 16 mA
Type: Three-state I/O

These are the isolated data bus signals. They are used to interface local data [15:8] to the VMEbus D[15:8] in conjunction with transparent latching bidirectional I/O buffers. They also are used to interface with local 8-bit I/O peripherals via the Device Location and DSACKi* Control registers.

5.2.2 CPU/Local Interface Signals

LD[31:16]

Drive: 16 mA
Type: Three-state I/O

These are the local data bus signals. They are used to write or read the local data bus and for writing and reading the on-chip control registers.

Note: The IDbus connects to LD[15:8] and VIC068A connects to LD[7:0].

LA[31:8]

Drive: 16 mA
Type: Three-state I/O

These are the local address bus signals. They are used as inputs during a VMEbus master cycle and to access on-chip control registers. They are used for output during local or slave accesses.

PAS*

Type: Input

This is the local-processor address strobe. It indicates to the VAC068A that a valid address is present on the address bus. This signal is typically driven by either VIC068A or the local processor.

R/W*

Type: Input

This is the local read/ write signal. When High, this signal indicates that the current cycle is a read. When Low, the current cycle is a write. This signal is typically driven by either the VIC068A or the local processor.

RESET*

Type: Input

This is the reset for the VAC068A. It is used alone or in conjunction with WORD* to reset the VAC068A internal registers. There are two reset types that may be implemented, and both of them are discussed in the reset section.

WORD*

Drive: 16 mA
Type: Input/Three-state output

This signal is active under programmable control from the appropriate region attribute register and controls the length of the data field. When it is asserted, the data path is 16 bits wide. When deasserted, a 32-bit data path is set. It is also used as an input in conjunction with RESET* to set VAC068A registers. It is typically connected to the VIC068A as an output.

ASIZ1, ASIZ0

Drive: 16 mA
Type: Three-state output

These are the address size signals. They are used to specify the address size of an access. They are active under programmable control from the appropriate region attribute register. These signals are typically driven to VIC068A along with WORD* to determine address and data path size.

ASIZ0	*ASIZ1*	*Addressing Mode*
0	0	User-defined
0	1	A32
1	0	A16
1	1	A24

DSACK1/0*

Drive: 16 mA
Type: Three-state I/O (rescinding)

These are the data sizing acknowledge signals. They are generated for any of the VAC068A device select outputs except CS* and VSBSEL* accesses. DSACK0* or DSACK1* can be selectively disabled or enabled in the DSACK1* Control register.

FC2/0

Type: Inputs

These are the function code signals. They are used by the VAC068A to determine the local access type and are typically driven by the local processor or the VIC068A as shown in the following tables:

(Per 680X0 User's Guide)

FC2	*FC1*	*FC0*	*Cycle*
0	0	1	User Data Space
0	1	0	User Program Space
1	0	1	Supervisor Data Space
1	1	0	Supervisor Program Space
1	1	1	CPU Space

(Per section 1.2.2 of this Handbook)

FC2	*FC1*	*Cycle*
0	0	Slave Block Transfer
0	1	Local DMA
1	0	Slave Access
1	1	DRAM Refresh

MWB*

Drive: 16 mA
Type: Output

This is the module-wants-bus signal. It is asserted under programmable control of the appropriate region attribute register and indicates that a VMEbus access is occurring. This signal is typically connected to the VIC068A.

FCIACK*

Drive: 16 mA
Type: Output

This is the local interrupt acknowledge signal. It indicates that the current cycle is an interrupt acknowledge cycle. This signal is typically connected to the VIC068A. It is asserted during local VAC068A interrupt cycles, or when HIACKEN is enabled in the PIO Direction register or when IOSEL5* address space is accessed when enabled in the PIO Function register.

DRAMCS*

Drive: 16 mA
Type: Output

This is the DRAM chip select signal. It is asserted when the local address maps into region 0 as defined by the DRAM Upper Limit Address register. It is also asserted when redirection is enabled in the VAC068A Decode Control register.

EPROMCS*

Drive: 16 mA
Type: Output

This is the EPROM chip select signal. It is asserted after a global reset, during a local access to EPROM address space, and during redirection of SLSEL1* on the local bus via the VAC068A Decode Control register.

FPUCS*

Drive: 16 mA
Type: Output

This is the floating-point-unit chip select signal. It is asserted when a floating-point coprocessor access is occurring. This is decoded from the processor function codes or under programmable control in the PIO Function register to be asserted in the IOSEL4* address range.

VSBSEL*

Drive: 16 mA
Type: Output

This is the VSB (VME Subsystem Bus) select signal. It is used to identify accesses to a daughterboard or VSB. It is asserted when enabled from the appropriate region attribute register.

REFGT*

Drive: 16 mA
Type: Output

This is the refresh grant signal. It is asserted during a DRAM refresh cycle and is typically decoded from the VIC068A function codes (FC1 and FC2).

LBR*

Type: Input

This is the VIC068A local bus request signal. It is used to signal the VAC068A when the VIC068A requests the local bus. It is typically connected to the VIC068A LBR* signal.

CS*

Drive: 16 mA
Type: Output

This is the VIC068A chip select signal. It is asserted when the fixed address of the VIC068A is present on the local address bus. This signal is typically connected to the VIC068A chip select signal (CS*).

BLT*

Type: Input

This is the block transfer signal. It is used to determine when a block transfer is in progress and to increment internal address counters during a boundary crossing. This signal is typically connected to the VIC068A.

CACHINH*

Drive: 16 mA
Type: Open Collector Output

This is the cache inhibit signal. It is asserted when enabled in either the Region Attribute registers or in the A24 Space Base Address register. It is also asserted on access to the DRAM Mailbox and VMEbus A16 address space (Region 6). It may be connected to the CDIS signal on 680X0-type processors.

LDMACK*

Drive: 16 mA
Type: Output

This is the local DMA activity signal. It is asserted when there is DMA activity mapped into a particular region. It is typically decoded from the VIC068A function codes (FC1 and FC2).

CPUCLK

Type: Input

This is the CPU clock signal. It is typically connected to the system CPU clock. Maximum frequency is 50 MHz.

SLSEL0*

Drive: 16 mA
Type: Output

This is the slave select 0 signal. It is asserted when enabled by a comparison of its base address register and the address on the VMEbus. It indicates to the VIC068A that a slave operation is pending.

SLSEL1*

Drive: 16 mA
Type: Output

This is the slave select 1 signal. It is asserted when enabled by a comparison of its base address register and the address on the VMEbus. It indicates to the VIC068A that a slave operation is pending.

ICFSEL*

Drive: 16 mA
Type: Output

This is the interprocessor communications signal. It is asserted under programmable control of a comparison of its base address register and the address on the VMEbus. It indicates a VIC068A interprocessor communication access.

IOSEL1/0*

Drive: 16 mA
Type: Output

These are 2 of the 6 I/O select signals. They are asserted when the local bus address matches their fixed memory location. They are also used in conjunction with the IDbus when programmed in the PIO Function register.

5.2.3 Parallel I/O-Shared Function Signals

The functions of these signals are programmed in the PIO Function register. When the corresponding bit is set in this register, the signal is the shared function. When the corresponding bit is cleared, the signals operate in the general-purpose parallel I/O mode (PIO).

PIO0−TXDA

Drive: 16 mA
Type: Input/Three-state output

The PIO0−TXDA signal is programmed to serve either as General-Purpose I/O pin bit 0, or as an output for the UART Channel-A Transmit signal.

PIO1−RXDA

Drive: 16 mA
Type: Input/Three-state output

The PIO1−RXDA signal is programmed to serve as either General-Purpose I/O pin bit 1, or as an input for the UART Channel-A Receiver signal.

PIO2−TXDB

Drive: 16 mA
Type: Input/Three-state output

The PIO2−TXDB signal is programmed to serve as either General-Purpose I/O pin bit 2, or as an output for the UART Channel-B Transmit signal.

PIO3−RXDB

Drive: 16 mA
Type: Input/Three-state output

The PIO3−RXDB signal is programmed to serve as either General-Purpose I/O pin bit 3, or as an input for the UART Channel-B Receiver signal.

PIO4−IORD*

Drive: 16 mA
Type: Input/Three-state output

The PIO4−IORD* signal is programmed to serve as either General-Purpose I/O pin bit 4, or as an output for the read enable signal (local I/O accesses).

PIO5−IOWR*

Drive: 16 mA
Type: Input/Three-state output

The PIO5−IOWR* signal is programmed to serve as either General-Purpose I/O pin bit 5, or as an output for the write enable signal (local I/O accesses).

PIO6−IOSEL3*

Drive: 16 mA
Type: Input/Three-state output

The PIO6−IOSEL3* signal is programmed to serve as either General-Purpose I/O pin bit 6, or as an output for the IOSEL3* enable signal (local fixed-map I/O select).

PIO7−Interrupt Request

Drive: 16 mA
Type: Input/Three-state output

The PIO7−Interrupt Request signal is used as either General-Purpose I/O pin bit 7, or as an output for interrupt requests on one of PIO 7, 10, or 11 (programmed in the Interrupt Control register).

PIO8−IOSEL4*

Drive: 16 mA
Type: Input/Three-state output

The PIO8−IOSEL4* signal is programmed to serve as either General-Purpose I/O pin bit 8, or as an output for the IOSEL4* enable signal (local fixed-map I/O select). IOSEL4* accesses also assert FPUCS* when so programmed in the PIO Function register.

PIO9−IOSEL5*

Drive: 16 mA
Type: Input/Three-state output

The PIO9−IOSEL5* signal is programmed to serve as either General-Purpose I/O pin bit 9, or as an output for the IOSEL5* enable signal (local fixed-map I/O select). IOSEL5* accesses also assert FCIACK* when so programmed in the PIO Function register.

PIO10−Interrupt Request

Drive: 16 mA
Type: Input/Three-state output

The PIO10−Interrupt Request signal is used as either General-Purpose I/O pin bit 10, or as a programmed interrupt request as programmed in the Interrupt Control register.

PIO11−Interrupt Request

Drive: 16 mA
Type: Input/Three-state output

The PIO11−Interrupt Request signal is used as either General-Purpose I/O pin bit 11, or as an output for interrupt requests as programmed in the Interrupt Control register.

PIO12−SHRCS*

Drive: 16 mA
Type: Input/Three-state output

The PIO12−SHRCS* signal is programmed to serve as either General-Purpose I/O pin bit 12, or as an output for shared resource chip select.

PIO13−IOSEL2*

Drive: 16 mA
Type: Input/Three-state output

The PIO13−IOSEL2* signal is programmed to serve as either General-Purpose I/O pin bit 13, or as an output for the IOSEL2* enable signal (local fixed-map I/O select).

5.2.4 Data Flow Control Signals

These signals are inputs to VAC068A and are connected to outputs from VIC068A.

SWDEN*

Type: Input

This is the swap data enable signal. It is used in conjunction with DDIR* to swap data to or from the Isolated Data bus signals ID[15:8] to the Local Data LD[15:8] bus. This signal is typically connected to the VIC068A.

DDIR

Type: Input

This is the data direction signal. It is typically connected to the VIC068A.

LADO

Type: Input

This is the latch address out signal. It is used to latch the local address out to the VMEbus. It is typically connected to the VIC068A. LADO is also used to increment internal address counters during a VMEbus boundary crossing.

LADI

Type: Input

This is the latch address in signal. It is used to latch the local address from the VMEbus.

LAEN

Type: Input

This is the local address bus enable signal. It is used by the VAC068A to indicate that the VIC068A has bus mastership of the local bus.

ABEN*

Type: Input

This is the VMEbus address enable signal. It is used to indicate that the VIC068A is driving the VMEbus address bus.

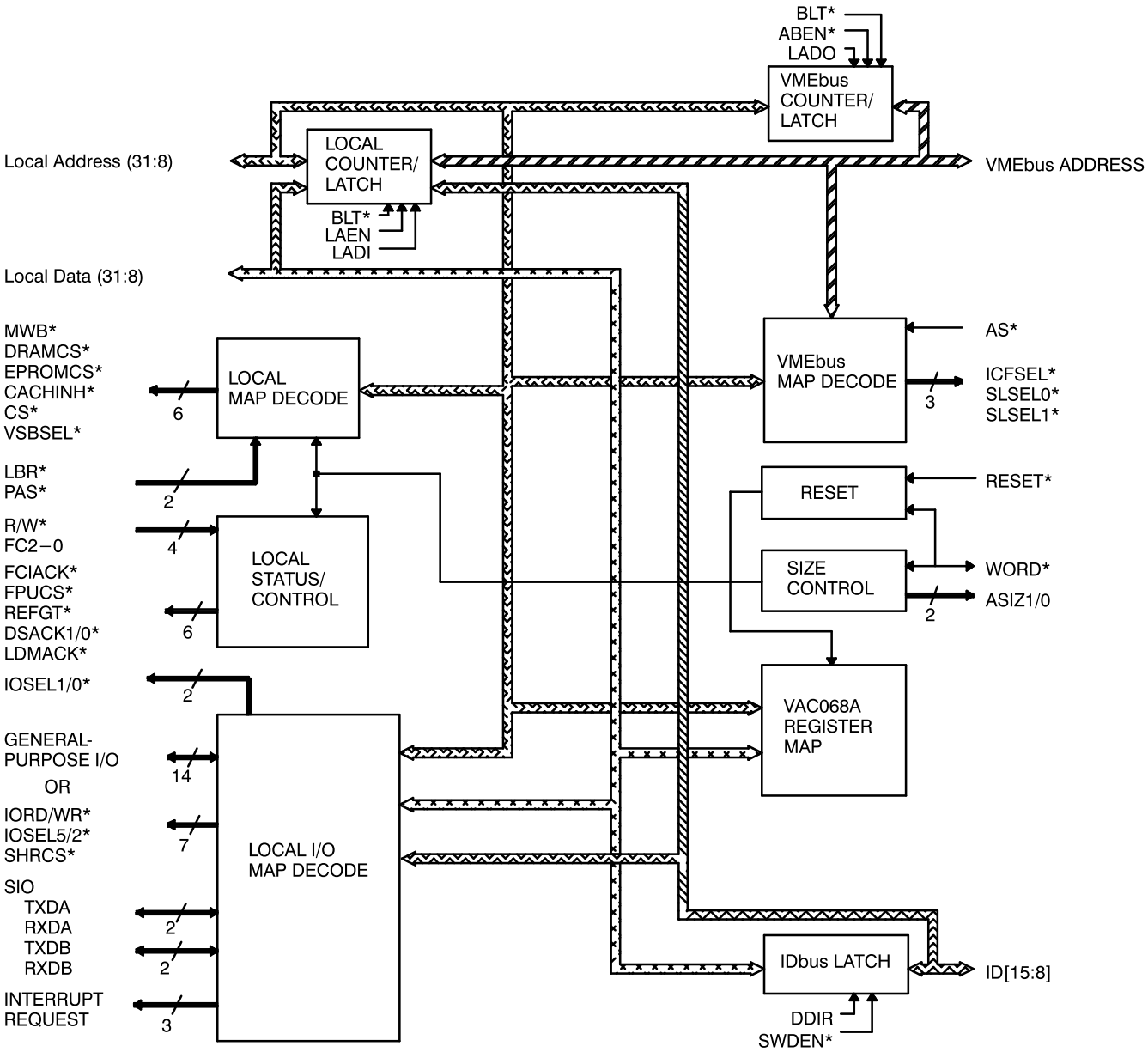

Figure 5−1. VAC068A Block Diagram