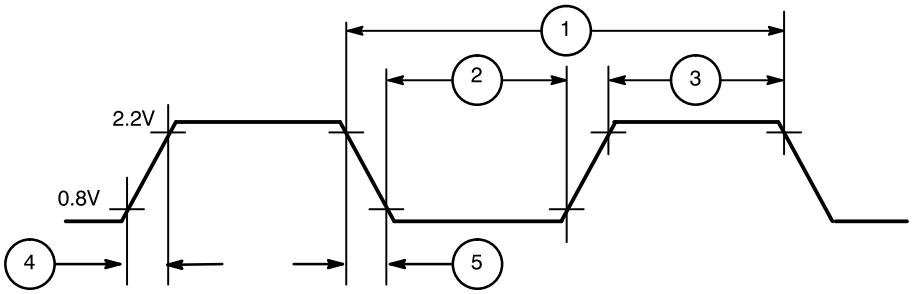
1.13

VIC068A AC Performance Specifications

Clock Input

Num.	Characteristic	Min.	Max.
	Frequency of Operation (MHz)	1	64
1	Cycle Time (ns)	15.6	1000
2, 3	Clock Pulse Width (Measured from 1.5V to 1.5V)	Note 1	Note 1
4, 5	Rise and Fall Time (ns)	—	5



Note:

1. A 60/40 to 40/60 duty cycle must be maintained.

AC Specifications[2]

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
ARBITRATION								
A1	BRi*[0] to BBSY*[H]	3, 4	2½T+5	3T+25	2½T+4	3T+26	2½T+4	3T+31½
A2	BRi*[0] to BBSY*[L]	4, 5	3T+8	3½T+28	3T+7	3½T+34	3T+7	3½T+35
A3	BRi*[0] to BGiOUT*[L]	4, 5	3T+4	4T+25	3T+4	4T+26	3T+3	4T+28
A4	BRi*[0] to BCLR*[L]	4	2	16	2	16	2	19
A5	BGiIN*[0] to BGiOUT*[L]	4	2	18	2	18	2	20
A6	BGiIN*[0] to BBSY*[L]	6	4	23	4	24	3	25
A7	BGiIN*[0] to BRi*[H]	4, 6	5	3T+26	4	3T+27	4	3T+31
A8	BGiIN*[1] to BGiOUT*[H]	4	3	20	2	21	2	23

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
A9	BBSY*[0] to BGiOUT*[H]	4, 5	4	21	3	22	3	24
A10	BBSY*[1] to BGiOUT*[L]	4	3T+5	4T+25	3T+4	4T+26	3T+3	4T+29
A11	BBSY*[1] to BCLR*[H]	4	1T+4	2T+24	1T+4	2T+25	1T+3	2T+27
MASTER ACCESSES								
B1	BGiIN*[0] to DENO*[L]	4, 6, 7	8	3T+36	7	3T+37	6	3T+42
B2	BGiIN*[0] to LADO[H]	4, 6	14	3T+59	13	3T+61	12	3T+67
B3	BGiIN*[0] to AS*[L]	4, 6	3T+5	6T+28	3T+5	6T+29	3T+4	6T+31
B4	BGiIN*[0] to A[7:1] Valid	4, 6	6	3T+31	6	3T+32	5	3T+37
B5	BGiIN*[0] to LWORD*[H/L]	4, 6	6	3T+31	6	3T+32	5	3T+37
B6	BGiIN*[0] to WRITE*[H/L]	4, 6	6	3T+31	6	3T+32	5	3T+37
B7	BGiIN*[0] to ABEN*[L]	4, 6	7	3T+34	6	3T+36	6	3T+38
B8	PAS*[0] & MWB*[0] to BRi*[L]	4	4	22	3	22	3	24
B9	PAS*[0] & MWB*[0] to ISOBE*[L]	4	4	22	3	23	3	25
B10	PAS*[0] & MWB*[0] to LADO[H]	4	15	60	13	62	12	68
B11	PAS*[0] & MWB*[0] to BBSY*[L]	4, 8	7	32	5	33	5	36
B12	PAS*[0] & MWB*[0] to ABEN*[L]	4, 8	1½T+8	2½T+36	1½T+7	2½T+37	1½T+6	2½T+41
B13	PAS*[0] & MWB*[0] to A[7:1]	4, 8	1½T+7	2½T+36	1½T+6	2½T+37	1½T+5	2½T+41
B14	PAS*[0] & MWB*[0] to LWORD*[H/L]	4, 8	1½T+7	2½T+36	1½T+6	2½T+37	1½T+5	2½T+41
B15	PAS*[0] & MWB*[0] to WRITE*[H/L]	4, 8	1½T+7	2½T+36	1½T+6	2½T+37	1½T+5	2½T+41
B16	PAS*[0] & MWB*[0] & DS*[0] to DS1/0*[L]	4, 8	4½T+10	5½T+46	4½T+9	5½T+47	4½T+9	5½T+57
B17	PAS*[0] & MWB*[0] to SWDEN*[L]	4	1½T+7	2½T+36		12	3	14
B18	PAS*[0] & MWB*[0] to DENIN*[L]	4, 9	3	20	3	20	2	22
B19	PAS*[0] & MWB*[0] to DENIN1*[L]	4, 9	3	20	3	21	3	23
B20	PAS*[0] & MWB*[0] & DS*[0] to AS*[L]	4, 8	4½T+6	5½T+28	4½T+5	5½T+29	4½T+5	5½T+32
B21	R/W*[0] to DDIR[H]	4, 7	4	22	3	23	2	25
B22	R/W*[1] to DDIR[L]	4, 7	2	14	1	14	1	15
B23	D[7:0] to LD[7:0] Valid	4, 9	3	18	2	18	2	22
B24	DTACK*[0] to LEDI[H]	4, 9	3T+6	4T+28	3T+4	4T+29	3T+4	4T+32

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
B25	DTACK*[0] to DSACKi*[L]	4	4	30	3	31	3	36
B26	PAS*[1] & DS*[1] to DSACKi*[H]	4	2	19	2	20	2	27
B27	PAS*[1] to AS*[H]	4	6	30	5	31	5	41
B28	DS*[1] to ISOBE*[H]	4	4	23	3	24	3	26
B29	DS*[1] to SWDEN*[H]	4	4	10	3	10	2	13
B30	DS*[1] to DENIN1*[H]	4, 9	3	19	3	20	2	22
B31	DS*[1] to DENIN*[H]	4, 9	3	19	3	20	2	22
B32	DS*[1] to LD[7:0] Invalid	4, 9	3	20	2	22	2	28
B33	DS*[1] to LD[7:0] Hi-Z	4, 9	3	20	2	22	2	28
B34	DS*[0] to DSACKi*[L]	4, 10	6	T+30	5	T+32	5	T+35
B35	DS*[0] to LADO[H]	4, 10	8	38	7	39	7	43
B36	DS*[0] to LEDO[H]	4, 10	4	T+16	3	T+18	3	T+20
LOCAL BUS TIMING (VIC068A AS LOCAL BUS MASTER)								
C1	LBG*[0] to PAS*[L]	4	5T+6	6T+31	5T+5	6T+33	5T+5	6T+44
C2	LBG*[0] to LA[7:0] Valid	4	3T+8	4T+36	3T+7	4T+37	3T+6	4T+46
C3	LBG*[0] to SIZ[1:0] Valid	4	1T+3	2T+20	1T+3	2T+21	1T+2	2T+28
C4	LBG*[0] to FC[2:1] Valid	4	1T+3	2T+20	1T+3	2T+21	1T+2	2T+27
C5	LBG*[0] to LD[7:0] Driven	7	3T+8	4T+38	3T+7	4T+39	3T+7	4T+48
C6	LBG*[0] to LAEN[H]	4	3T+10	4T+43	3T+9	4T+44	3T+8	4T+48
C7	LBG*[0] to ISOBE*[L]	4	3T+8	4T+37	3T+7	4T+39	3T+7	4T+42
C8	LBG*[0] to SWDEN*[L]	4	3T+9	4T+39	3T+8	4T+41	3T+7	4T+45
C9	LBG*[0] to DDIR[H]	4, 7	3T+8	4T+37	3T+7	4T+39	3T+7	4T+42
C10	LBG*[0] to DENIN1*[L]	4, 7	3T+7	4T+36	3T+6	4T+38	3T+6	4T+42
C11	LBG*[0] to DENIN*[L]	4, 7	3T+7	4T+32	3T+6	4T+35	3T+5	4T+38
C12	LBG*[0] & DS1/0*[0] & WRITE*[0] to R/W*[L]	4, 7	3T+8	4T+38	3T+7	4T+40	3T+7	4T+47
C13	LBG*[0] & DS1/0*[0] to DS*[L]	4	5T+8	6T+39	5T+7	6T+42	5T+7	6T+56
C14	PAS*[0] to DS*[L]	4, 11	0	12	0	15	0	15
C15	LBR*[H] to LBG*[1]	4, 12		T		T		T
SLAVE ACCESSES								
D1	SLSELi*[0] & AS*[0] to LBR*[L]	4	7	35	6	36	6	40
D2	SLSELi*[0] & AS*[0] & DS1/0*[1] to LADI[H]	4	5	25	4	26	4	29
D3	LD[7:0] to D[7:0]	4, 9	2	16	2	16	2	18
D4	DSACKI*[0] to LEDO[H]	4, 9	SAT+8	SAT+½T +35	SAT+7	SAT+½T +36	SAT+6	SAT+½T +39

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
D5	DSACKi*[0] to DTACK*[L]	4	SAT+10	SAT+½T +45	SAT+9	SAT+½T +47	SAT+9	SAT+½T +53
D6	DS1/0*[0] to DTACK*[L]	4, 13	2T+5	3½T+28	2T+5	3½T+29	2T+4	3½T+33
D7	DS1/0*[0] to LEDI[H]	4, 13	9	41	8	43	8	47
D8	AS*[1] to LA[7:0], R/W* Invalid	4	5	38	4	42	4	55
D9	AS*[1] to LA[7:0], R/W* High-Z	4	5	38	4	42	4	55
D10	AS*[1] to FC2/1, Invalid	4	10	42	8	44	8	56
D11	AS*[1] & DSACKi*[1] to FC2/1, High-Z	4	10	42	8	44	8	56
D12	AS*[1] to SIZ1/0, Invalid	4	7	32	6	34	6	37
D13	AS*[1] & DSACKi*[1] to SIZ1/0, High-Z	4	3	1T+17	2	1T+19	2	1T+24
D14	AS*[1] to ISOBE*[H]	4	6	30	5	31	5	34
D15	AS*[1] to SWDEN*[H]	4	4	24	4	25	3	27
D16	AS*[1] to DENIN1*[H]	4, 7	5	27	4	28	4	30
D17	AS*[1] to DENIN*[H]	4, 7	5	27	4	28	4	30
D18	AS*[1] & DSACKi*[1] to LBR*[H]	4	5	26	4	27	4	30
D19	AS*[1] to LAEN[L]	4	9	40	8	43	7	56
D20	DS*1/0[1] to LD[7:0] Invalid	4, 7	2	27	2	30	2	39
D21	DS*1/0[1] to LD[7:0] High-Z	4, 7	2	27	2	30	2	39
D22	DSACKi*[0] to PAS*[H]	4	SAT+10	SAT+½T +44	SAT+9	SAT+½T +46	SAT+8	SAT+½T +56
D23	DSACKi*[0] to DS*[H]	4	SAT+9	SAT+½T +40	SAT+8	SAT+½T +41	SAT+7	SAT+½T +48
D24	DSi*[1] to DTACK*[H]	4	3	27	3	28	3	35
INTERRUPT								
E1	IACKIN*[0] to IACKOUT*[L]	4	2	16	2	17	2	18
E2	IACKIN*[1] to IACKOUT*[H]	4	3	18	2	19	2	20
E3	FCIACK*[0] & PAS*[0] to BRi*[L]	4	5T+9	6T+41	5T+8	6T+42	5T+7	6T+48
E4	FCIACK*[0] & PAS*[0] to IACK*[L]	4, 8	7½T+7	8½T+34	7½T+6	8½T+35	7½T+6	8½T+39
E5	FCIACK*[0] & PAS*[0] to LD[7:0] Driven	4, 14	5T+12	6T+50	5T+10	6T+52	5T+10	6T+57
E6	FCIACK*[0] & PAS*[0] to LD[7:0] valid	4, 15	9T+5	10T+29	9T+5	10T+33	9T+4	10T+37

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
E7	FCIACK*[0] & PAS*[0] to LIACK0*[L]	4, 16	5T+7	6T+32	5T+6	6T+33	5T+5	6T+36
E8	IRQi*[0] to IPL	4	5	33	5	34	4	37
E9	BGiIN*[0] to BBSY*[L]	4	7	32	5	33	5	36
E10	BGiIN*[0] to AS*[L]	4	3T+5	4T+27	3T+4	4T+28	3T+4	4T+31
E11	BGiIN*[0] to DS1/0*[L]	4	3T+10	4T+45	3T+9	4T+46	3T+8	4T+55
E12	BGiIN*[0] to IACK*[L]	4, 15	39	7	40	7	44	
E13	PAS*[0] to ISOBE*[L]	4	5T+9	6T+39	5T+7	6T+40	5T+7	6T+44
E14	PAS*[0] to SWDEN*[L]	4	5T+8	6T+37	5T+7	6T+38	5T+6	6T+42
E15	IPLi to IPLi	4, 11		10		12		12
MASTER BLOCK TRANSFER WITH LOCAL DMA (INITIATION CYCLE)								
F1	MWB*[0] & PAS*[0] & DS*[0] to BRi*[L]	4	T+7	2T+32	T+6	2T+33	T+5	2T+38
F2	BGiIN*[0] to LBR*[L]	4	4T+10	5T+42	4T+8	5T+44	4T+8	5T+50
F3	MWB*[0] & PAS*[0] & DS*[0] to LBR*[L]	4, 8	5T+10	6T+42	5T+8	6T+44	5T+8	6T+50
F4	MWB*[0] & PAS*[0] & DS*[0] to LADO[H]	4	T+7	2T+35	T+6	2T+36	T+6	2T+39
F5	MWB*[0] & PAS*[0] & DS*[0] to BLT*[L]	4	T+6	2T+28	T+5	2T+29	T+4	2T+37
MASTER BLOCK TRANSFER WITH LOCAL DMA (WRITE)								
** First cycle **								
G1	DSACKi*[0] and DS*[0] to DS*[H]	4	MBAT0+9	MBAT0+½T +41	MBAT0+8	MBAT0+½T +43	MBAT0+7	MBAT0+½T +52
G2	DSACKi*[0] and DS*[L] to LEDO[H]	4	MBAT0+8	MBAT0+½T +36	MBAT0+7	MBAT0+½T +37	MBAT0+6	MBAT0+½T +40
G3	DSACKi*[0] and DS*[L] to LA[7:0] valid	4	MBAT0+T +11	MBAT0+ 1½T+32	MBAT0+T +9	MBAT0+ 1½T+36	MBAT0+T +9	MBAT0+ 1½T+40
G4	DSACKi*[0] and DS*[L] to DSi*[L]		MBAT0+ 3T+6	MBAT0+ 3½T+37	MBAT0+ 3T+5	MBAT0+ 3½T+39	MBAT0+ 3T+5	MBAT0+ 3½T+42
G5	DTACK*[0] to LEDO[L]	4	7	32	6	33	6	38
G6	DTACK*[0] to DSi*[H]		10	49	9	51	9	56
G7	DTACK*[0] to A[7:0] Valid	4	11	46	10	48	9	64
G8	DS*[H] to DS*[L]	4	DST+1½T −13	DST+1½T −6	DST+1½T −14	DST−1½T −5	DST+1½T −15	DST+1½T −4
** Second and subsequent cycles **								
G9	DSACKi*[0] and DS*[L] to DS*[H]	4	MBAT1+9	MBAT1+½T +41	MBAT1+8	MBAT1+½T +43	MBAT1+7	MBAT1+½T +52
G10	DSACKi*[0] and DS*[L] to LEDO[H]	4	MBAT1+8	MBAT1+½T +36	MBAT1+7	MBAT1+½T +37	MBAT1+6	MBAT1+½T +40
G11	DSACKi*[0] and DS*[L] to LA[7:0] Valid	4	MBAT1+T +11	MBAT1+ 1½T+32	MBAT1+T +9	MBAT1+ 1½T+36	MBAT1+T +9	MBAT1+ 1½T+40

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
G12	DSACKi*[0] and DS*[L] to DSi*[L]	4	MBAT1+ 3T+6	MBAT1+ 3½T+29	MBAT1+ 3T+5	MBAT1+ 3½T+30	MBAT1+ 3T+5	MBAT1+ 3½T+38
G13	DTACK*[0] to LEDO[L]	4	7	32	6	33	6	38
G14	DTACK*[0] to DSi*[H]	4	10	45	9	46	9	59
G15	DTACK*[0] to A[7:0] Valid	4	11	46	10	48	9	64
G16	DTACK*[0] to DS*[H]	4,17	T + 15	1½T + 45	1½T + 14	1½T + 46	T + 13	1½T + 47
G17	LEDO[L] to LEDO[H]	4,17	T + 11	1½T + 25	1½T + 10	1½T + 26	T + 9	1½T + 27
MASTER BLOCK TRANSFER WITH LOCAL DMA (READ)								
** First Cycle **								
H1	DTACK*[0] to LEDI[H]		2T+6	3T+23	2T+4	3T+25	2T+4	3T+27
H2	DTACK*[0] to DSi*[H]		2T+9	3T+28	2T+8	3T+30	2T+7	3T+32
H3	DTACK*[0] to A[7:0] Valid	4	1½T+10	2½T+44	1½T+9	2½T+45	1½T+8	2½T+53
H4	DTACK*[0] to DS*[L]	4	1½T+8	2½T+38	1½T+7	2½T+40	1½T+7	2½T+47
H5	DSACKi*[0] and DS*[L] to DS*[H]		MBAT0+9	MBAT0+½T +38	MBAT0+8	MBAT0+½T +40	MBAT0+7	MBAT0+½T +45
H6	DSACKi*[0] and DS*[L] to LEDI[L]		MBAT0+9	MBAT0+½T +48	MBAT0+8	MBAT0+½T +50	MBAT0+7	MBAT0+½T +55
H7	DSACKi*[0] and DS*[L] to LA[7:0] Valid	4	MBAT0+T +11	MBAT0+ 1½T+30	MBAT0+T +9	MBAT0+ 1½T+32	MBAT0+T +9	MBAT0+ 1½T+35
H8	DSACKi*[0] and DS*[L] to DSi*[L]	4	MBAT0+11	MBAT0+½T +74	MBAT0+10	MBAT0+½T +76	MBAT0+10	MBAT0+½T +83
** Second and subsequent cycles **								
H9	DTACK*[0] to LEDI[H]	4	2T+6	3T+23	2T+4	3T+25	2T+4	3T+27
H10	DTACK*[0] to DSi*[H]	4	2T+9	3T+28	2T+8	3T+30	2T+7	3T+32
H11	DTACK*[0] to A[7:0] Valid	4	10	44	9	45	8	53
H12	DTACK*[0] to DS*[L]	4	8	38	7	40	7	47
H13	DSACKi*[0] and DS*[0] to DS*[H]	4	MBAT1+9	MBAT1+½T +36	MBAT1+8	MBAT1+½T +38	MBAT1+7	MBAT1+½T +45
H14	DSACKi*[0] and DS*[0] to LEDI[L]	4	MBAT1+9	MBAT1+½T +44	MBAT1+8	MBAT1+½T +46	MBAT1+7	MBAT1+½T +55
H15	DSACKi*[0] and DS*[0] to LA[7:0] Valid	4	MBAT1+T +11	MBAT1+ 1½T+31	MBAT1+T +9	MBAT1+ 1½T+33	MBAT1+T +9	MBAT1+ 1½T+35
H16	DSACKi*[0] and DS*[0] to DSi*[L]	4	MBAT1+11	MBAT1+½T +72	MBAT1+10	MBAT1+½T +76	MBAT1+10	MBAT1+½T +83
MASTER BLOCK TRANSFER WITH LOCAL DMA (BOUNDARY CROSSING)								
J1	DS*[L] to BLT*[H]		2	30	2	32	2	35
J2	DS*[H] to BLT*[L]		2	17	2	19	2	21
J3	DSi*[L] to LEDO[H/L]		2	21	2	23	2	25
J4	DSi*[H] to LADO[L/H]	4	1	16	2	18	2	20

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
SLAVE BLOCK TRANSFER (WRITE)								
** First Cycle **								
See: Local Bus Timing (VIC068A as local bus master)								
** Second and subsequent cycles **								
K1	DSi*[0] to LEDI[H]	4	4	20	4	22	4	24
K2	DSi*[0] to DS*[L]		6	35	5	36	5	39
K3	DSACKi*[0] and DS*[L] to DS*[H]	4	SBAT+9	SBAT+½T+41	SBAT+8	SBAT+½T+42	SBAT+7	SBAT+½T+52
K4	DSACKi*[0] and DS*[L] to DTACK*[L]	4	SBAT+12	SBAT+½T+51	SBAT+11	SBAT+½T+53	SBAT+10	SBAT+½T+67
K5	DSACKi*[0] and DS*[L] to ISOBE*[H]	4	SBAT+13	SBAT+½T+54	SBAT+11	SBAT+½T+56	SBAT+11	SBAT+½T+62
K6	DSACKi*[0] and DS*[L] to SWDEN*[H]	4	SBAT+12	SBAT+½T+50	SBAT+10	SBAT+½T+52	SBAT+10	SBAT+½T+61
K7	DSACKi*[0] and DS*[L] to LA[7:0] Valid	4	SBAT+T+10	SBAT+1½T+34	SBAT+T+8	SBAT+1½T+36	SBAT+T+8	SBAT+1½T+40
K8	DSACKi*[0] and DS*[L] to LEDI*[L]	4	SBAT+8	SBAT+½T+46	SBAT+7	SBAT+½T+48	SBAT+6	SBAT+½T+53
K9	DS1/0*[1] to DTACK*[H]	4	5	27	5	28	4	35
SLAVE BLOCK TRANSFER (READ)								
** First Cycle **								
See: Local Bus Timing (VIC068A as local bus master)								
** Second and subsequent cycles **								
L1	DS1/0*[1] to LEDO[L]		4	23	3	24	3	30
L2	DS*[H] to DS*[L]	4	DST+1½T−13	DST+1½T−2	DST+1½T−14	DST+1½T−3	DST+1½T−15	DST+1½T−4
L3	DS1/0*[0] to DENO*[L]	4	3	20	3	22	3	24
L4	DSACKi*[0] and DS*[0] to LEDO[H]	4	SBAT+8	SBAT+½T+36	SBAT+7	SBAT+½T+37	SBAT+6	SBAT+½T+41
L5	DSACKi*[0] and DS*[0] to DS*[H]	4	SBAT+9	SBAT+½T+41	SBAT+8	SBAT+½T+43	SBAT+7	SBAT+½T+52
L6	DSACKi*[0] and DS*[0] to DTACK*[L]		SBAT+11	SBAT+½T+47	SBAT+9	SBAT+½T+48	SBAT+9	SBAT+½T+53
L7	DSACKi*[0] and DS*[0] to LA[7:0] Valid	4	SBAT+T+9	SBAT+1½T+34	SBAT+T+8	SBAT+1½T+36	SBAT+T+8	SBAT+½T+40
L8	DS1/0*[1] to DENO*[H]	4	3	19	3	20	2	22
L9	DS1/0*[1] to DTACK*[H]	4	3	20	3	21	3	24
L10	LEDO[L] to LEDO[H]	4,18	T + 11	1½ + 25	T + 10	1½ + 26	1½ + 9	1½ + 27
L11	DTACK*[0] to DS*[H]	4,18	T + 15	1½ + 45	1½ + 14	1½ + 46	1½ + 13	1½ + 47
REGISTER ACCESS								
M1	PAS*[0] & DS*[0] & CS*[0] to DSACKi*[L]	4	4T+5	5T+34	4T+5	5T+35	4T+4	5T+38

Operation		Notes	Commercial		Industrial		Military	
			Min.	Max.	Min.	Max.	Min.	Max.
M2	PAS*[0] & DS*[0] & CS*[0] to LD[7:0] Valid	4, 9	3T+5	4T+28	3T+5	4T+29	3T+4	4T+37
M3	AS*[0] & ICFSEL*[0] to DTACK*[L]	4	4T+6	4T+30	4T+5	4T+31	4T+5	4T+34
RESET								
N1	LBG*[0] to HALT*[L], RESET*[L]	4	8	36	7	37	6	48
N2	IRESET*[0] to LBR*[L]	4	6	29	5	30	5	33
N3	IRESET*[0] to IPL0[Z]	4	2	16	2	16	2	20
SET-UP TIMES								
P1	LA, ASIZ[1:0] Valid to PAS*[0]	4	−2T		−2T		−2T	
P2	SIZ[1:0], WORD*, FC[2:1] Valid to PAS*[0]	4	−2T		−2T		−2T	
P3	LD[7:0] Valid to DS*[0]	4	0		0		0	
HOLD TIMES								
Q1	PAS*[1] to LA, ASIZ[1:0] Invalid	4	0		0		0	
Q2	PAS*[1] to SIZ[1:0], WORD*, FC[2:1] Invalid	4	0		0		0	
Q3	DS*[1] to LD[7:0] Invalid	4	0		0		0	
Q4	DS1/0*[1] to DTACK*[H]	4	0		0		0	

Notes:

2. T = CLK64M clock period
   SAT = Slave Access Timing
   MBAT0 = Master Block Transfer Timing 0
   MBAT1 = Master Block Transfer Timing 1
   SBAT = Slave Block Transfer Timing
   DST = Data Strobe Timing
3. ROR mode.
4. Timing specified but not tested.
5. While VMEbus system controller.
6. Synchronous delay depends on speed in which BGiIN* is returned. If BGiIN* is returned in zero time after request, synchronous delay will be maximum.
7. Write operation only.
8. While VMEbus master.
9. Read operation only.
10. Master write post only.
11. Skew.
12. Input requirement.
13. Slave write post only.
14. VMEbus interrupt only.
15. Local interrupt (LICR[4] = 1) only.
16. Local interrupt (LICR[4] = 0) only.
17. “Slow” Slave.
18. “Slow” Master.

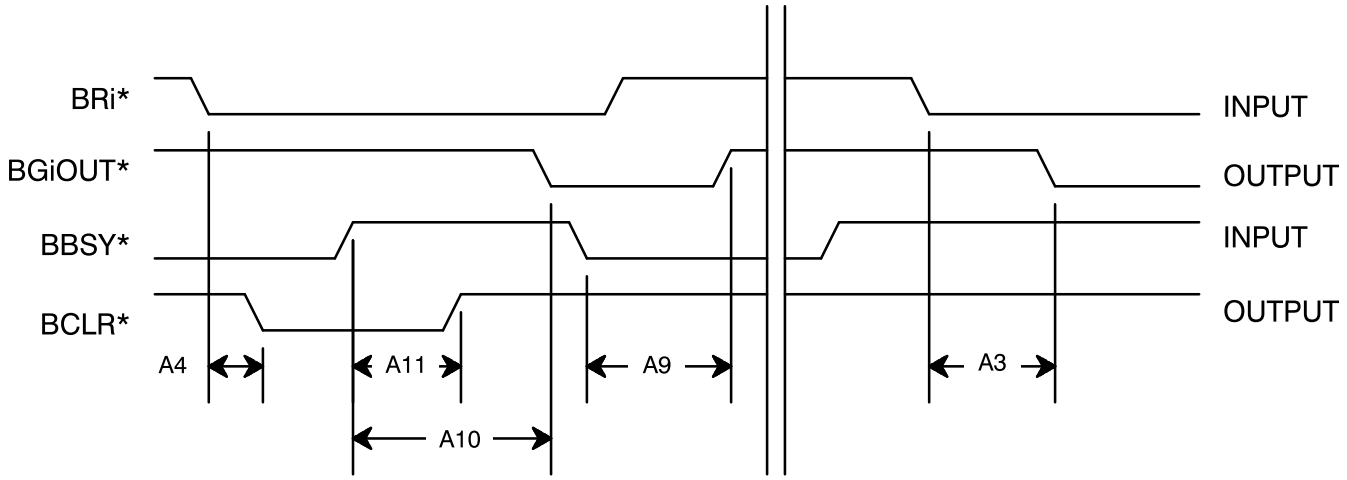


Figure 1−21. VMEbus Arbitration—VIC068A as arbitor, priority interrupt

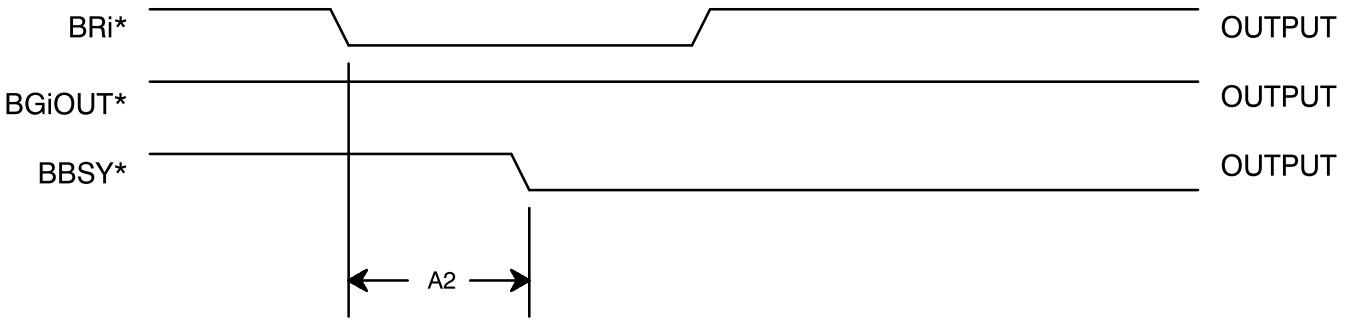


Figure 1−22. VMEbus Arbitration—VIC068A as System Controller (granting bus internally)

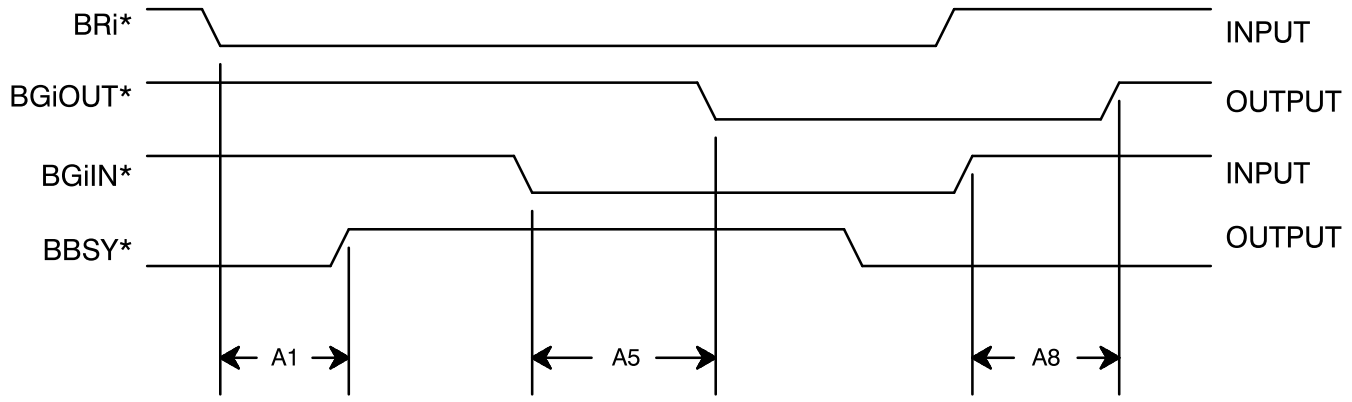


Figure 1−23. VMEbus Arbitration—VIC068A (not System Controller) honoring ROR

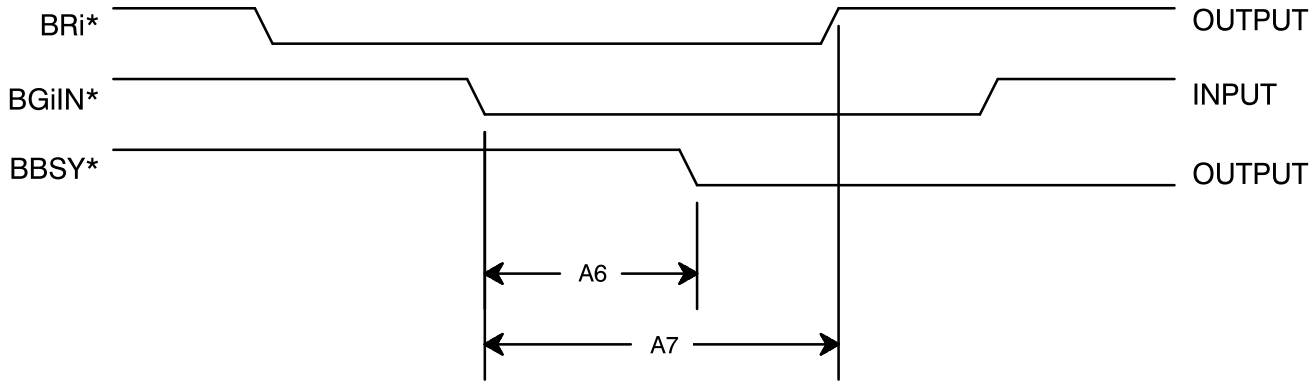


Figure 1−24. VMEbus Arbitration—VIC068A (not System Controller) taking the VMEbus

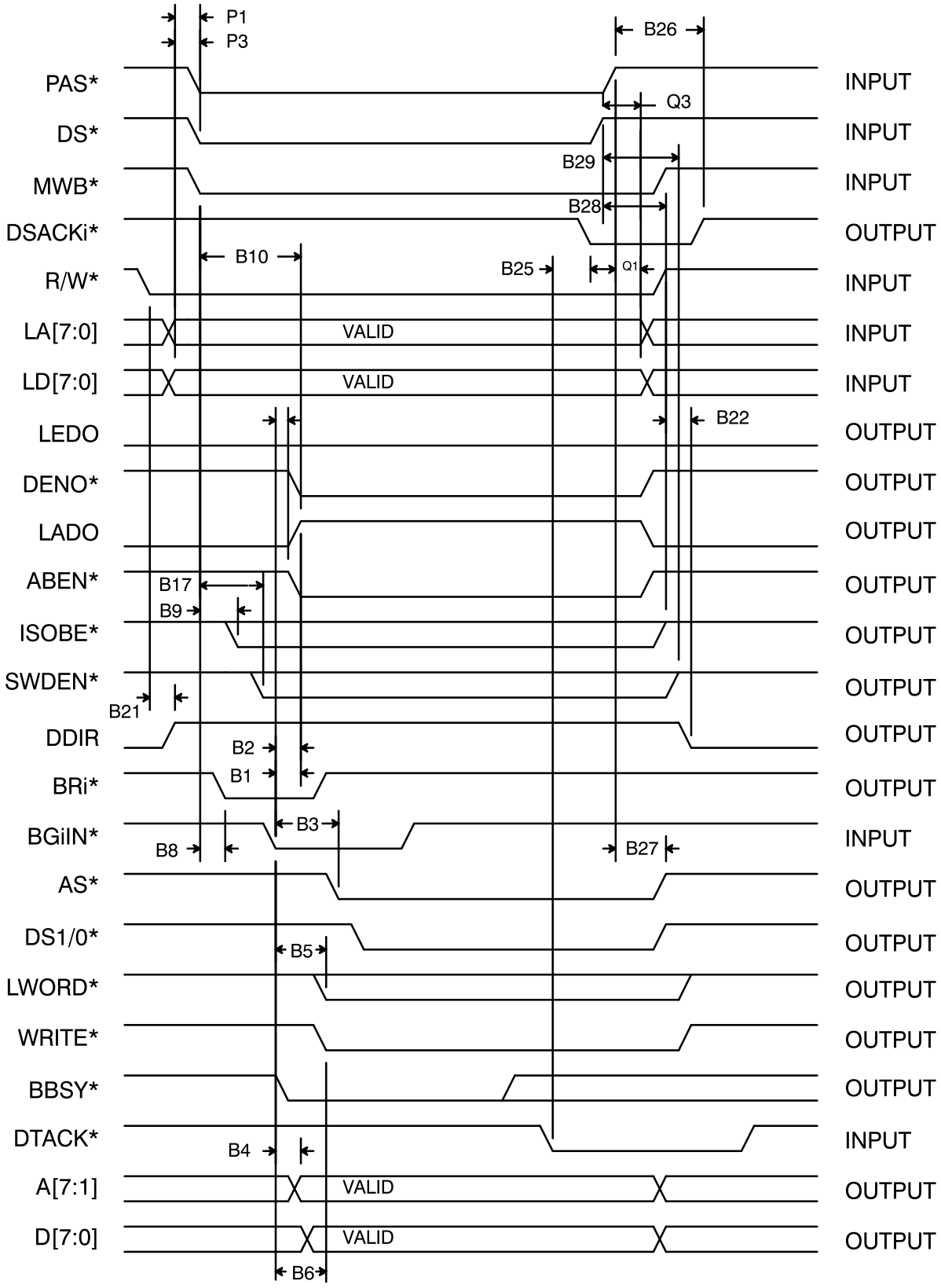


Figure 1−25. Master Write

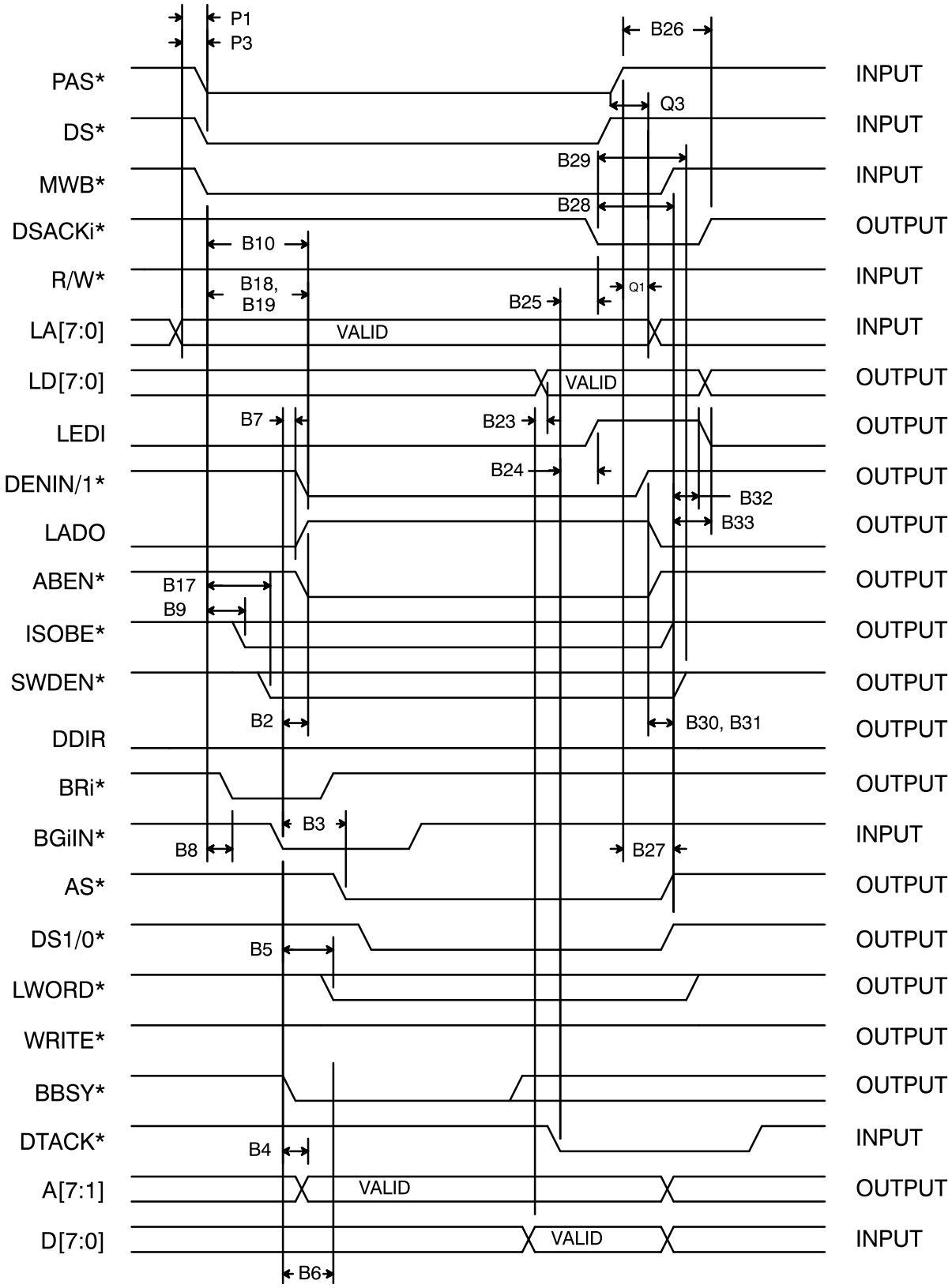


Figure 1−26. Master Read

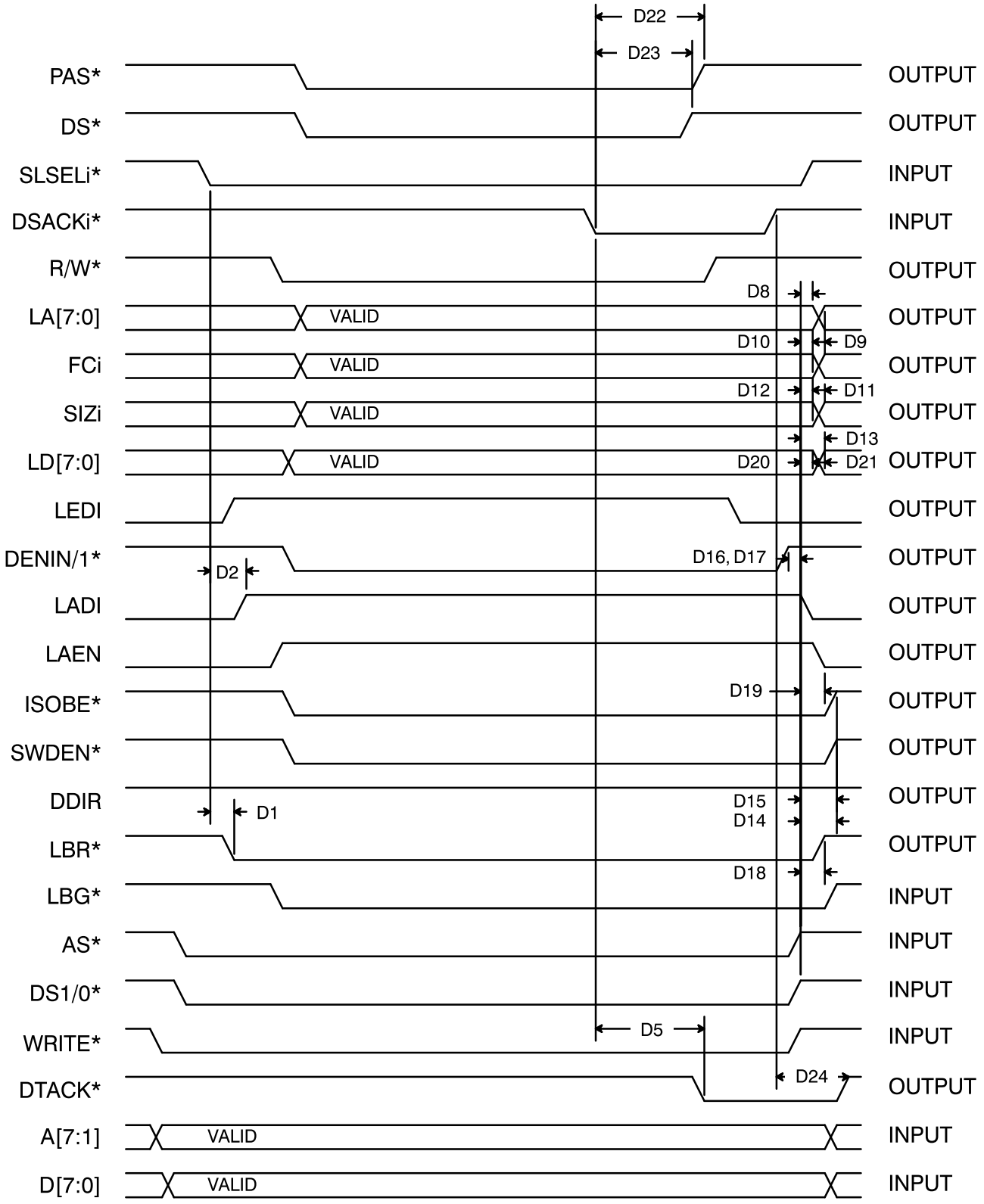


Figure 1−27. Slave Write

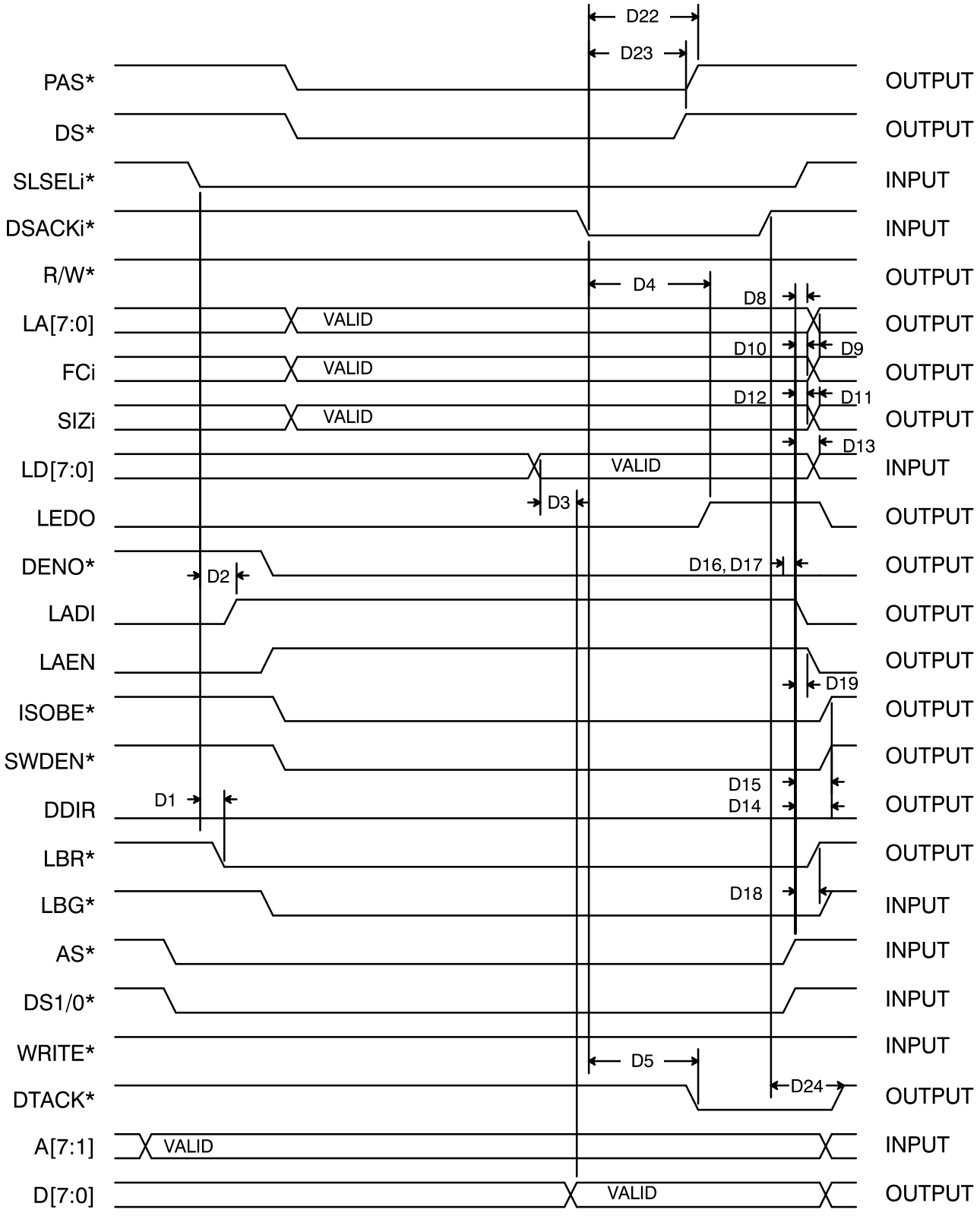


Figure 1−28. Slave Read

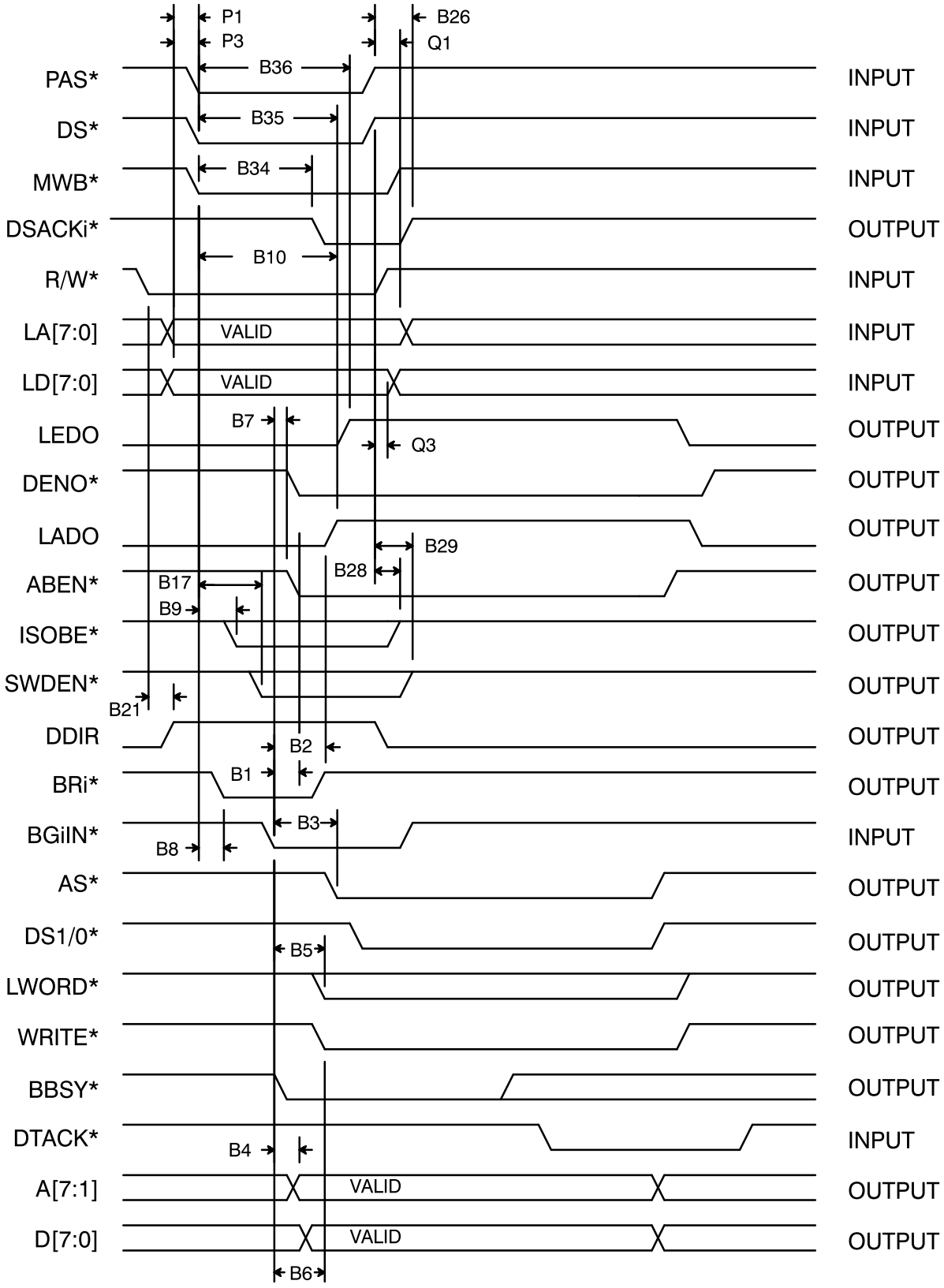


Figure 1−29. Master Write Post

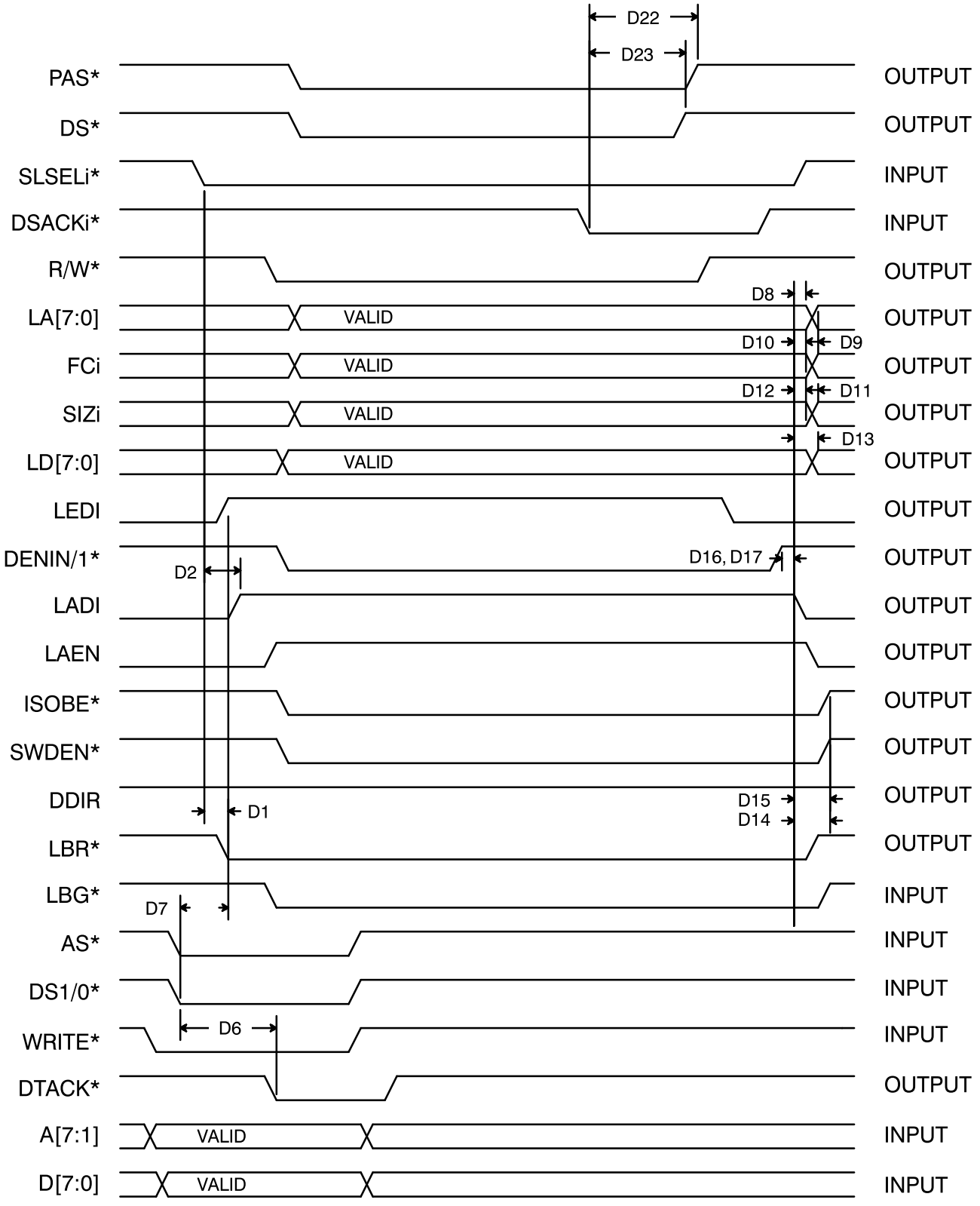


Figure 1−30. Slave Write Post

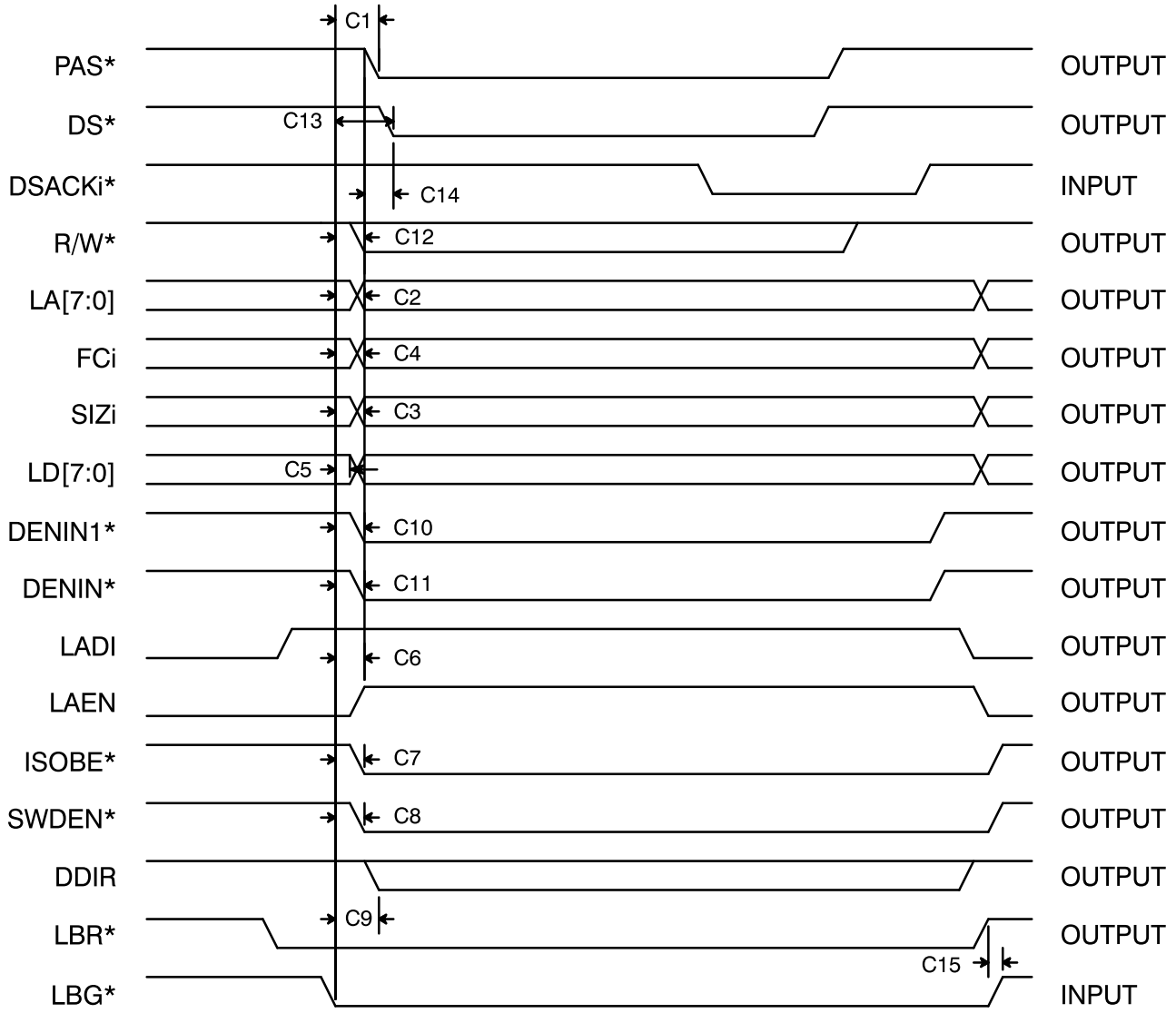


Figure 1−31. Local Bus

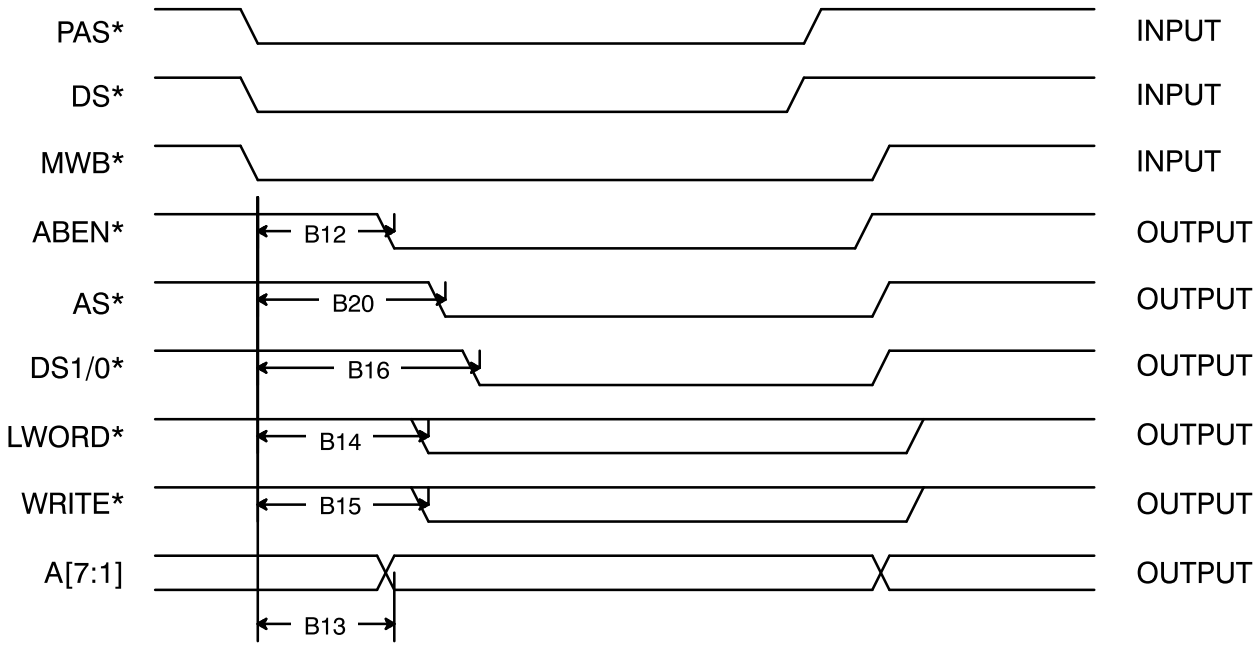


Figure 1−32. While VME Master

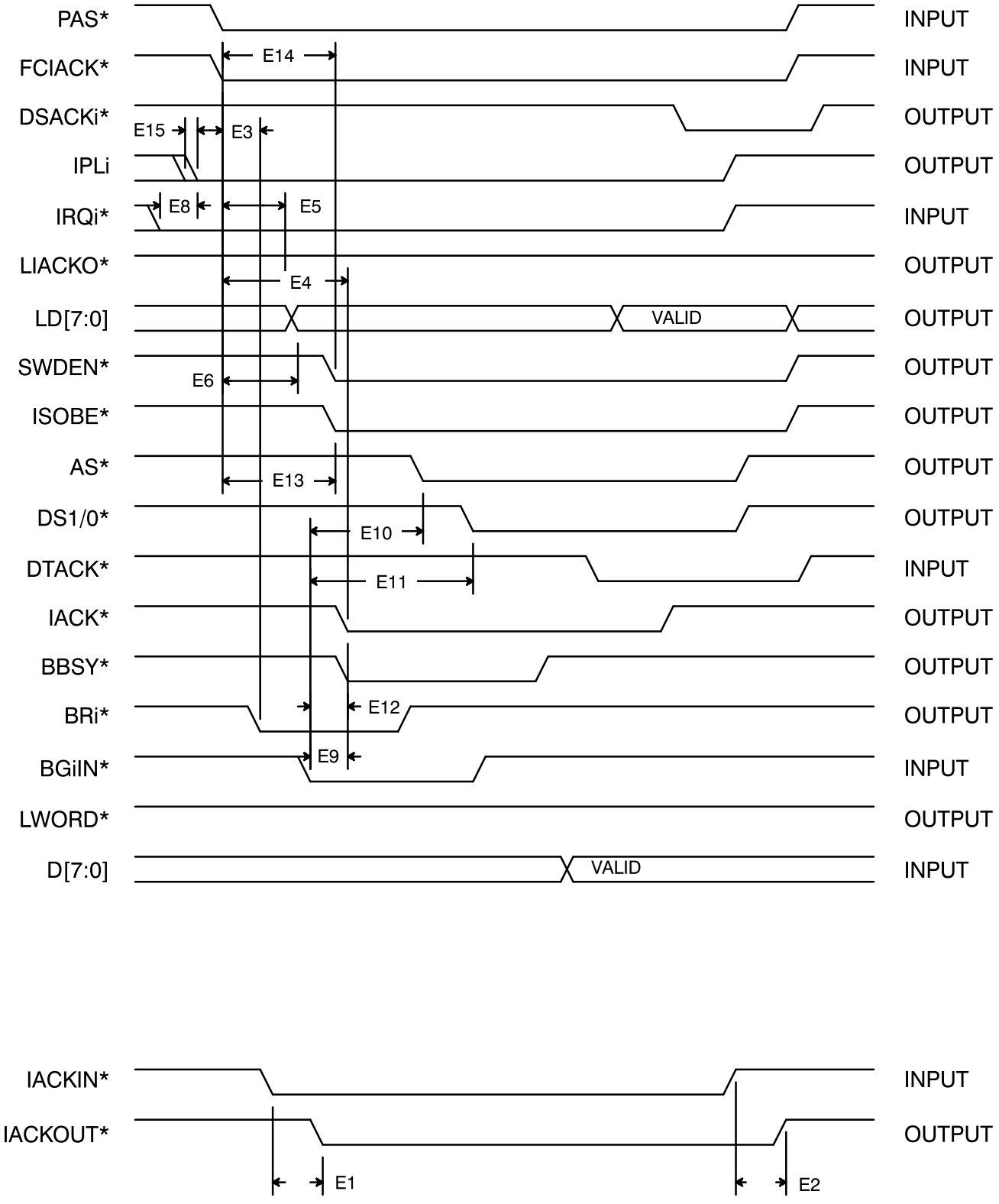


Figure 1−33. VME IACK

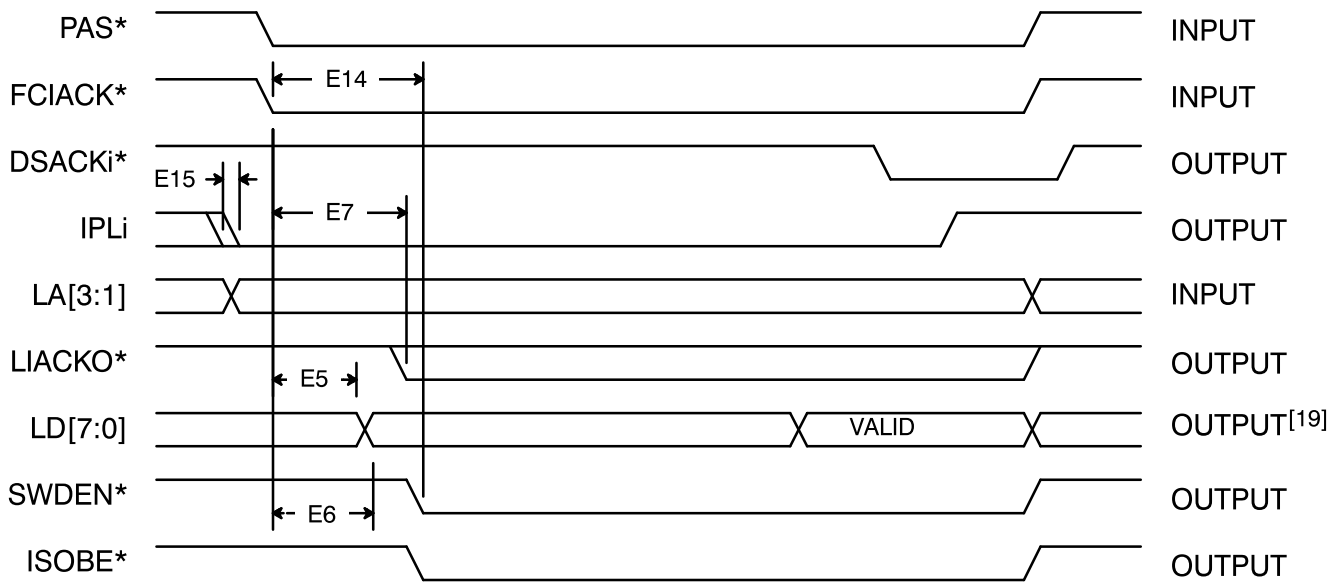


Figure 1−34. Local IACK

Note:

19. If VIC068A is configured to supply vector.

Initiation

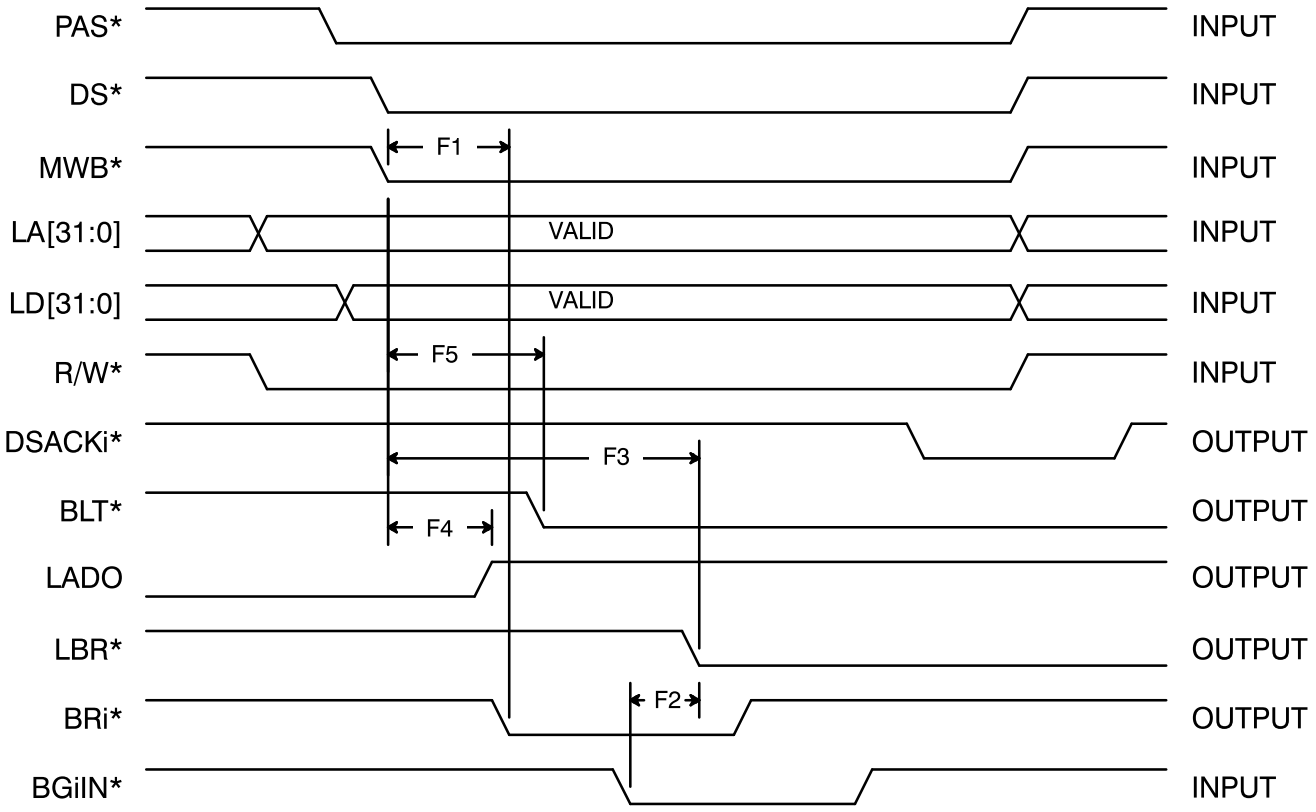


Figure 1−35. Initiation

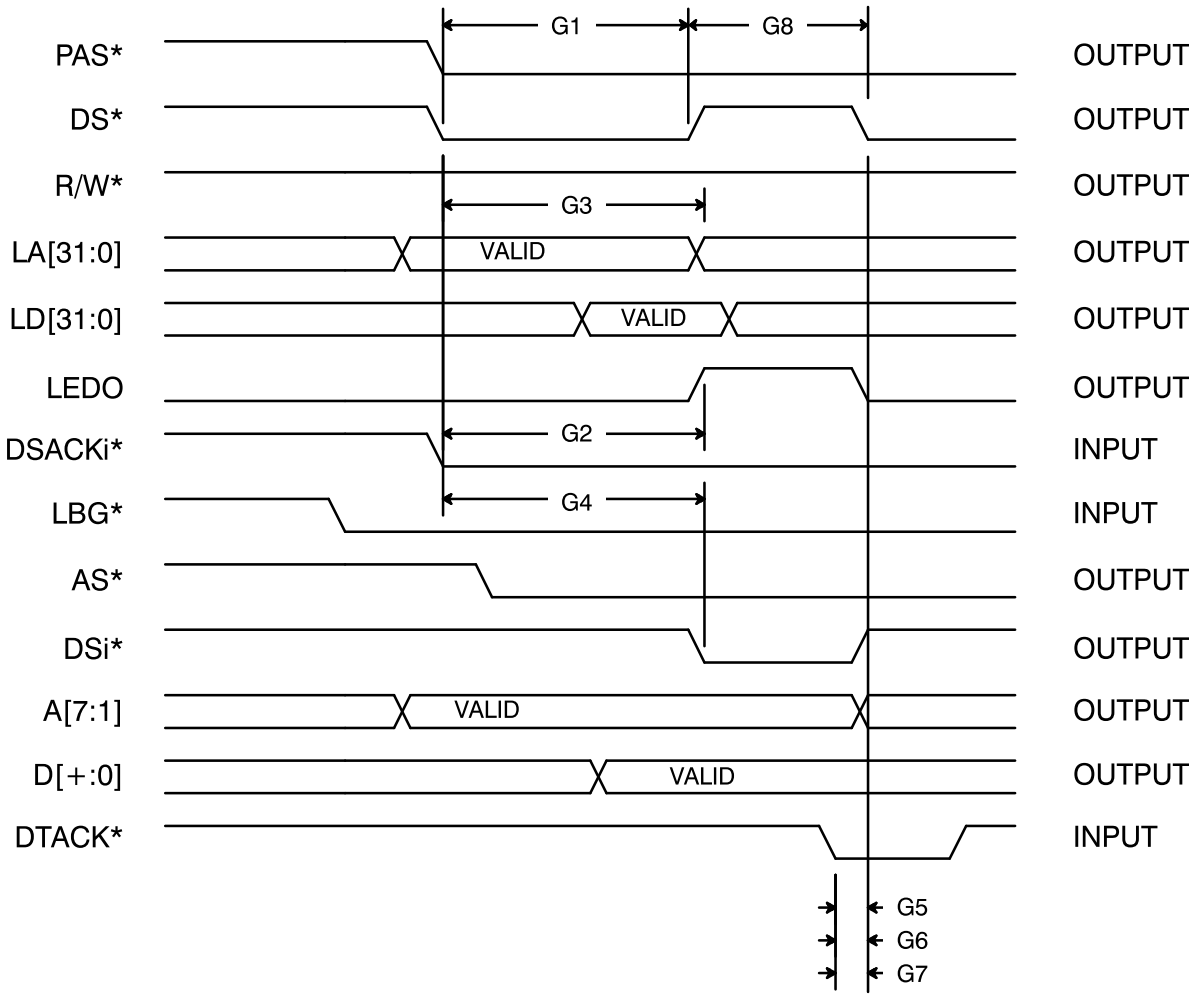


Figure 1−36. First MBLT Write

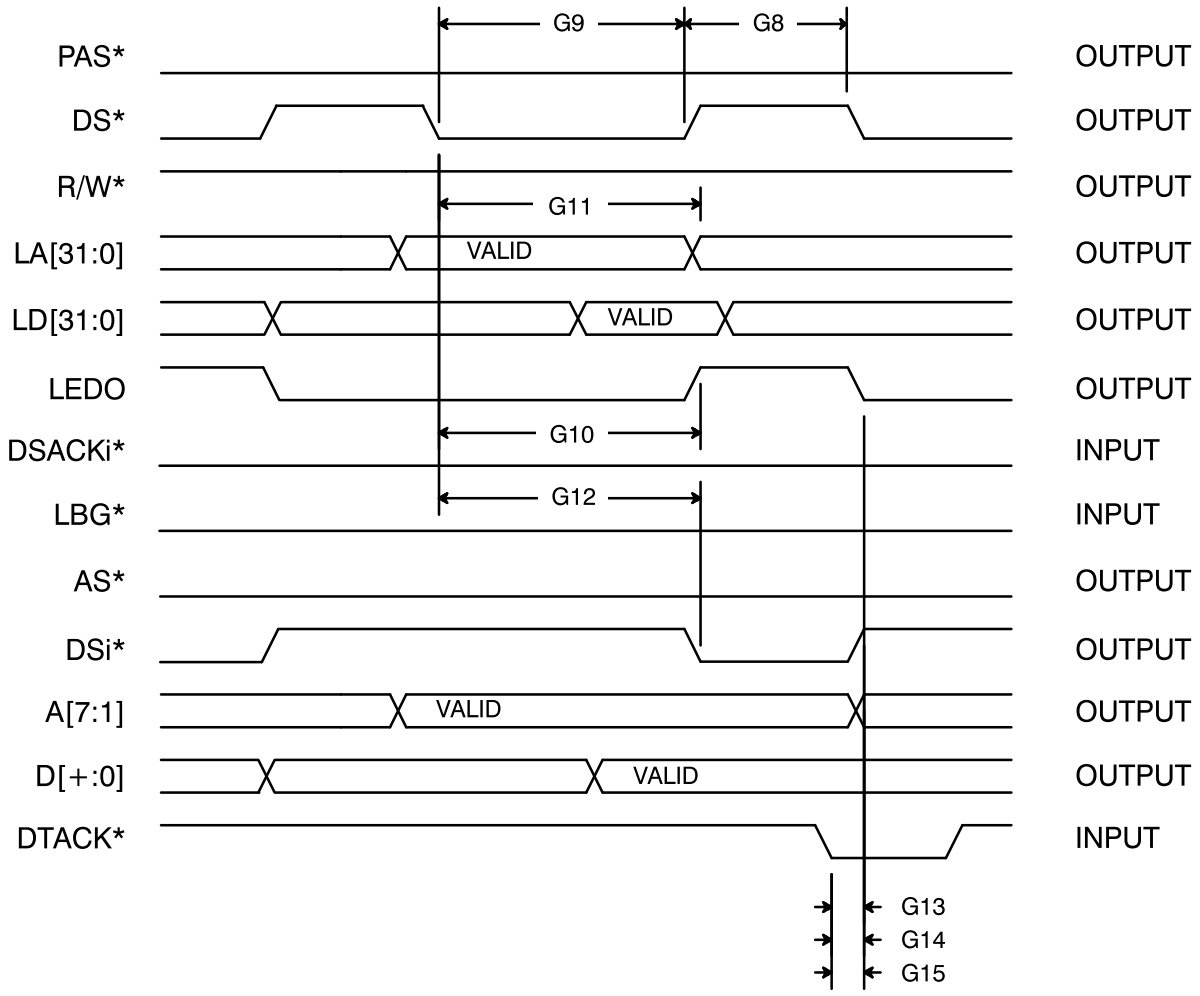


Figure 1−37. Second MBLT Write

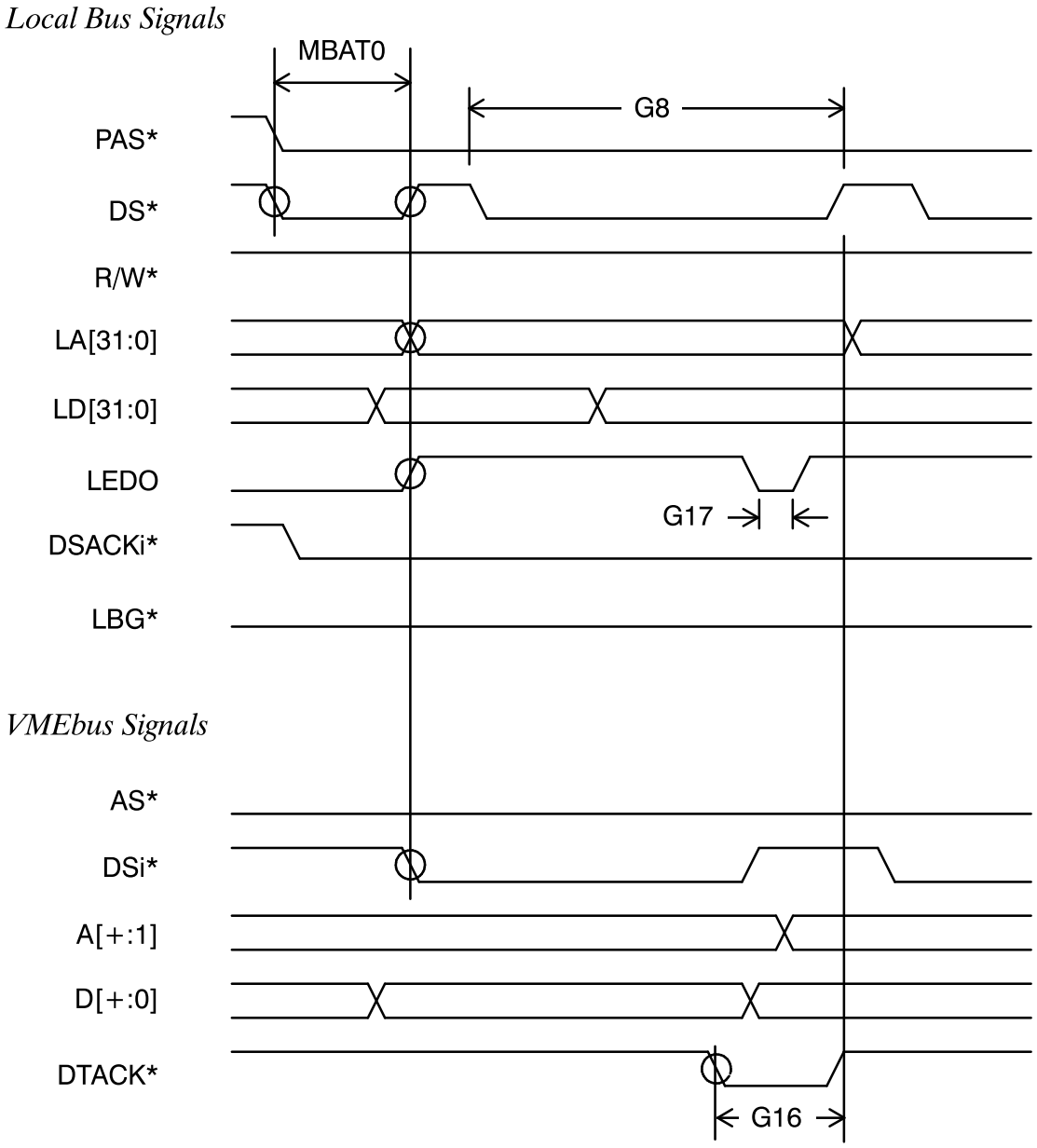


Figure 1−38. Master Block Transfer—Write (Slow Slave)

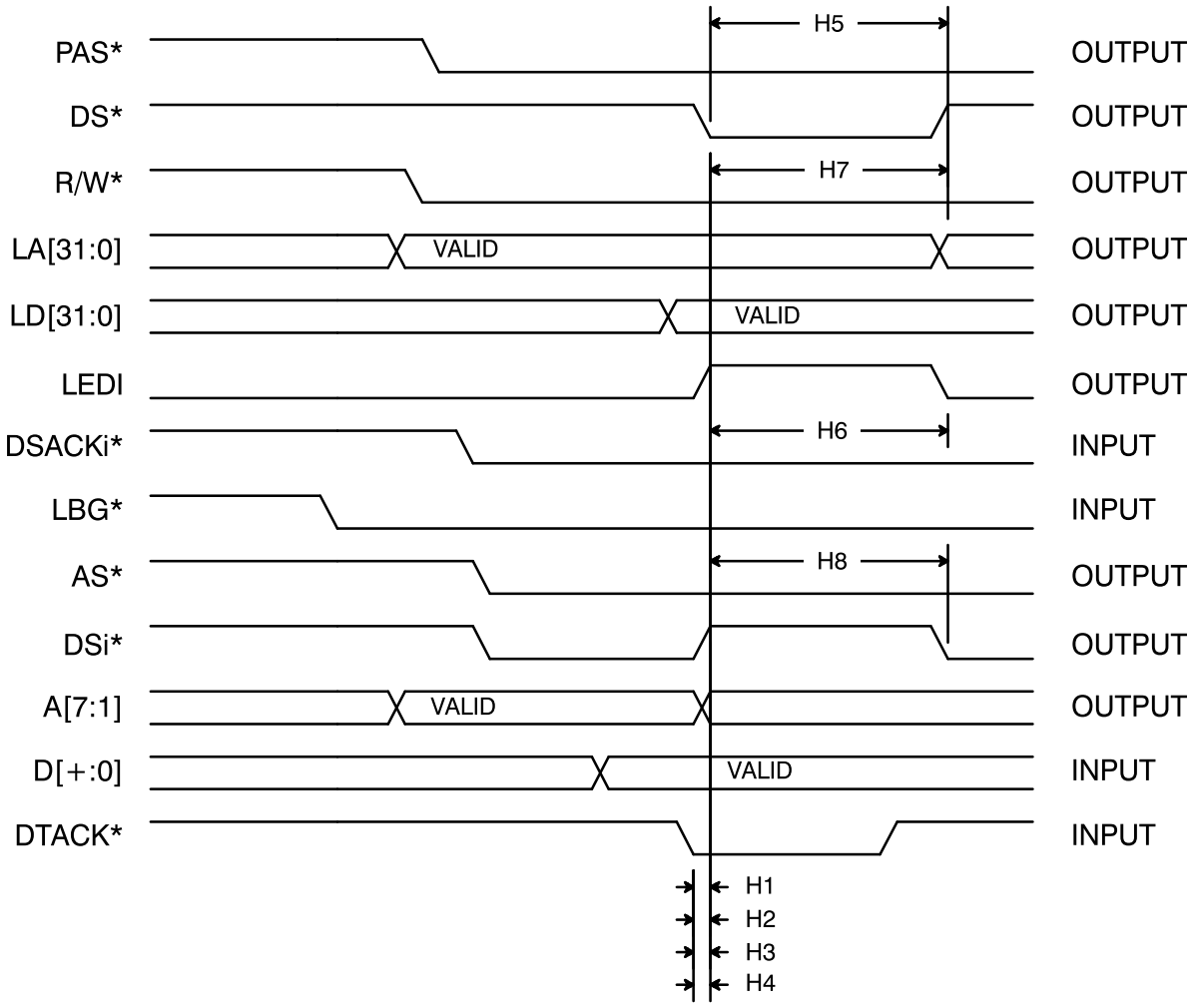


Figure 1−39. First MBLT Read

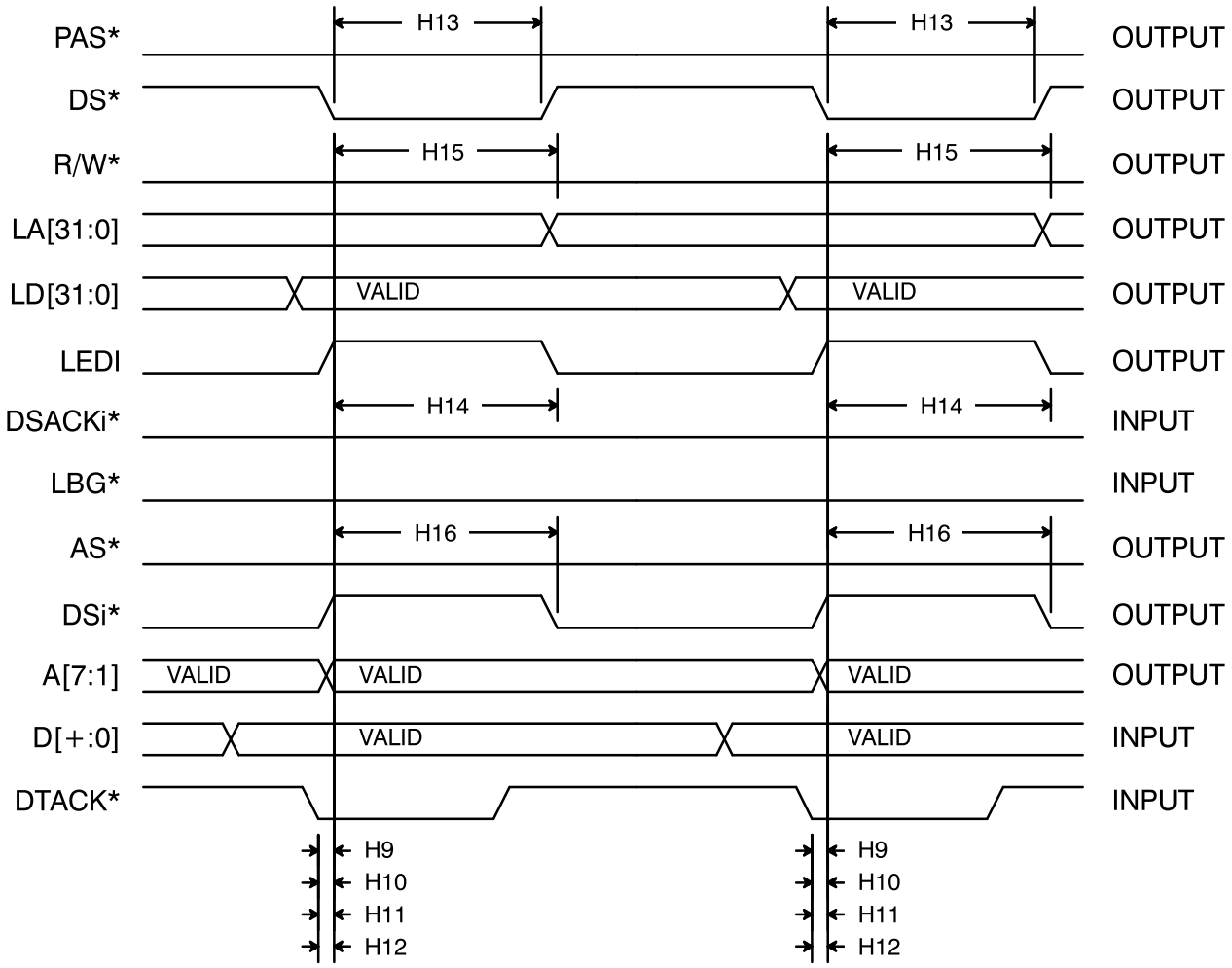
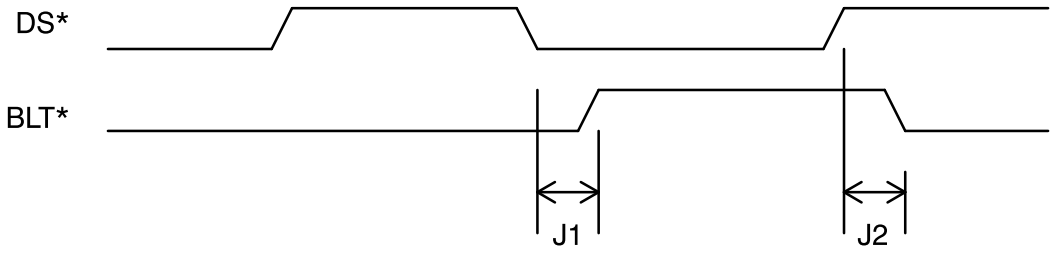


Figure 1−40. Second MBLT Read

Local Boundary Crossing



VMEbus Boundary Crossing

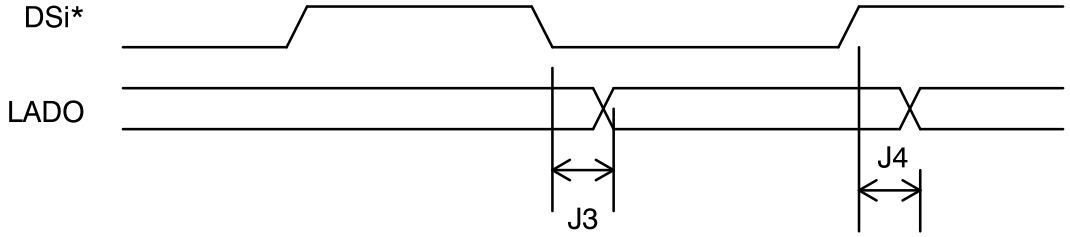


Figure 1−41. Boundary Crossing

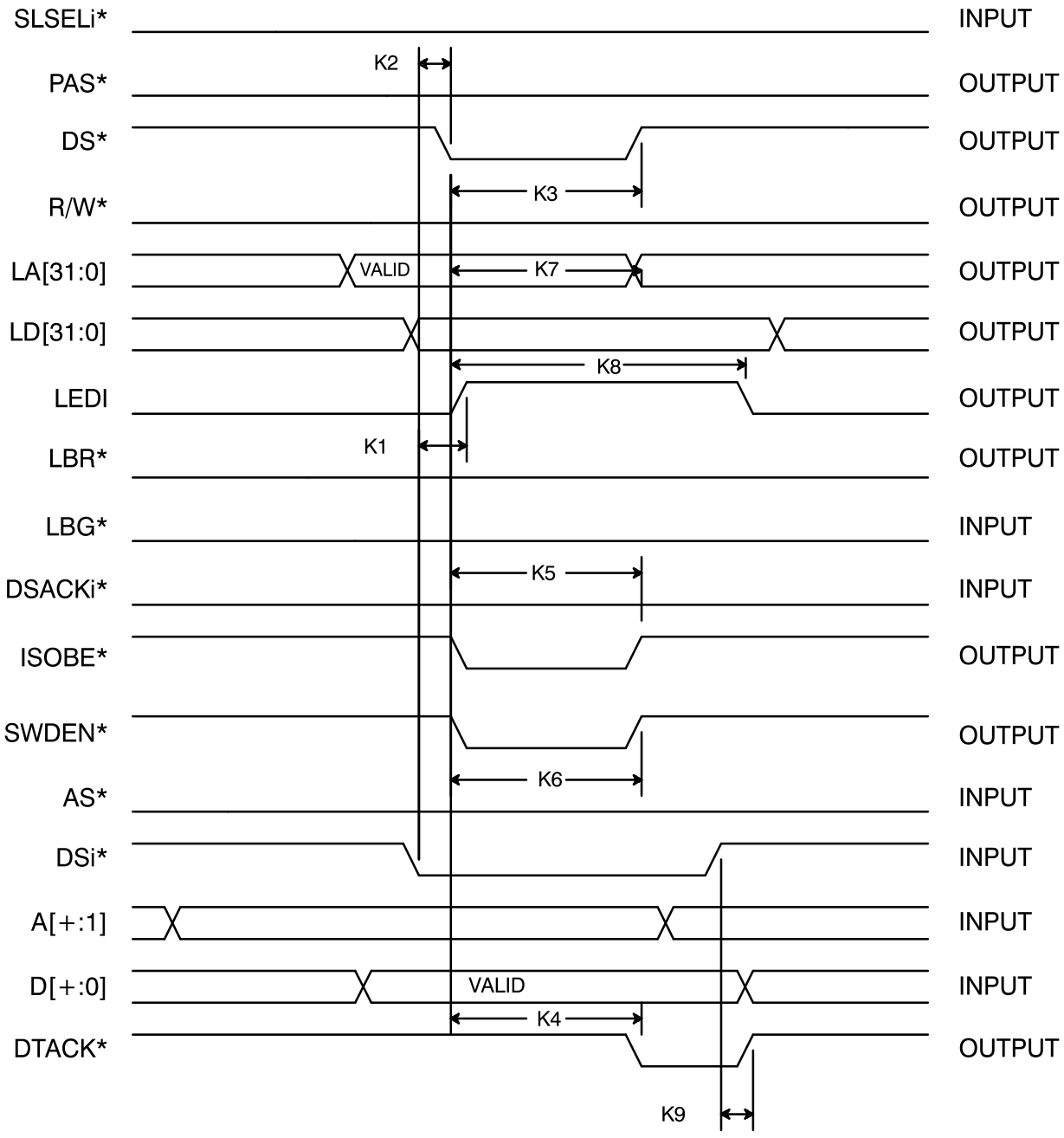


Figure 1−42. Slave Write BLT

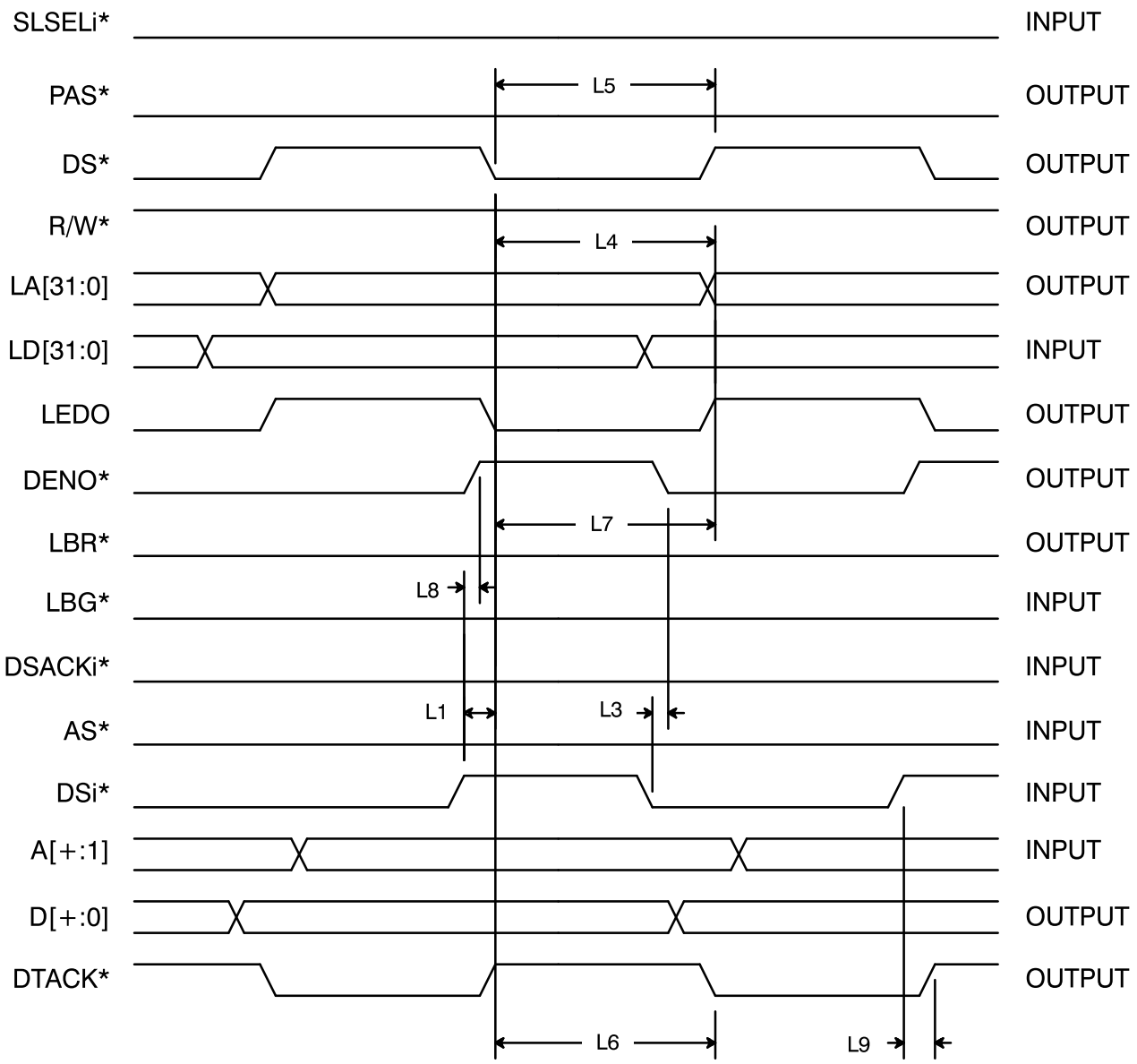


Figure 1−43. Slave Read BLT

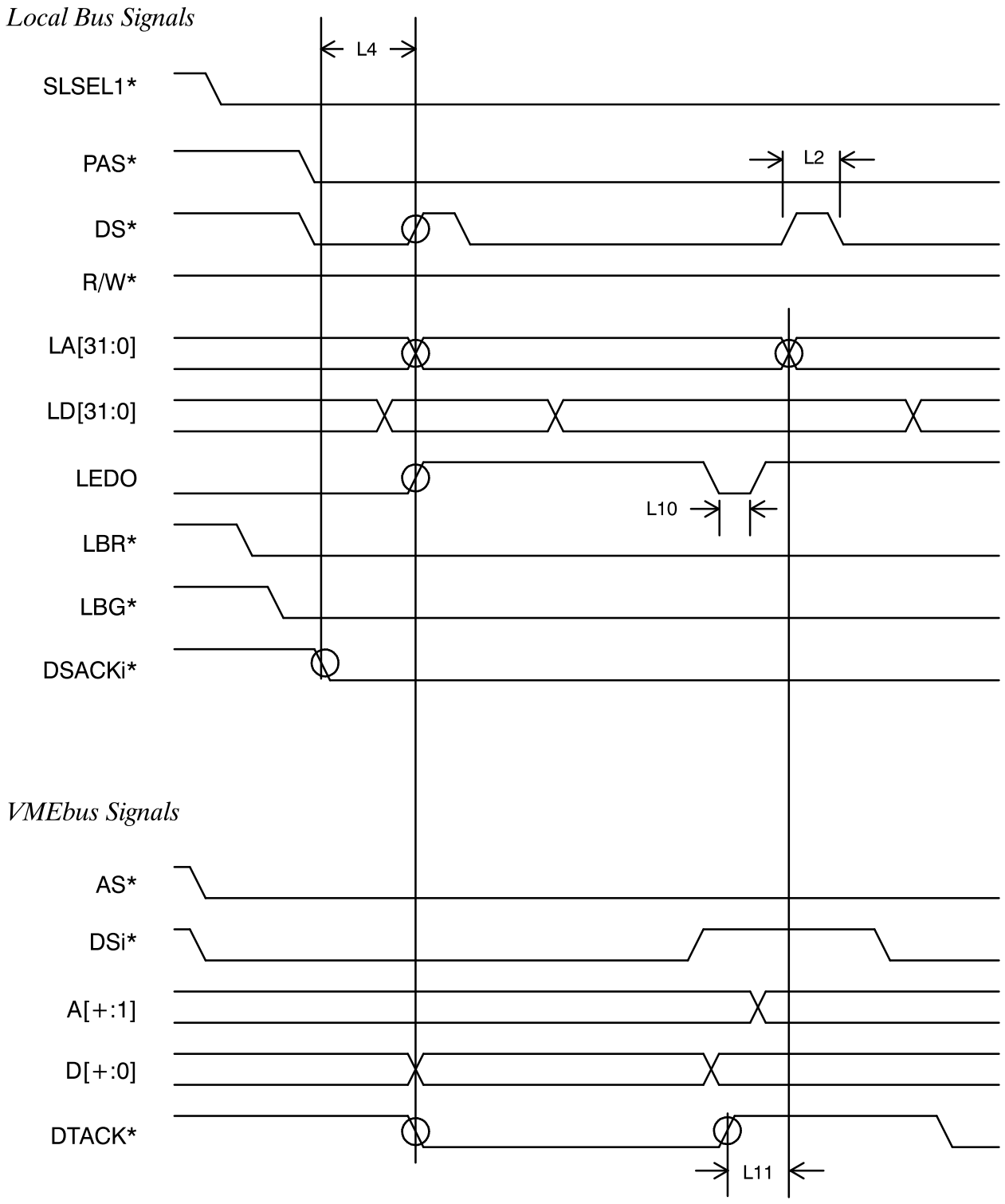
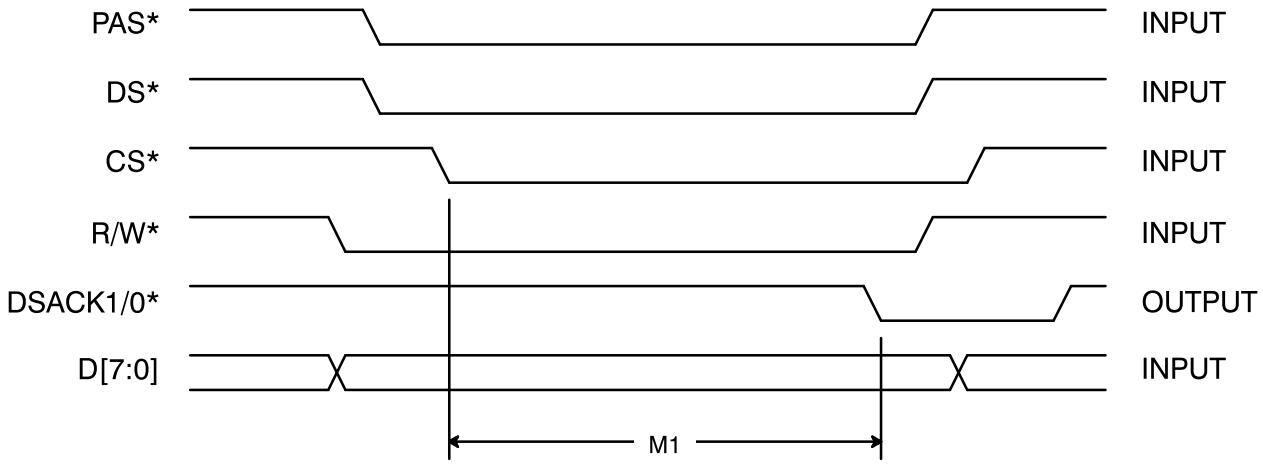
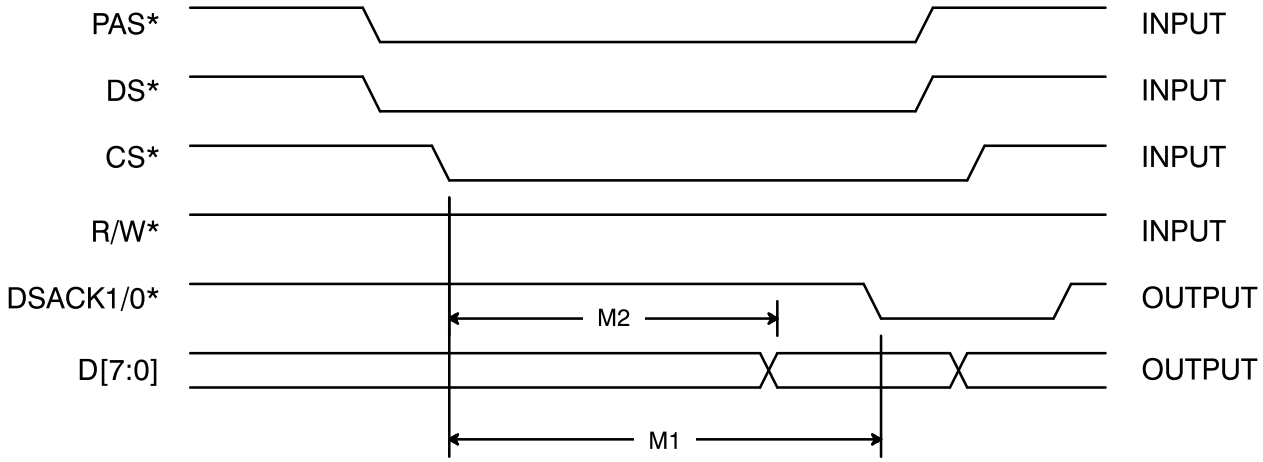


Figure 1−44. Slave Block Transfer—Read, Slow Master

Write



Read



ICF Select

Figure 1−45. Register Operations

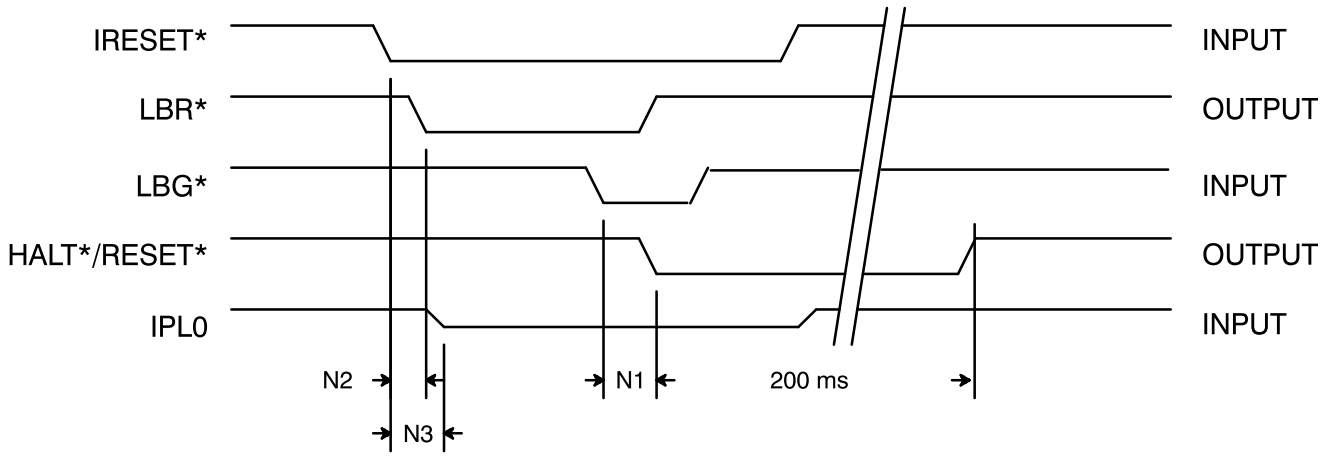


Figure 1−46. Global Reset

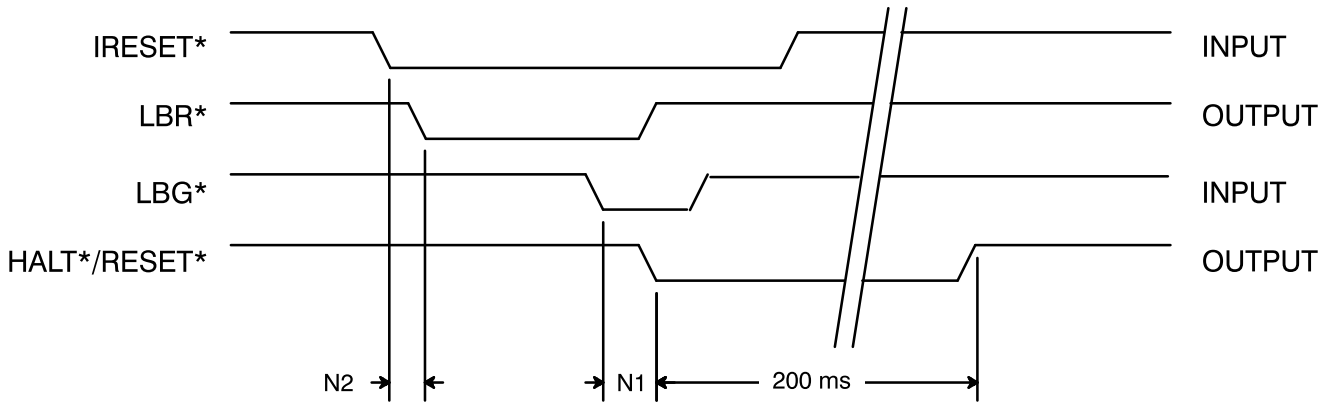


Figure 1−47. Internal Reset