1.2 VIC068A Signal Descriptions

1.2.1 VMEbus Signals

This chapter lists VMEbus-specified signals that are driven and received directly by the VIC068A. For complete definitions and descriptions of these signals, refer to the VMEbus specification (IEEE 1014).

SYSRESET*

Input: Yes
Output: Yes, open collector
Drive: 48 mA

This is the VMEbus system reset signal. A Low level on this signal resets the internal logic of the VIC068A and asserts the signals HALT* and RESET*. These signals remain asserted for a minimum of 200 ms. If the VIC068A is configured as VMEbus system controller, a Low level on IRESET* asserts SYSRESET* for a minimum of 200 ms. See section 1.11.1.

ACFAIL*

Input: Yes
Output: No
Drive: None

This is the VMEbus AC fail signal. This signal should be driven by the VMEbus power monitor (if installed), not the VIC068A. The VIC068A can be enabled to provide a local interrupt when this signal is asserted. See section 1.9.5.

SYSFAIL*

Input: Yes
Output: Yes, open collector
Drive: 48 mA

As an output, the SYSFAIL* signal is asserted when it detects that HALT* has been asserted for more than 6 µs by a source other than the VIC068A.

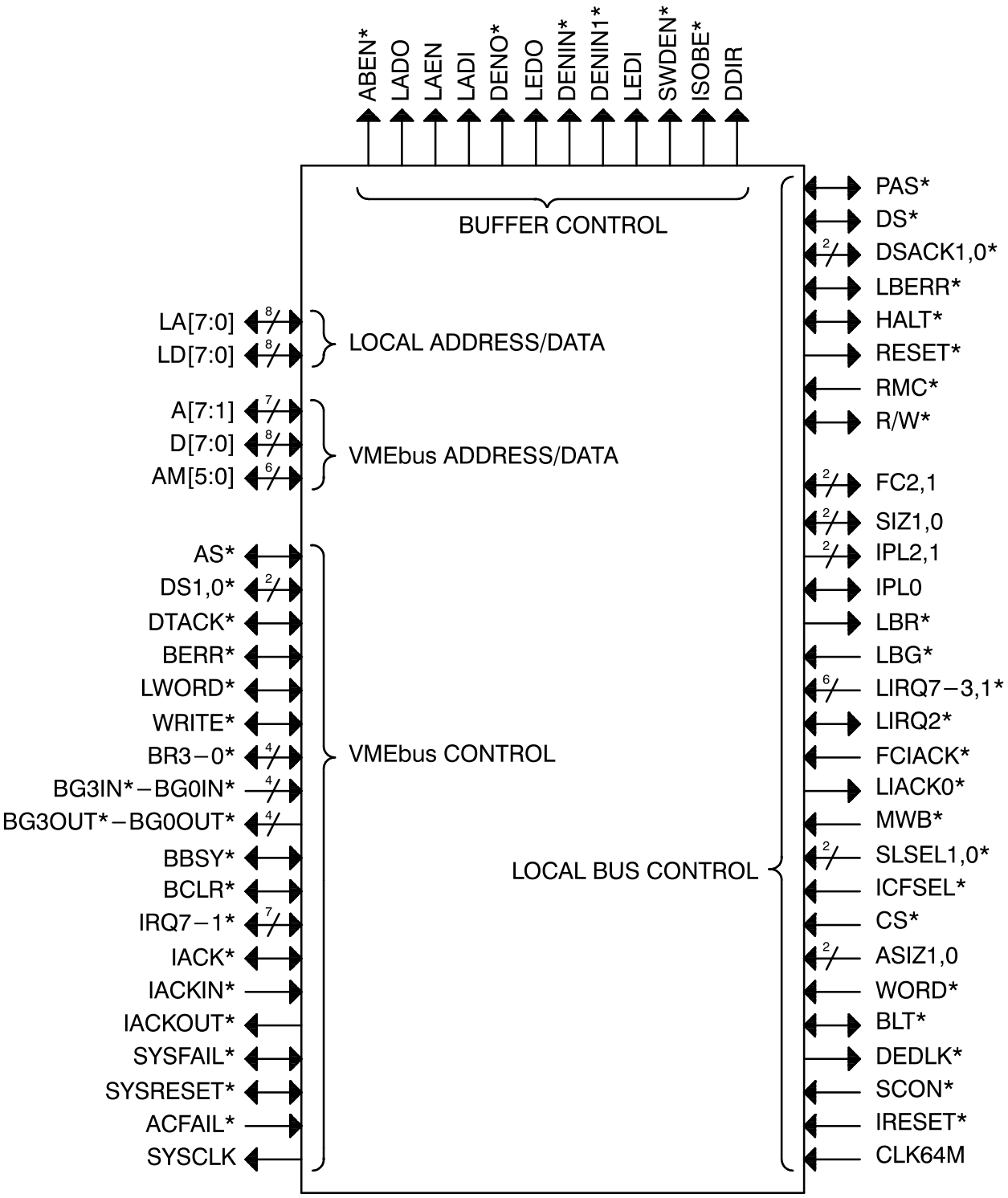

Figure 1−3. VIC068A Signal Diagram

This signal is asserted by the VIC068A after a global reset. It may be masked by clearing ICR6[6] or by setting ICR7[7]. The VIC068A can also be enabled to provide a local interrupt on the assertion of this signal. See section 1.9.5.

SYSCLK

Input: No
Output: Yes, three-state
Drive: 64 mA

This is the VMEbus system clock signal. This signal is driven by the VIC068A when configured as system controller (SCON* asserted). The output frequency is one-fourth the frequency delivered to the VIC068A CLK64M signal. To deliver the required 16 MHz on this signal, the VIC068A must run at 64 MHz. The VIC068A does not use this signal internally.

BR3* – BR0*

Input: Yes
Output: Yes, open collector
Drive: 48 mA

These are the VMEbus Bus Request signals.

BG3IN* – BG0IN*

Input: Yes
Output: No
Drive: None

These are the VMEbus daisy-chained Bus-Grant-In signals.

BG3OUT* – BG0OUT*

Input: No
Output: Yes
Drive: 8 mA

These are the VMEbus daisy-chained Bus-Grant-Out signals.

BBSY*

Input: Yes
Output: Yes, rescinding
Drive: 48 mA

This is the VMEbus Bus-Busy signal.

BCLR*

Input: Yes
Output: Yes, three-state
Drive: 64 mA

This is the VMEbus Bus-Clear signal.

D7 − D0

Input: Yes
Output: Yes, three-state
Drive: 48 mA

These are the VMEbus low-order data lines.

A7 − A1

Input: Yes
Output: Yes, three-state
Drive 48 mA

These are the VMEbus low-order address lines.

AS*

Input: Yes
Output Yes, rescinding
Drive: 64 mA

This is the VMEbus Address Strobe signal.

DS1* − DS0*

Input: Yes
Output: Yes, rescinding
Drive: 64 mA

These are the VMEbus Data Strobe signals.

DTACK*

Input: Yes
Output: Yes, rescinding
Drive: 48 mA

This is the VMEbus Data-Transfer-Acknowledge signal.

BERR*

Input: Yes
Output: Yes, rescinding
Drive: 48 mA

This is the VMEbus Bus-Error signal.

WRITE*

Input: Yes
Output: Yes, rescinding
Drive: 48 mA

This is the VMEbus Data-Direction signal.

LWORD*

Input: Yes
Output: Yes, rescinding
Drive: 48 mA

This is the VMEbus Longword signal.

AM5 – AM0

Input: Yes
Output: Yes, three-state
Drive: 48 mA

These are the VMEbus Address-Modifier signals.

IACK*

Input: Yes
Output: Yes, rescinding
Drive: 48 mA

This is the VMEbus Interrupt Acknowledge signal.

IACKIN*

Input: Yes
Output: No
Drive: None

This is the VMEbus daisy-chained Interrupt-Acknowledge-In signal.

IACKOUT*

Input: No
Output: Yes
Drive: 8 mA

This is the VMEbus daisy-chained Interrupt-Acknowledge-Out signal.

IRQ7* – IRQ1*

Input: Yes
Output: Yes, open collector
Drive: 48 mA

These are the VMEbus Interrupt request signals.

1.2.2 Local Signals

These signals define the local bus structure of the VIC068A. They are modeled after Motorola 68K signals.

LD7 – LD0

Input: Yes
Output: Yes, three-state
Drive: 8 mA

These are the Local Data 7–0 signals. These signals are typically connected to the local processor data lines D[7:0] through an isolation buffer. VIC068A register accesses are also made through these data signals.

LA7 – LA0

Input: Yes
Output: Yes, three-state
Drive: 8 mA

These are the Local Address 7–0 signals. These signals are typically connected to the local processor address lines. VIC068A registers are also addressed through these signals. When acting as the local bus master, the VIC068A drives these lines with the LAEN (active High) signal to supply the local address.

CS*

Input: Yes
Output: No
Drive: None

This is the VIC068A chip select signal. This signal should be asserted whenever access to the VIC068A internal registers is required. See section 1.7.2.

PAS*

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

This is the physical/processor address strobe. This signal is used to qualify an incoming address when performing VMEbus master operations or register operations. This signal is driven when performing slave transfers, DRAM refresh, slave block transfers and block transfers with local DMA. When acting as an output, the minimum assertion and negation timing for this signal is configured by the Local Bus Timing register (LBTR).

DS*

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

This is the local data strobe. This signal is used to qualify incoming data when performing VMEbus master operations or register operations. This signal is driven when performing slave transfers, DRAM refresh, slave block transfers, and block transfers with local DMA. When acting as an output, the minimum assertion and negation timing for this signal is directed by the Local Bus Timing register (LBTR).

DSACK1*, DSACK0*

Input: Yes
Output: Yes, three-state
Drive: 8 mA

These are the local data-size-acknowledge signals. One or both of these signals should be asserted to the VIC068A whenever the VIC068A is local bus master to acknowledge the successful completion of each cycle of a slave transfer, slave block transfer, or block transfers with local DMA. The VIC068A asserts one or both of these signals to acknowledge the

successful completion of a VMEbus master operation (after receiving the VMEbus DTACK* signal). The following should be noted about the DSACK1/0* signals:

- The VIC068A asserts a 16-bit DSACKi* code when the WORD* signal is asserted, indicating access to a D16 VMEbus resource is complete. See section 1.5.3.
- The VIC068A treats the assertion of any DSACK1/0* signal as a 32-bit acknowledge for slave accesses.
- The VIC068A does not directly support 16- or 8-bit local bus sizes.
- The VIC068A always asserts both DSACK*s for register accesses as well as for interrupt acknowledge cycles.

LBERR*

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

This is the local bus-error signal. This signal should be asserted to the VIC068A whenever the VIC068A is local bus master to acknowledge the unsuccessful completion of a slave transfer, slave block transfer, and block transfers with local DMA, in which case the VIC068A asserts the VMEbus BERR* signal. The VIC068A asserts this signal to acknowledge the unsuccessful completion of a VMEbus master operation (after receiving the VMEbus BERR* signal).

During deadlocks, LBERR* may also be configured to assert with the HALT* signal to initiate a Motorola 68K retry sequence. LBERR* may also be configured to assert without HALT* for RMC cycle deadlocks. See section 1.5.7.

RESET*

Input: No
Output: Yes, three-state
Drive: 8 mA

This is the local reset indication signal. This signal is asserted whenever the VIC068A is in a reset state. An internal, global, or system reset causes the VIC068A to start its 200-ms reset timer and to assert RESET* for a minimum of one reset timer period. If a reset condition is present at the end of the reset timer period (200 ms), the reset timer is retriggered for an additional 200-ms period and continues to assert RESET*. This reset timer retrigger operation repeats until the reset condition is not present when the reset timer period ends. Once the VIC068A stops driving RESET* Low, this pin is three-stated. Since the VIC068A does

not actively drive RESET* to its inactive state, a pull-up resistor should be used on this signal to ensure that any device monitoring the RESET* signal will see its removal. See section 12.1.

HALT*

Input: Yes
Output: Yes, three-state
Drive: 8 mA

This is the "halted" condition indication signal. This signal, along with RESET*, is asserted during reset conditions. An internal, global, or system reset causes the VIC068A to assert HALT* for a minimum of 200 ms. If the reset condition continues for longer than 200 ms, HALT* begins additional 200-ms timeouts until all reset conditions are cleared. Assertion of HALT* for more than 6 µs by anything other than the VIC068A causes the VIC068A to assert SYSFAIL*.

HALT* may be configured to assert during deadlock conditions along with LBERR* to initiate a retry sequence for Motorola 68K processors. See section 1.5.7.

R/W*

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

This is the local data direction signal. This signal is driven while the VIC068A is a local bus master to indicate local data direction. As an input, R/W* indicates data direction for VMEbus master cycles. In this case, the VMEbus signal WRITE* reflects the value of R/W*. A Low condition indicates a write operation.

FC2, FC1

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

These are the local function code signals. These signals identify the type of local cycle in progress. As inputs, they should reflect the type of operations in terms of User/Supervisory Code/Data. They may be connected directly to the Motorola FC2/1 outputs for 68000-30 processors. For the 68040, the FC2/1 inputs may be connected to the TM2/1 outputs, respectively. Additional qualification may be required for 68040 applications because the 68040 uses previously reserved/unused function codes.

FC2	*FC1*	*Description*
0	0	User Data
0	1	User Program
1	0	Supervisor Data
1	1	Supervisor Program

As outputs, the VIC068A drives these signals whenever it is local bus master to indicate the type of local cycle the VIC068A is performing. See section 1.6.3.

FC2	*FC1*	*Description*
0	0	Slave Block Transfer
0	1	Local DMA
1	0	Slave Access
1	1	DRAM Refresh

SIZ1, SIZ0

Input: Yes
Output: Yes, rescinding
Drive: 8 mA

These are the local data size signals. As inputs, these signals identify the width of the VME-bus data to be transferred. The SIZi signals should not be used to indicate the physical port size of the slave device (D16, or D32). This is done with the WORD* signal. As outputs, they are driven by the VIC068A as local bus master to identify the width of the incoming data. See sections 1.5.9, 1.6.5, and 1.6.8.

SIZ1	*SIZ0*	*Data Width*
0	0	Longword
0	1	Byte
1	0	Word
1	1	3-Byte

LBR*

Input: No
Output: Yes
Drive: 8 mA

This is the local bus request signal. This signal is asserted whenever the VIC068A desires mastership of the local bus. This signal remains asserted for the entire bus tenure.

Local bus mastership is requested when each of the following operations is desired:

- Standard slave accesses
- Slave block transactions
- Block transfers with local DMA
- DRAM refresh

LBG*

Input: Yes
Output: No
Drive: None

This is the local bus grant signal. The signal is asserted by local resources in response to the LBR* signal. The VIC068A does not incorporate a local-bus-grant-acknowledge protocol, so the LBG* signal must remain asserted for the duration of LBR*.

MWB*

Input: Yes
Output: No
Drive: None

This is the "Module-Wants-Bus" signal. This signal is asserted by local resources to begin a VMEbus transaction. When qualified by the PAS* signal, the VIC068A asserts the VMEbus BRi* signal. This signal is usually asserted by local-to-VMEbus address decoders.

FCIACK*

Input: Yes
Output: No
Drive: None

This is the local interrupt acknowledge signal. This signal is asserted (qualified by PAS*) to acknowledge all VIC068A-generated local interrupts. See Chapter 1.9.

SLSEL1*, SLSEL0*

Input: Yes
Output: No
Drive: None

These are the slave select signals. These signals indicate the VIC068A has been selected to perform a VMEbus slave operation. When qualified by AS* and valid AM codes, the

VIC068A requests the local bus to perform the slave cycle. These signals are usually asserted by VMEbus-to-local-address decoders.

The SLSEL1/0 signals may be used independently of each other to provide unique slave characteristics as defined by the Slave Select Control registers. See section 1.6.1.

ICFSEL*

Input: Yes
Output: No
Drive: None

This is the Interprocessor Communication Facility (ICF) Select signal. This signal indicates that the ICF functions of the VIC068A have been selected. These include the ICF registers and the ICF switch interrupts. This signal is qualified with AS* and A16 AM codes (A16/Supervisory for global switches). See Chapter 1.8.

ASIZ1, ASIZ0

Input: Yes
Output: No
Drive: None

These are the VMEbus address size signals. These signals are driven to indicate the VMEbus address size of master VMEbus transfers. The address size information is issued on the VMEbus AM codes. User-defined address spaces may be accessed by asserting both ASIZ1/0 signals. In this case, the AM codes are issued according to the programming of the Address Modifier Source register.

ASIZ1	*ASIZ0*	*Address Size*
0	0	User defined
0	1	A32
1	0	A16
1	1	A24

WORD*

Input: Yes
Output: No
Drive: None

This is the VMEbus data width control signal. This signal, when asserted, indicates the requested VMEbus transaction should be treated as a D16 data path. When deasserted, the

VMEbus data path is assumed to be D32. This signal should be used to configure VMEbus data width for master cycles only. Data width for slave cycles is configured in the Slave Select Control registers.

This signal is also used to configure the data width for block transfers with local DMA. When this signal is asserted during the block transfer initiation cycle, the block transfer is assumed to be a D16 block transfer.

This signal may be changed dynamically for individual transfers, or strapped Low at power-up for permanent D16 operation. If WORD* is strapped Low at power-up, the VIC068A is configured as a D16 slave, independent of the slave configuration in the Slave Select Control registers.

WORD* should not be used to indicate data size (i.e., byte, word, or longword) only VMEbus data port size (i.e., D16 or D32).

BLT*

Input: Yes
Output: Yes, open collector
Drive: 8 mA

This is the block transfer with local DMA indication signal. This signal is used to indicate that a block transfer with local DMA is in progress. This signal remains asserted for the entire block transfer including interleave periods with the exception of local page boundary crossings. BLT* toggles during local boundary crossings to increment the external LA[+:8] counters. See section 1.10.1.1.

DEDLK*

Input: No
Output: Yes
Drive: 8 mA

This is the deadlock indication signal. This signal indicates that a deadlock condition has occurred. This signal should be used by local logic to remove its request for the VMEbus. DEDLK* remains asserted until the slave transaction is complete.

DEDLK* is also asserted to indicate that a VMEbus master cycle is being attempted during the interleave period of a block transfer with local DMA, without the dual-path feature enabled. In this case, DEDLK* is asserted while MWB* is asserted. If, during the interleave

period, the MWB* signal is asserted after the VMEbus has been re-obtained, the VIC068A will assert DEDLK* for the duration of the burst. See section 1.5.7.

IPL2, IPL1, IPL0

Inputs: IPL0 only
Output: Yes, open collector
Drive: 8 mA

These are the local priority encoded interrupt request signals. These signals are asserted to interrupt the local processor. All local VIC068A interrupts are issued with these signals. These signals emulate the Motorola 68K interrupt mechanism. The assertion of one or more of these signals indicates a single interrupt with a priority given by the negative-logic value of the IPLi signals. Level 7 is the highest priority. These signals are open collector to allow the wire-ORing of multiple interrupt sources. See Chapter 1.9.

During the assertion of IRESET*, IPL0 becomes an input. If IPL0 is asserted at this time, a global reset is performed. See section 1.11.1.2.

LIRQ7* – LIRQ1*

Input: Yes
Output: LIRQ2* only
Drive: 8 mA (LIRQ2* only)

These are the local interrupt request signals. These signals serve as local interrupt request signals for the VIC068A. If enabled to handle the particular local interrupt, the VIC068A issues a processor interrupt with the IPLi signals at the assertion of a LIRQi*. Configuration of local interrupts is allowed through the Local Interrupt Configuration registers. See section 1.9.3.

LIRQ2* may also be configured to issue periodic "heartbeat" interrupts at user-defined intervals. See section 1.9.6.

LIACKO*

Input: No
Output: Yes
Drive: 8 mA

This is the "autovectoring" indication signal. This signal is asserted when the VIC068A is configured to allow the interrupting device to place its status/ID vector on the local data bus

in response to a VIC068A-handled local interrupt acknowledge. This signal may be used to signal an autovectored interrupt acknowledge cycle for 68020/30/40 processors. This signal may be connected directly to the AVEC signal for these processors. See section 1.9.3.

IRESET*

Input: Yes
Output: No
Drive: None

This is the internal reset signal. This signal is used to issue both internal and global resets to the VIC068A. If asserted with IPL0*, a global reset is performed. If asserted without IPL0*, an internal reset is performed. All internal state machines and selected register bits are reset during the assertion of IRESET*. HALT* and RESET* are both asserted during the assertion of IRESET*. If configured as system controller, SYSRESET* is also asserted during the assertion of IRESET*. See Chapter 1.12.

SCON*

Input: Yes
Output: No
Drive: None

This is the system controller enabling signal. This signal is used to configure the VIC068A as VMEbus system controller. This signal must be strapped Low at power-up and remain Low for VIC068A to reliably assume the role of VMEbus system controller, otherwise this signal should be tied High. See Chapter 1.4.

CLK64M

Input: Yes
Output: No
Drive: None

This is the VIC068A master clock input. This 64-MHz clock input is used to clock internal arbitration, timing, and delay functions within the VIC068A. Clock speeds as low as 1 MHz may be used, but all synchronous delays as well as VMEbus and local timing are affected.

RMC*

Input: Yes
Output: No
Drive: None

This is the Read-Modify-Write control signal. This signal may be used to control indivisible cycles on the VMEbus. Its operation is controlled with the Interface Configuration register, bits 5−7. See section 1.5.6.

1.2.3 Buffer Control Signals

These signals control the latching and enabling of the external address and data latches and buffers. For block transfers with local DMA, some of these signals are used to control the counting and enabling of external counters required for page boundary crossing. These signals can be directly connected to Cypress CY7C964s which simplifies the VME interface by replacing 8 bit wide external latches, buffers and counters with one CY7C964. A complete 32 bit wide VME interface would consist of the VIC068A and three CY7C964s. See Section 4, The CY7C964 Bus Interface Logic Circuit, for more information.

For simple VME designs (i.e. single-cycle only) the VIC068A can directly drive the control lines of discrete buffers and latches (*Figure 1−4).*

Figure 1−4 shows typical connections between the external latches/buffers and the buffer control signals.

ABEN*

Input: No
Output: Yes
Drive: 8 mA

This is the VMEbus Address Bus ENable signal. This signal is used to enable the external VMEbus address drivers for VMEbus master operations. It is typically connected to the OEAB input of a ’543 address transceiver.

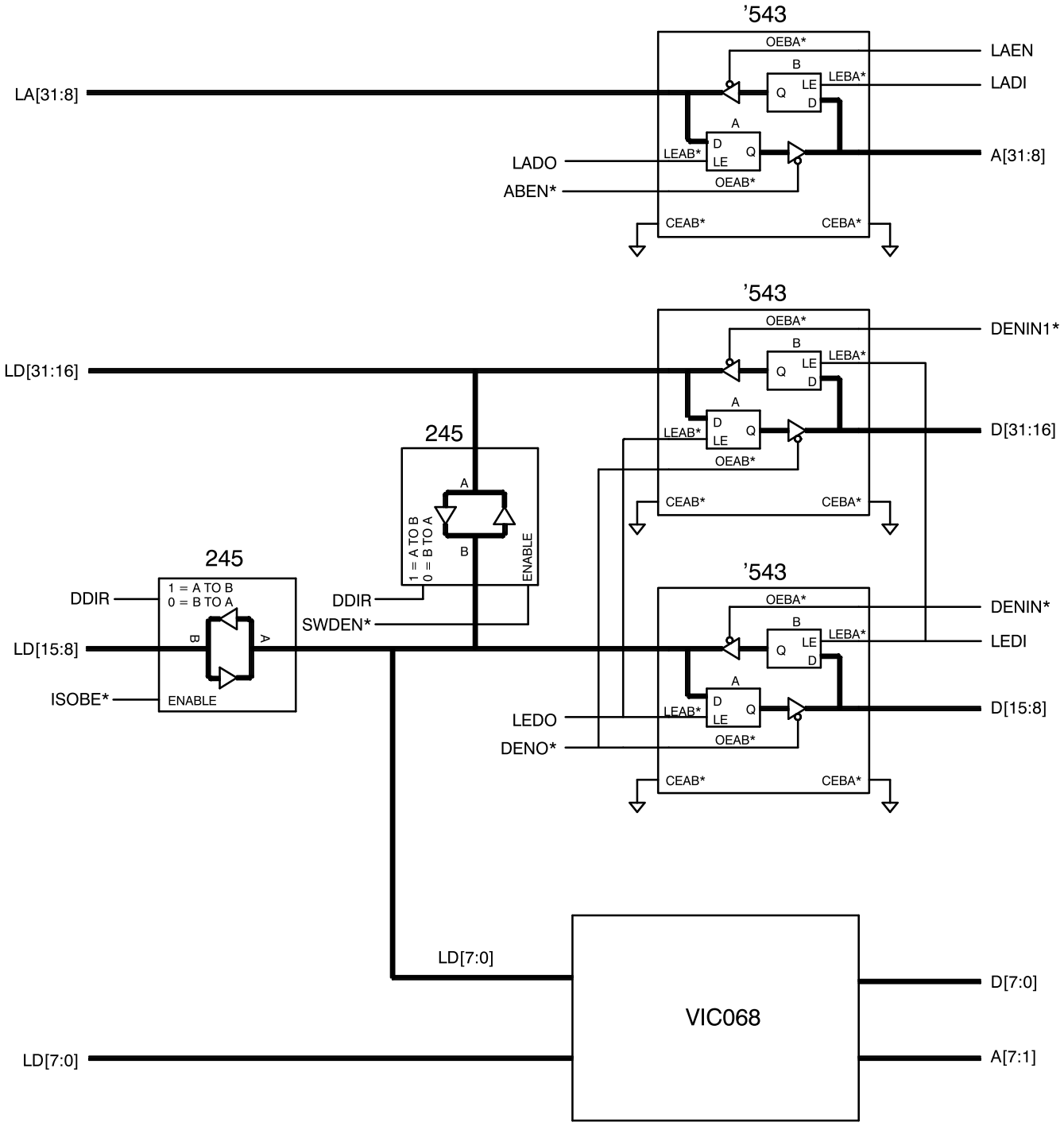

Figure 1−4. VIC068A Control Signals for Shared Memory Implementation

LAEN

Input: No
Output: Yes
Drive: 8 mA

This is the Local Address ENable signal. This signal is used to enable the external local address drivers for slave accesses. It is typically connected to the OEBA input of a ’543 address transceiver through an inverter.

Note that this signal is an active-High signal.

LADO

Input: No
Output: Yes
Drive: 8 mA

This is the Latch ADdress Out signal. This signal is used to latch the outgoing VMEbus address for VMEbus master operations. When this signal is asserted (High), it is assumed that the latches are in a latched state. When deasserted, the latches should be in a flow-through state. This allows direct connection to the ’543 address driver LEAB input. LADO is very important for proper operation of master write posting and block transfers with interleave periods. For these operations, the VIC068A may use LADO in combination with LADI and ABEN* to temporarily store the contents of a VMEbus address during intervening slave accesses.

LADI

Input: No
Output: Yes
Drive: 8 mA

This is the Latch ADdress In signal. This signal is used to latch the incoming VMEbus address for slave accesses. When this signal is asserted (High), it is assumed that the latches are in a latched state. When deasserted, the latches should be in a flow-through state. This allows direct connection to the ’543 address driver LEBA input. LADI is used in conjunction with LADO to temporarily store outgoing VMEbus master transaction addresses during intervening slave accesses.

DENO*

Input: No
Output: Yes
Drive: 8 mA

This is the Data ENable Out signal. This signal enables data onto the VMEbus data bus for master write and slave read cycles. This signal is typically connected to the OEAB input of the ’543 data latches.

DENIN* (formerly LWDENIN*)

Input: No
Output: Yes
Drive: 8 mA

This is the Lower Word Data ENable IN signal. This signal enables data onto the lower word of the local data bus LD[15:8] for master read and slave write cycles. This signal is typically connected to the OEBA input of the ’543 lower data latch.

DENIN1* (formerly UWDENIN*)

Input: No
Output: Yes
Drive: 8 mA

This is the Upper Word Data ENable IN signal. This signal enables data onto the upper word of the local data bus LD[31:16] for master read and slave write cycles. This signal is typically connected to the OEBA input of the upper ’543 data latches.

LEDO

Input: No
Output: Yes
Drive: 8 mA

The Latch Enable Data Out signal. This signal latches the outgoing VMEbus data for master write and slave read cycles. When this signal is asserted (High), it is assumed that the latches are in a latched state. When deasserted, the latches should be in a flow-through state. This allows direct connection to the ’543 address driver LEAB input. This signal may be used in conjunction with LEDI to temporarily store outgoing master write post data (data switchback).

LEDI

Input: No
Output: Yes
Drive: 8 mA

This is the Latch Enable Data In signal. This signal latches the incoming VMEbus data for master read and slave write cycles. When this signal is asserted (High), it is assumed that the latches are in a latched state. When deasserted, the latches should be in a flow-through state. This allows direct connection to the ’543 address driver LEBA input. This signal may be used in conjunction with LEDO to temporarily store outgoing master write post data.

ISOBE*

Input: No
Output: Yes
Drive: 8 mA

This is the ISOlation Buffer Enable signal. This signal, along with the SWDEN* signal, steers data from LD[31:16] to/from LD[15:0], which is referred to in this document as byte-lane switching. This signal is typically connected to the EN input of the ’245 isolation buffer.

SWDEN*

Input: No
Output: Yes
Drive: 8 mA

This is the SWap Data ENable signal. This signal, along with the ISOBE* signal, provides byte-lane switching. It provides for swapping LD[31:16] to LD[15:0]. This signal is typically connected to the EN input of the ’245 swap buffer.

DDIR

Input: No
Output: Yes
Drive: 8 mA

This is the Data DIRection signal. This signal provides the data direction (i.e., read/write) information to the isolation and swap buffers. When asserted, buffers should be configured in the local-to-VMEbus (A-to-B) direction. This signal is typically connected to the DIR input of the ’245 isolation/swap buffers.