Cypress Semiconductor
Product Reliability
1996

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CYPRESS SEMICONDUCTOR

QUALITY POLICY

It is the intent of Cypress Semiconductor Corporation to provide product and services on time, at competitive costs, with zero defects.

1.0 OVERVIEW OF CYPRESS SEMICONDUCTOR TOTAL QUALITY MANAGEMENT SYSTEM

This report summarizes Cypress Semiconductor Product Reliability for the period of January 1, 1995 through December 31, 1995. Cypress Semiconductor has established aggressive reliability objectives to assure that all products exhibit reliability which exceeds customer reliability requirements for purchased components. In addition, the quality standard at Cypress is zero defects which results in a culture requiring continuous improvement in quality and reliability. This report includes data from product fabricated at the San Jose, California; Round Rock, Texas; and Bloomington, Minnesota facilities.

Product reliability is assured by a total quality management system. The quality management system is described in detail in the Cypress Semiconductor Quality Manual (Cypress Semiconductor Document Number 90-00001). Key reliability-related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) manufacturing identification of "Maverick Lot" yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing process; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarking.

Product Reliability data is accumulated as a result of new product Qualification Test Plan activities (Cypress Semiconductor Document Number 25-00040) as well as from the Reliability Monitor Program (Cypress Semiconductor Document Number 25-00008). All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Reliability strategy requires that every failure which occurs during reliability testing is subjected to failure analysis (Cypress Semiconductor Document Number 25-00039) to determine the failure mechanism. Corrective action is then implemented to prevent future failures. The result is continuous improvement in product reliability.

Copies of the Cypress Semiconductor documents referenced herein are available through your Cypress Semiconductor sales representative. Questions about product reliability may be addressed to the undersigned.

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2.0 ELECTRICAL AVERAGE OUTGOING QUALITY

Every lot that leaves Cypress Semiconductor must pass Cypress's Quality Assurance. Although all the tests are important, electrical AOQ is the best measure of the quality a customer receives. The following table summarizes our electrical AOQ measurements. Our ultimate goal is to always supply defect free products to our customers.

Test:	**Electrical Average Outgoing Quality (AOQ)**
Scope:	**All lots are sampled.**
Sample Size:	**For monolithic devices: a minimum of 231 devices.**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements. A Materials Reviews Board dispositions all failed lots.**

Table 1: Electrical Average Outgoing Quality for Commercial Products.

Technology Family	1990	1991	1992	1993	1994	1995
BiCMOS	N/A	15	13	56	56	75
FAMOS	387	255	169	57	57	111
FLASH	N/A	N/A	345	119	119	176
SRAM/LOGIC	425	299	128	41	45	44
Overall	414	266	132	48	55	62

HIGH TEMPERATURE OPERATING LIFE:

EARLY FAILURE RATE

3.0 EARLY FAILURE RATE SUMMARY

3.1 Early Failure Rate Determination

High Temperature Operating Life testing (HTOL), for as long as 80 hours, is used to estimate device early failure rate. This stress test will typically correspond to the first 2000 hours of device operation in a system environment. The remainder of the device's lifetime is characterized with extended HTOL testing (See Section 4).

Test:	**High Temperature Operating Life Test (HTOL)**
Conditions:	**Dynamic Operating Conditions, V_{CC} = 5.75 Volts, 150°C or 125°C, *f* = 1 Mhz.**
Duration:	**Early Failure Rate samples are tested between 12 and 80 hours HTOL at 150°C (EFR) or up to 96 hours at 125°C (EFR2).**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements.**

Table 2: Early Failure Rate Summary

Technology	# Devices Tested	# Fails	Failure Mode	Defects (PPM)
BiCMOS	12,954	1	Ionic Contamination	77
FAMOS	7,866	1	Unknown	127
FLASH	8,919	0	---	0
SRAM/LOGIC	45,410	10	1 Photo Defect 1 Ionic Contamination 1 Particle 1 Poly Defect 6 Oxide Defects	220
OVERALL	**75149**	**12**	**See Above**	160

HIGH TEMPERATURE OPERATING LIFE:

LONG-TERM FAILURE RATE

4.0 LONG TERM FAILURE RATE SUMMARY

4.1 Long Term Failure Rate Determination

A High Temperature Operating Life test (HTOL) is used to estimate long term reliability. By operating the devices at accelerated temperature and voltage, hundreds of thousands of use hours can be compressed into hundreds of test hours. The method used to estimate failure rates from stress data is summarized in Appendix A.

Test:	**High Temperature Operating Life Test (HTOL)**
Conditions:	**Dynamic Operating Conditions, V_{CC} = 5.75 Volts, 150°C or 125°C, *f* = 1 Mhz**
Duration:	**A minimum of 168 hours at 150°C or 125°C. Tested to 1000 hours at 150°C or 2000 hours at 125°C.**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements.**

4.0 LONG TERM FAILURE RATE SUMMARY (CONT.)

Table 3: Long Term Failure Rate Summary[1]

Technology	Device Hours[2]	# Fails	Failure Mode	Activation Energy	Acceleration Factor	MTBF[1] (hours)	Failure Rate (FIT)[2]
TOTAL BiCMOS	1,469,140	1	Unknown	0.45	27	19,600,000	51
TOTAL FAMOS	698,223	0	None	0.60	82	62,500,000	16
FLASH	1,161,015	1	Particle	0.70	170	100,000,000	10
FLASH	1,161,015	1	Fab Defect	0.45	27	15,400,000	65
TOTAL FLASH	1,161,015	2	See Above	---	---	13,300,000	75
SRAM/LOGIC	3,568,870	3	Unknown	0.45	27	23,300,000	43
SRAM/LOGIC	3,568,870	3	Particles	0.70	170	143,000,000	7
TOTAL SRAM/LOGIC	3,568,870	6	See Above	--	--	20,000,000	50
OVERALL	**6,897,248**	**9**	**See Above**	**0.6**	**82**	**52,600,000**	19

[1] Mean Time Between Failures, See Appendix A

[1] Chi-squared 60% estimations used to calculate the failure rate. Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

[2] Equivalent Device Hours at 150°C, see Appendix C

4.0 LONG TERM FAILURE RATE SUMMARY (CONT.)

Device reliability is highly dependant on temperature. Cooler system environments invariably result in more reliable systems. This fact is illustrated below in Table 4. Depending on the failure mechanism, lowering the box temperature just ten degrees can improve reliability from 60% to 100%. Even when our devices generate very little heat, close proximity to other hot running units can decrease its reliability. Thermodynamic laws cannot be circumvented. Good system reliability requires good thermal management.

Table 4: Effect of Different Junction Temperature Assumptions on Failure Rates

Technology	Failure Mode	E_A (eV)	Junction Temperature 50°C[4]		Junction Temperature 60°C[4]		Junction Temperature 70°C[3,4]	
			AF	FR (FIT)	AF	FR (FIT)	AF	FR (FIT)
TOTAL BiCMOS	Unknown	0.45	70	20	43	32	27	51
TOTAL FAMOS	None	0.60	287	5	150	9	82	16
FLASH	Particle	0.70	736	2	346	5	170	10
FLASH	Fab Defect	0.45	70	25	43	41	27	65
TOTAL FLASH	See Above	---	---	27	---	46	---	75
SRAM/LOGIC	Unknown	0.45	70	17	43	27	27	43
SRAM/LOGIC	Particles	0.7	736	2	346	3	170	7
TOTAL SRAM/LOGIC	See Above	---	---	19	---	30	---	50
OVERALL	**See Above**	**0.6**	**287**	**5**	**150**	**10**	**82**	19

[3] The junction temperature is approximately equal to ambient temperature plus 15°C.

[4] An assumption of a 70°C junction temperature is used in all other failure rate calculations.

DATA
RETENTION
FAILURE RATE

5.0 PRODUCT FAMILY DATA RETENTION RELIABILITY SUMMARY

5.1 Data Retention Failure Rate Determination

A high-temperature, non-biased bake test ensures that data retention meets established reliability goals. The devices are baked without bias at either 165°C for plastic-packaged devices, or 250°C for hermetically-packaged devices.

Test:	**Data Retention Testing**
Conditions:	**High Temperature Non-biased Bake**
Purpose:	**High Temperature Non-biased Bake is performed on programmed devices to establish a failure rate for cell charge loss. The reliability at nominal system ambient temperature is related to the failure rate at elevated temperatures through the Arrhenius equation.**
Duration:	**Minimum of 168 hours; tested to 1000 hours.**
Failure:	**Devices are programmed with a worst case program pattern before being subjected to data retention testing. The memory pattern is verified at each read point and any device with altered bits is classified a failure.**

5.0 PRODUCT FAMILY DATA RETENTION RELIABILITY SUMMARY (CONT.)

Table 5: Data Retention Failure Rate Summary

	Plastic 165°C			Hermetic 250°C		
	Device Hours	# Fails	Failure Rate (FIT)	Device Hours	# Fails	Failure Rate (FIT)
FAMOS	286,300	0	0	38,304	0	0
FLASH	533,520	0	0	21,720	0	0
OVERALL	819,820	0	0	60,024	0	0

HIGH TEMPERATURE
STEADY STATE LIFE TEST

6.0 HIGH TEMPERATURE STEADY STATE LIFE TEST

6.1 High Temperature Steady State Life Test Failure Rate Determination

The High Temperature Steady State Life test (HTSSL) is used primarily to accelerate ionic contamination problems. Static bias is used because a constant voltage gradient accelerates diffusion of ionic species. The method used to estimate failure rates from stress data is summarized in Appendix A.

Test:	**High Temperature Steady State Life Test (HTSSL)**
Conditions:	**Static Operating Conditions, 125°C or 150°C, VCC=5.75 V.**
Duration:	**A minimum of 168 hours at 150°C, tested to 1000 hours. A minimum of 336 hours at 125°C, tested to 2000 hours.**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements.**

Table 6: High Temperature Steady State Life Test

Technology	Device Hours[1]	Failures	Failure Mode	Activation Energy (eV)	Failure Rate (FIT)
BiCMOS	259,289	1	Unknown	0.45	143
BiCMOS	259.289	1	Topside Cracks	1.3	0.3
Total BiCMOS	259,289	2	See Above	---	143
Total FAMOS	233,107	0	None	0.60	0
FLASH	184,319	1	Broken Bond	0.45	201
FLASH	184,319	1	Particle	0.70	32
Total FLASH	184,319	2	See Above	---	233
SRAM/LOGIC	655,550	1	Ionic Contamination	1.2	0.2
SRAM/LOGIC	655,550	1	Unknown	0.45	56
SRAM/LOGIC	655,550	1	Particle	0.70	9
Total SRAM/LOGIC	655,550	3	See Above	---	65
OVERALL	**1,332,265**	**7**	**See Above**	**0.60**	**64**

[1] Equivalent Device Hours at 150°C, see Appendix C

PROCESS

ENVIRONMENTAL TESTS

7.0 PROCESS ENVIRONMENTAL TESTS

Cypress Semiconductor Reliability qualifies and continuously monitors packaging reliability to ensure exceptional resistance to environmental stress. Package reliability stress testing and failure rates are summarized in the following section.

7.1 Pressure Cooker Test (PCT)

Test:	**Pressure Cooker Test (PCT)**
Conditions:	**15 PSIG, 121°C, No bias, for a minimum of 168 hours.**
Purpose:	**The Pressure Cooker Test is a highly accelerated packaging stress test used to ensure environmental durability of epoxy packaged parts. Passivation cracks, ionic contamination and corrosion susceptibility are all accelerated by this stress.**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements.**

Table 7: Pressure Cooker Test Failure Rate Summary

Technology	Device Hours	# Fails	Failure Mode	Failure Rate (FIT)
BiCMOS	70,392	0	None	0
FAMOS	78,384	0	None	0
FLASH	141,168	0	None	0
SRAM/LOGIC	488,064	5	Oxide Defects	1
OVERALL	**778,008**	**5**	**See Above**	1

See Appendix A for acceleration factor and failure rate calculation.

7.0 PROCESS ENVIRONMENTAL TESTS (CONT.)

7.2 Highly Accelerated Stress Test (HAST)

Cypress uses HAST to accelerate temperature, humidity, bias failure mechanisms. This change was necessary because our package reliability had improved to the point where the old 85°C/85% R.H. temperature-humidity-bias testing would not induce failures. Failures are necessary to judge progress and compare packaging changes. HAST testing has been shown to be at least twenty times more accelerated then 85°C/85% R.H. temperature-humidity-bias testing. HAST acceleration factor information can be found in Appendices A, C, and E.

Test:	**Highly Accelerated Stress Test (HAST)**
Conditions:	**Present Conditions: 140°C / 85% RH /5.5 V bias, or 130°C / 85% R.H. / 5.5 V bias, for a minimum of 128 hours.**
Pre-Conditioning:	**For DIPs: 40 Temperature Cycles (-65 - 150°C)** **For SMDs: 48 hours of Pressure Cooker (121°C/100% R.H.) followed by solder reflow simulation.**
Purpose:	**HAST is an accelerated biased humidity test that provides an acceleration of at least 10 over 85°C/85% R.H. temperature-humidity bias testing. This test provides rapid feedback regarding the quality of the epoxy package process.**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements.**

7.0 PROCESS ENVIRONMENTAL TESTS (CONT.)

Table 8: Highly Accelerated Stress Test (HAST) Failure Rate Summary

Technology	Device Hours[1]	# Fails	Failure Mode	Failure Rate (FIT)
BiCMOS	59,512	0	None	0
FAMOS	110,129	2	Topside Cracks	1
FLASH	80,991	1	Topside Cracks	1
SRAM/LOGIC	557,555	10	3 Particles 1 Poly Defect 3 Topside Cracks 3 Oxide Defects	1
OVERALL	**808,187**	**13**	**See Above**	**1**

[1] Equivalent Device Hours at 150°C, see Appendix C

For further information on HAST versus 85°C/85% R.H. acceleration factor, see Appendix E.

7.0 PROCESS ENVIRONMENTAL TESTS (CONT.)

7.3 Temperature Cycle Test (TC)

Differences in thermal expansion coefficients are accentuated by cycling devices through temperature extremes. If the materials do not expand and contract equally, large stresses can develop. Because the relation between stress cycles and use cycles is not well quantified, Cypress Reliability undertook an investigation to calculate wire bond breakage temperature cycling acceleration factors. See Appendix B and D.

Test:	**Temperature Cycle**
Conditions:	**MIL-STD-883D, Method 1010, Condition C, -65°C to 150°C JEDEC 22-A104 Condition B, -40°C to 125°C**
Pre-Condition:	**For SMDs: 48 hours of Pressure Cooker (121°C/100%RH) follow by solder reflow simulation.**
Purpose:	**The Temperature Cycle test stresses mechanical integrity by exposing a device to alternating temperature extremes. Weakness and thermal expansion mismatches in die interconnections, die attach, and wire bonds are often detected with this acceleration test.**
Duration:	**100 cycles minimum, tested to 1000 cycles.**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements.**

7.0 PROCESS ENVIRONMENTAL TESTS (CONT.)

Table 9: Temperature Cycling Failure Rate Summary

Technology	# Device-Test Cycles[1]	# Fails	Failure Mode	Failure Rate (FIT)
BiCMOS	1,063,256	5	Topside Cracks	4
FAMOS	1,137,230	27	Topside Cracks	20
FLASH	706,506	2	Broken Bond Wires	0
SRAM/LOGIC	3,940,452	21	16 Topside Cracks 1 Particle 4 Oxide Defects	5
OVERALL	**6,847,444**	**55**	**See Above**	**7**

[1] Device-Test Cycles based on (-65 to 150°C) condition. See Appendix B and C.
[2] See Appendix B.

8.0 OVERALL FAILURE RATE SUMMARY

The reliability failure rates are summarized in the following table.

Table 10: Life Time Failure Rate Summary

	FAILURE RATE (FIT)					
	RELIABILITY STRESS TEST					
	HTOL	HTSSL	DRET	PCT	HAST	TC
BiCMOS	51	143	---	0	0	4
FAMOS	16	0	0	0	1	20
FLASH	75	233	0	0	1	0
SRAM/LOGIC	50	65	---	1	1	5
OVERALL	**19**	**64**	**0**	**1**	**1**	**7**

ADDITIONAL RELIABILITY RELATED STRESS TESTING

9.0 ADDITIONAL RELIABILITY RELATED STRESS TESTING SUMMARY

Cypress products require superior resistance to hot carriers, latch-up, electrostatic discharge, and soft errors caused by alpha particle penetration.

9.1 Low Temperature Operating Life (LTOL)

Test:	**Low Temperature Operating Life (LTOL)**
Conditions:	**Dynamic bias, V_{CC} = 6.5 V, -45°C, f = 1 MHz, 1000 hrs.**
Purpose:	**LTOL studies are done to monitor Hot carrier-induced product degradation. All of Cypress products are built using high performance Lightly Doped Drain (LDD) structures that have been designed to minimize hot carrier effects. The parameters monitored to check for device degradation are T_{AA} and T_{ACS}.** **Characterization is done at 25°C and $V_{cc,nominal}$.**

9.0 ADDITIONAL RELIABILITY RELATED STRESS TESTING SUMMARY (CONT.)

Table 11: Low Temperature Operating Life Test Results

Technology	Device Hours	# Fails	Failure Mode	Failure Rate (FIT)
BiCMOS	143,000[1]	0	None	0
FAMOS	151,548	0	None	0
FLASH	48,000	0	None	0
SRAM/LOGIC	90,000	0	None	0
OVERALL	432,548	0	None	0

[1] 1994 Data.

9.0 ADDITIONAL RELIABILITY RELATED STRESS TESTING SUMMARY (CONT.)

9.2 Latch-up Sensitivity

Test:	**Latch-up Sensitivity**
Conditions:	**In accordance with JEDEC 17. Positive injection at 8.0 V, Negative injection at -5.0 V, DC Pre V_{CC} and DC Post V_{CC} tests, Power Supply Overvoltage test at 8 V, Test temperature = 125°C.**
Purpose:	**The Latch-up test is designed to test the resistance of the devices to extreme voltage and current excursions.**
Failure:	**A devices fails if after testing I_{CC} has increased more than 200 mA above the quiescent value.**

Results: All products are tested for latch-up during qualification.

(a) Outputs: All outputs are tested using a hot socket technique where the full voltage is applied on a voltage ramp, where voltage is increased slowly. During the hot socket technique, a maximum of 200 mA was allowed in order to protect the outputs from overstress.

(b) Inputs: All inputs are tested using both the hot socket technique and the voltage ramp technique.

Conclusion: Cypress Semiconductor products are very resistant to Latch-up. A customer need take no special precautions in the design of a system incorporating Cypress products.

9.0 ADDITIONAL RELIABILITY RELATED STRESS TESTING SUMMARY (CONT.)

9.3 Electrostatic Discharge (ESD)

Test:	**Electrostatic Discharge (ESD)**
Conditions:	**Human Body Model (HBM) MIL-STD-883D, Method 3015.7** **Charged Device Model (CDM) Cypress Spec. 25-00020**
Purpose:	**To establish the ESD sensitivity of a devices.**
Failure:	**A failure is any device that fails to meet data sheet electrical requirements after ESD testing.**

Classification (HBM)[5]: Military Class 1: 0 - 1999 V
Military Class 2: 1999 - 3999 V
Military Class 3: 4000 and above

Procedures (HBM): For every pin, a positive and negative pulse is applied between (1) the pin and ground, (2) the pin and V_{CC}, and (3) the pin and all other pins tied together.

Procedures (CDM): Each pin is capacitively charged and discharged five times through a pogo probe at positive and negative voltages.

Results: A table of device names and ESD-HBM and ESD-CDM classification can be found in Appendix I.

Conclusion: Cypress products are not ESD sensitive. A customer should exercise normal care in handling all semiconductor products.

[5] There is currently no Military or JEDEC ESD-CDM specification. Cypress requires that corner pins pass CDM testing at 1000 V and all other pins to pass at 500 V.

9.0 ADDITIONAL RELIABILITY RELATED STRESS TESTING SUMMARY (CONT.)

9.4 Alpha Particle Sensitivity (Accelerated Soft-Error) Stress Testing

Test:	**Alpha Particle Sensitivity (Accelerated soft-error) Stress Testing**
Conditions:	**A 0.1 µCurie Thorium-232 Alpha Particle source is used for accelerated soft-error rate testing. The source is placed 2 mm above the die surface and directly over the array. The device is continually exercised in a write/read CKBD/CKBD-BAR test mode. Devices are typically evaluated at $V_{cc,min}$ at a cycle time of 128 ns.**
Purpose:	**This is a highly accelerated test that utilizes a radioactive source to provide an accelerated method of evaluating the alpha sensitivity of Cypress Static RAM products.**
Failure:	**The number of failures are defined as the number of bits that change states during radiation stress testing.**

9.0 ADDITIONAL RELIABILITY RELATED STRESS TESTING SUMMARY (CONT.)

9.4 Alpha Particle Sensitivity (Accelerated soft-error) Stress Testing (cont.)

Results: For our first and second generation products, organic die coating or low alpha particle mold compounds are often used to reduce alpha particle penetration. Our third generation, six transistor SRAM cell is virtually impervious to alpha particle interruptions and hence requires no additional protection. A summary or our soft-error rate measurements follow.

Table 13: Summary of Soft Error Rate Data

DEVICE FAMILY	TECHNOLOGY SUB-FAMILY	PROJECTED ALPHA PARTICLE INDUCED SER[1]
1k TO 4k SRAM	CMOS	50 FIT
4k SRAM	ECL	10 FIT
16k SRAM	CMOS	80 FIT
64k SRAM	CMOS	190 FIT
64k SRAM	BICMOS	10 FIT
256k SRAM	CMOS	200 FIT
1 M SRAM	CMOS	200 FIT
SRAMs	CMOS Third Generation	0 FIT

Conclusion: Cypress Static RAMs are very resistant to alpha particle induced soft errors.

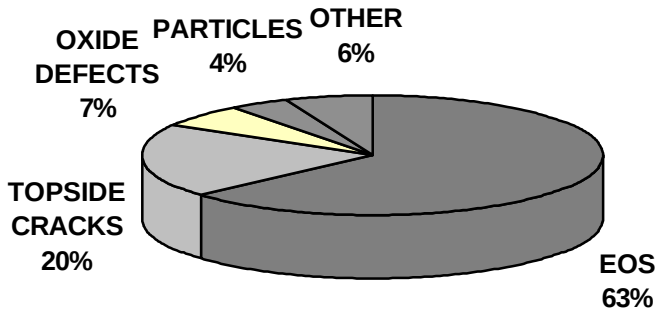
[1]These estimated soft error rates take into account the acceleration factor between the alpha flux rate of the source used for this test and the estimated flux rate from the packaging materials. Die coat contributes less than 0.0001 α/cm^2-hr, but to account for particle flux from chip metallization, a conservative value of 0.001 α/cm^2-hr was used. A non-coated die surrounded by standard mold compound will generally be exposed to an alpha flux rate of 0.1 to 0.01 α/cm^2- hr.

FAILURE MECHANISMS AND CORRECTIVE ACTIONS

10.0 FAILURE MECHANISMS AND CORRECTIVE ACTIONS

Failure Modes and Corrective Actions

Table 14: Summary of 1995 Failure Modes



Failure Mechanism: Electrical Over Stressed (EOS) Devices

- Solution: Improved Burn-In Board Monitoring

EOS failures are indicative of our stress testing procedures, not our product's reliability. These failures, though, decrease throughput and increase failure analysis cycle time. To reduce these failures, we purchased new burn-in boards and have qualified new burn-in subcontractors.

Failure Mechanisms: Topside Cracks

- Solution: Elimination of Dispensed Polyimide Die Coat and Improved Layout Rules

Thin film cracking is caused by high die stresses. By removing the dispensed polyimide die coat used as an alpha barrier on some devices and substituting a low alpha mold compound, we were able to greatly reduce die stresses while still maintaining our good alpha particle immunity. Further improvements were implemented in the design of our products through slotting of large metal buses. No topside cracking failures have been observed since these changes were implemented.

Failure Mechanism: Oxide Defects and Particles.

- Improved Processing and Cleanliness

Our fabs have done an excellent job this year reducing oxide and particle related defects. In the past year, defect densities have been greatly reduced with a corresponding increase in yield and reliability.