Static RAMs

Organization/Density

Density	X1	X4	X4 SIO	X8	X9	X16
4K	7C147 2147	7C123 7C148 7C149 7C150 7C189 7C190 2148 2149	7C122 9122 93422			
16K	7C167A	7C168A 7C169A 7C170A	7C171A 7C172A	7C128A		
64K to 72K	7C187	7C164 7C166	7C161 7C162	7C185 6264	7C182	
256K to 576K	7C197	7C194 7C195 7C196	7C191 7C192	7C199 62256	7C188	7C178* 7C179*
1M	7C107A 7C1007	7C106A 7C1006	7C101A 7C102A 7C1001 7C1002	7C109 7C109A 7C1009		7C1031* 7C1032*

*Synchronous

Up to 4K SRAMs

Size	Organization	Pins	Part Number	Speed (ns)	Packages
64	16 x 4—Inverting	16	CY7C189	t_{AA} = 15,25	P
64	16 x 4—Non-Inverting	16	CY7C190	t_{AA} = 15, 25	P
64	16 x 4—Inverting	16	CY74S189	t_{AA} = 35	P
64	16 x 4—Inverting	16	CY27S03A	t_{AA} = 25, 35	P
64	16 x 4—Non-Inverting	16	CY27S07A	t_{AA} = 25, 35	P
1K	256 x 4	22	CY7C122	t_{AA} = 15, 25, 35	D, L, P, S
1K	256 x 4	24S	CY7C123	t_{AA} = 7, 9, 10, 12, 15	L, P, V
1K	256 x 4	22	CY9122/91L22	t_{AA} = 25, 35, 45	P
1K	256 x 4	22	CY93422A/93L422A	t_{AA} = 35, 45	L, P
4K	4K x 1—CS Power-Down	18	CY7C147	t_{AA} = 25, 35, 45	P
4K	4K x 1—CS Power-Down	18	CY2147/21L47	t_{AA} = 35, 45, 55	P
4K	1K x 4—CS Power-Down	18	CY7C148	t_{AA} = 25, 35, 45	D, P
4K	1K x 4—CS Power-Down	18	CY2148/21L48	t_{AA} = 35, 45, 55	D, P
4K	1K x 4	18	CY7C149	t_{AA} = 25, 35, 45	D, L, P
4K	1K x 4	18	CY2149/21L49	t_{AA} = 35, 45, 55	D, P
4K	1K x 4—Separate I/O, Reset	24S	CY7C150	t_{AA} = 10, 12, 15, 25, 35	D, P, S

16K SRAMS

Size	Organization	Pins	Part Number	Speed (ns)	Packages
16K	2K x 8—CS Power-Down	24	CY7C128A	t_{AA} = 15, 20, 25, 35, 45, 55	D, L, P, V
16K	2K x 8—CS Power-Down	24	CY6116A	t_{AA} = 20, 25, 35, 45, 55	D, L
16K	2K x 8—CS Power-Down	32	CY6117A	t_{AA} = 20, 25, 35, 45, 55	L
16K	16K x 1—CS Power-Down	20	CY7C167A	t_{AA} = 15, 20, 25, 35, 45	P, V
16K	4K x 4—CS Power-Down	20	CY7C168A	t_{AA} = 15, 20, 25, 35, 45	D, P, V
16K	4K x 4	20	CY7C169A	t_{AA} = 15, 20, 25, 35, 45	P
16K	4K x 4—Output Enable	22S	CY7C170A	t_{AA} = 15, 20, 25, 35, 45	P, V
16K	4K x 4—Separate I/O	24S	CY7C171A	t_{AA} = 15, 20, 25, 35, 45	P
16K	4K x 4—Separate I/O	24S	CY7C172A	t_{AA} = 15, 20, 25, 35, 45	D, P

Note: Please contact a Cypress Representative for product availability.

Static RAMs (continued)

64K to 72K SRAMs

Size	Organization	Pins	Part Number	Speed (ns)	Packages
64K	8K x 8—CS Power-Down	28S	CY7C185/185A	t_{AA} = 15, 20, 25, 35, 45	D, L, P, V
64K	8K x 8—CS Power-Down	28	CY7C186/186A	t_{AA} = 15, 20, 25, 35, 45	D, P
64K	64K x 1—CS Power-Down	22S	CY7C187/187A	t_{AA} = 15, 20, 25, 35, 45	D, P, V
64K	16K x 4—Separate I/O, Transparent Write	28	CY7C161/161A	t_{AA} = 15, 20, 25, 35, 45	D, P, V
64K	16K x 4—Separate I/O	28	CY7C162/162A	t_{AA} = 15, 20, 25, 35, 45	L, P, V
64K	16K x 4—CS Power-Down	22	CY7C164/164A	t_{AA} = 15, 20, 25, 35, 45	D, P, V
64K	16K x 4—Output Enable	24	CY7C166/166A	t_{AA} = 15, 20, 25, 35, 45	P, V
72K	8K x 9	28	CY7C182	t_{AA} = 25, 35, 45, 55	P, V

256K to 576K SRAMs

Size	Organization	Pins	Part Number	Speed (ns)	Packages
256K	32K x 8—CS Power-Down	28	CY7C198	t_{AA} = 25, 35, 45	L, P
256K	32K x 8—CS Power-Down	28S	CY7C199	t_{AA} = 12, 15, 20, 25, 35, 45, 55	D, L, P, V, Z
256K	32K x 8—CS Power-Down (3.3V)	28S	CY7C1399	t_{AA} = 15, 20, 25	P, V
256K	64K x 4—CS Power-Down	24	CY7C194	t_{AA} = 12, 15, 20, 25, 35, 45	D, P, V
256K	64K x 4—CS Power Down with OE	28	CY7C196	t_{AA} = 12, 15, 20, 25, 35, 45	L, P, V
256K	64K x 4—Separate I/O, Transparent Write	28	CY7C191	t_{AA} = 12, 15, 20, 25, 35, 45	D, P
256K	64K x 4—Separate I/O	28	CY7C192	t_{AA} = 12, 15, 20, 25, 35, 45	D, P, V
256K	64K x 4—CS Power-Down w/ OE	28	CY7C195	t_{AA} = 12, 15, 20, 25, 35	D, L, P, V
256K	256K x 1—CS Power-Down	24	CY7C197	t_{AA} = 12, 15, 20, 25, 35, 45	D, P, V
256K	32K x 8—Synchronous	28	CY7C193	t_{AA} = 20, 22	V
288K	32K x 9—CS Power-Down	32	CY7C188	t_{AA} = 15, 20, 25, 35	V
576K	32K x 18—Burst	52	CY7C178	t_{CDV} = 8, 10, 12 (@ 0 pF)	J, N
576K	32K x 18—Burst	52	CY7C179	t_{CDV} = 8, 10, 12 (@ 0 pF)	J, N

1M SRAMs

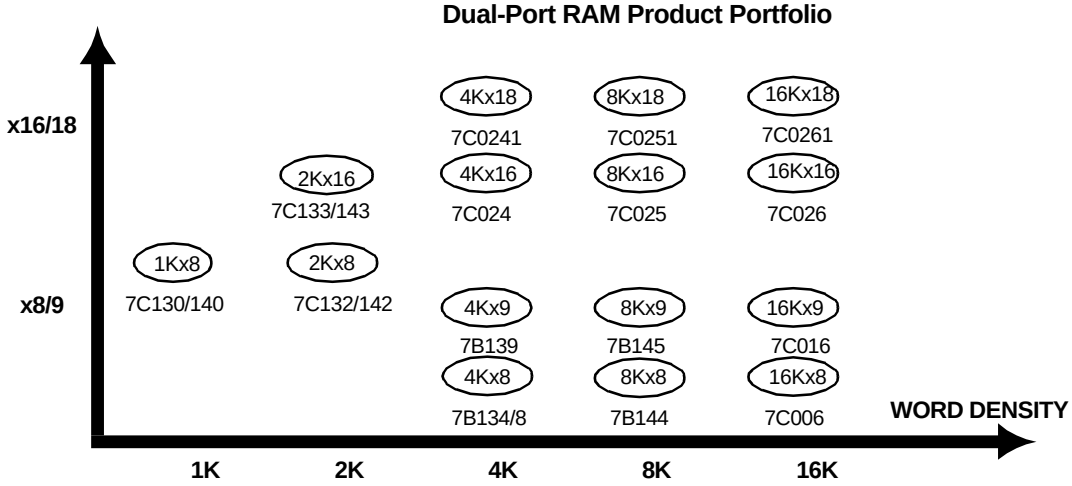
Size	Organization	Pins	Part Number	Speed (ns)	Packages
1M	64K x 18—Burst	52	CY7C1031	t_{CDV} = 8, 10, 12 (@ 0 pF)	J, N
1M	64K x 18—Burst	52	CY7C1032	t_{CDV} = 8, 10, 12 (@ 0 pF)	J, N
1M	64K x 18—Burst (3.3V)	52	CY7C1331	t_{CDV} = 12, 16, 19 (@ 0 pF)	J, N
1M	64K x 18—Burst (3.3V)	52	CY7C1332	t_{CDV} = 12, 16, 19 (@ 0 pF)	J, N
1M	128K x 8—CS Power-Down	32	CY7C1009	t_{AA} = 12, 15, 20, 25	D, L, P, V
1M	128K x 8—CS Power-Down	32	CY7C109A	t_{AA} = 12, 15, 20, 25, 35	D, L, P, V
1M	256K x 4—CS Power-Down	28	CY7C1006	t_{AA} = 12, 15, 20, 25	D, P, V
1M	256K x 4—CS Power-Down w/ OE	28	CY7C106A	t_{AA} =12, 15, 20, 25, 35	D, P, V
1M	256K x 4—Separate I/O, Transparent Write	32	CY7C1001	t_{AA} = 12, 15, 20, 25	D, P, V
1M	256K x 4—Separate I/O, Transparent Write	32	CY7C101A	t_{AA} = 12, 15, 20, 25, 35	D, P, V
1M	256K x 4—Separate I/O	32	CY7C1002	t_{AA} = 12, 15, 20, 25	D, P, V
1M	256K x 4—Separate I/O	32	CY7C102A	t_{AA} = 12, 15, 20, 25, 35	D, P, V
1M	1M x 1—CS Power-Down	28	CY7C1007	t_{AA} = 12, 15, 20, 25	D, P, V
1M	1M x 1—CS Power-Down	28	CY7C107A	t_{AA} =12, 15, 20, 25, 35	D, P, V

Note: Please contact a Cypress Representative for product availability.

Dual-Port RAMs

- Two ports for independent, asynchronous read and write operations
- Variety of bus widths
  - x8, x9, x16, x18 (all expandable)
- 15 ns access time
- Various arbitration schemes available
  - Busy
  - Interrupt
  - Semaphore
- TQFP/PQFP packaging available on all densities

Dual-Port RAM Product Portfolio



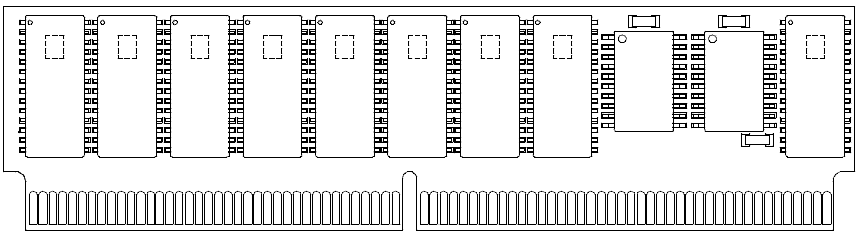
Dual-Port RAMs

Size	Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ ns)	Packages
8K	1K x 8—Dual-Port Master	48	CY7C130	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
8K	1K x 8—Dual-Port Slave	48	CY7C140	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
8K	1K x 8—Dual-Port Master	52	CY7C131	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
8K	1K x 8—Dual-Port Slave	52	CY7C141	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
16K	2K x 8—Dual Port Master	48	CY7C132	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
16K	2K x 8—Dual-Port Slave	48	CY7C142	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	D, P
16K	2K x 8—Dual-Port Master	52	CY7C136	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
16K	2K x 8—Dual-Port Slave	52	CY7C146	t_{AA} = 25, 30, 35, 45, 55	170 @ 25	J, L, N
32K	4K x 8—Dual-Port, No Arbitration	48	CY7B134	t_{AA} = 20, 25, 35, 55	240 @ 20	D, L, P
32K	4K x 8—Dual-Port, w/Semaph	52	CY7B1342	t_{AA} = 20, 25, 35, 55	240 @ 20	J
32K	2K x 16—Dual-Port Slave	68	CY7C143	t_{AA} = 15, 25, 35, 55	170 @25	J,A
32K	2K x 16—Dual-Port Master	68	CY7C133	t_{AA} = 15, 25, 35, 55	170 @ 25	J,A
32K	4K x 8—Dual-Port, w/ Semaph, Busy, Int	64, 68	CY7B138	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
32K	4K x 8—Dual-Port, No Arbitration	52	CY7B135	t_{AA} = 20, 25, 35, 55	240 @ 20	J, L
32K	4K x 9—Dual-Port, w/ Semaph, Busy, Int	68, 80	CY7B139	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
64K	8K x 8—Dual-Port, w/ Semaph, Busy, Int	64, 68	CY7B144	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
64K	8K x 9—Dual-Port, w/ Semaph, Busy, Int	68, 80	CY7B145	t_{AA} = 15, 25, 35, 55	260 @ 15	J, L, A
64K	4K x 16—Dual-Port, w/ Semaph, Busy, Int	84, 100	CY7C024	t_{AA} = 15, 25, 35, 55	280 @ 15	J,A
64K	4K x 18—Dual-Port, w/ Semaph, Busy, Int	84, 100	CY7C0241	t_{AA} = 15, 25, 35, 55	280 @ 15	J,A
128K	8K x 16 —Dual-Port w/ Semaph, Busy, Int	84, 100	CY7C025	t_{AA}=15, 25, 35, 55	280 @ 15	J,A
128K	8K x 18 —Dual-Port w/ Semaph, Busy, Int	84, 100	CY7C0251	t_{AA}=15, 25, 35, 55	280 @ 15	J,A
128K	16K x 8 —Dual-Port w/ Semaph, Busy, Int	64, 68	CY7C006	t_{AA}=15, 25, 35, 55	260 @ 15	J,A
128K	16K x 9 —Dual-Port w/ Semaph, Busy, Int	68, 80	CY7C016	t_{AA}=15, 25, 35, 55	260 @ 15	J,A

Note: Please contact a Cypress Representative for product availability.

SRAM Modules

Cypress Pentium Cache Module



- PC Cache
- 32-Bit Standard
- 8-, 16-, and 24-Bit Standard

Secondary Cache Subsystems

Size	Organization	Pins	Part Number	Speed (MHz)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
256K	P54C Cache (Intel™ Neptune)	160	CYM74BP54	f_{max}=60, 66 MHz	1500	PM
256K	P54C Cache (Intel Neptune)	160	**CYM74SP54**	f_{max}=60, 66 MHz	1500	PM
512K	P54C Cache (Intel Neptune)	160	**CYM74SP55**	f_{max}=60, 66 MHz	1500	PM
256K	P54C Cache (Intel Triton)	160	**CYM74C430**	50, 60, 66 MHz	1600	PM
256K	P54C Cache (Intel Triton)	160	**CYM74S430**	50, 60, 66 MHz	1200	PM
512K	P54C Cache (Intel Triton)	160	**CYM74S431**	50, 60, 66 MHz	1200	PM
256K	P54C Cache (Intel Triton VX)	160	CYM74D432	50, 60, 66 MHz	1435	PM
256K	P54C Cache (Intel Triton II)	160	**CYM74P430B**	50, 60, 66 MHz	750	PM
512K	P54C Cache (Intel Triton II)	160	**CYM74P431B**	50, 60, 66 MHz	1400	PM
256K	P54C Cache (Intel Triton II ETag)	160	**CYM74P434B**	50, 60, 66 MHz	900	PM
512K	P54C Cache (Intel Triton II ETag)	160	**CYM74P435B**	50, 60, 66 MHz	1550	PM
256K	P54C Cache (OPTi Viper)	160	CYM74D550	50, 60, 66 MHz	1650	PM
256K	P54C Cache (OPTi Viper)	160	**CYM74S550**	50, 60, 66 MHz	1500	PM
512K	P54C Cache (OPTi Viper)	160	**CYM74S551**	50, 60, 66 MHz	1500	PM
256K	P54C Cache (VLSI 590)	160	CYM74B590	60, 66 MHz	1500	PM
256K	P54C Cache (VLSI 590)	160	**CYM74S590**	60, 66 MHz	1500	PM
512K	P54C Cache (VLSI 590)	160	**CYM74S591**	60, 66 MHz	1500	PM
256K	Power PC	136	CYM76A256	50, 60, 66 MHz	1250	PM
256K	Power PC	136	CYM76S256	50, 60, 66 MHz	1200	PM
512K	Power PC	136	CYM76S512	50, 60, 66 MHz	1200	PM
256K	Power PC	160	CYM76S640	50, 60, 66 MHz	TBD	PM
512K	Power PC	160	CYM76S641	50, 60, 66 MHz	TBD	PM

Note: Please contact a Cypress Representative for product availability.

SRAM Modules (continued)

32-Bit Standard SRAM Module Family

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
512K	16K x 32	64	CYM1821	t_{AA} = 20, 25, 30, 35, 45	720 @ 20	PM, PZ
2M	64K x 32	64	CYM1831	t_{AA} = 15, 20, 25, 30, 35, 45	720 @ 25	PM, PN, PZ
4M	128K x 32	64	CYM1836	t_{AA} = 20, 25, 30, 35, 45 t_{AA} = 15	480 @ 20 760 @ 15	PM, PZ
8M	256K x 32	64	CYM1841A	t_{AA} = 25, 30, 35, 45, 55 t_{AA} = 20 t_{AA} = 12, 15	960 @ 25 1120 @ 20 1600 @ 12	PM, PN, PZ
8M	256K x 32 (72-pin Superset)	72	CYM1841AP7	t_{AA}=12, 15, 20, 25, 30, 35, 45	960 @ 25 1120 @ 20 1600 @ 15	PM
16M	512K x 32 (72-pin Superset)	72	CYM1846	t_{AA}=20, 25, 30, 35	800	PM, PZ
32M	1M x 32 (72-pin Superset)	72	CYM1851	t_{AA} = 20, 25, 30, 35	1250 @ 25	PM, PN, PZ

8-, 16-, and 24-Bit SRAM Modules, 32-Bit PGA and DIP Modules

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages
2M	256K x 8—JEDEC Sep I/O	60	CYM1441	t_{AA}=20, 25, 35, 45	960 @ 25	PZ
4M	512K x 8—JEDEC	32	CYM1464	t_{AA} = 20, 22, 25, 30, 35, 45, 55,	350 @ 20	PD
4M	512K x 8—JEDEC	32	CYM1465	t_{AA} = 70, 85,100,120, 150	110 @ 70	PD
16M	2M x 8	36	CYM1481	t_{AA} = 85, 100, 120	110 @ 85	PS
1M	64K x 16	40	CYM1622	t_{AA} = 15, 20, 25, 30, 35, 45	400 @ 25	PV
768K	32K x 24	56	CYM1720	t_{AA} = 15, 20, 25, 30, 35	330 @ 25	PZ
1.5M	64K x 24	56	CYM1730	t_{AA} = 25, 30, 35	510 @ 25	PZ
4M	128K x 32	66	CYM1838	t_{AA} = 25, 30, 35	720 @ 25	HG
8M	256K x 32	60	CYM1840	t_{AA} = 20, 25, 30, 35, 45, 55	1120 @ 25	PD

DRAM Controller Modules

Organization	Bus Width	Part Number	Speed (MHz)	Package
DRAM Accelerator	32-Bit	CYM7232	25/33/40	PGC
DRAM Accelerator	64-Bit	CYM7264	25/33/40	PGC

Note: Please contact a Cypress Representative for product availability.

Programmable Logic Devices (PLDs)

Cypress's Programmable Logic offering ranges from the industry-standard small Programmable Logic Devices (SPLDs) to Complex Programmable Logic Devices (CPLDs) and Field Programmable Gate Arrays (FPGAs). The entire family is supported by the Cypress *Warp*™ development tools for complete device independence during the design cycle.

PLDs (Small)

- CMOS Flash and UV erasable technology expertise
- Complete line of SPLDs
  - GAL® architectures like the 16V8, 20V8, PAL20, and 22V10
  - Application specific architectures in the CY7C330 family
- Packaging options include PDIP, PLCC, and LCC packages plus the space-saving QSOP package

PLDs

Part Number	t_{PD} (ns)	f (MHz)	I_{CC} (mA)	Pins	Packages
PALC16L8	20/25/35	18/28.5	70	20	D, L, P, Q, W
PALC16L8L	25/35	18/28.5	45	20	D, L, P, Q, W
PALC16R4	20/25/35	18/28.5	70	20	D, L, P, Q, W
PALC16R4L	25/35	18/28.5	45	20	D, L, P, Q, W
PALC16R6	20/25/35	18/28.5	70	20	D, L, P, Q, W
PALC16R6L	25/35	18/28.5	45	20	D, L, P, Q, W
PALC16R8	20/25/35	18/28.5	70	20	D, L, P, Q, W
PALC16R8L	25/35	18/28.5	45	20	D, L, P, Q, W
PALCE16V8	7.5	100	115	20	D, J, L, P
PALCE16V8	10/15/25	33/45/69	90	20	D, J, L, P, QSOP
PALCE16V8L	15/25	33/45.5	55	20	D, J, L, P, QSOP
PLDC20G10	25/35	18/33.3	55	24/28	D, J, L, P, W
PLDC20G10B	15/20/25	33/42/45.5	70	24/28	D, J, L, P, W
PLDC20RA10	15/20/25/35	18/33/42/45.5	75	24/28	D, J, L, P, W
PALCE20V8	7.5	100	115	24/28	D, J, L, P
PALCE20V8	10/15/25	33/45/58.8	90	24/28	D, J, L, P
PALCE20V8L	15/25	33/45.5	55	24/28	D, J, L, P, QSOP
PALC22V10*	20/25/35	18/33/41.7	90	24/28	D, J, L, P, Q, W
PALC22V10L*	25/35	18/33.3	55	24/28	D, J, L, P, Q, W
PALC22V10B*	15/20	42/50	90	24/28	D, J, L, P, Q, W
PALC22V10D	7.5	100	130	24/28	D, J, L, P
PALC22V10D	10/15/25	30/50/76.9	90	24/28	D, J, L, P
PALCE22V10	5	142.8	115	24/28	D, J, L, P
PALCE22V10	10/15/25	33/50/76.9	90	24	D, J, L, P
CY7C331	20/25/35	35	130	28	D, J, P, Q, W
CY7C335	15/20/25	35/45/50	140	28	D, J, P, W

* Not recommended for new designs.

Note: Please contact a Cypress Representative for product availability.

Complex PLDs (CPLDs)

UltraLogic™ FLASH370™/FLASH370i™

- State-of-the-art Flash technology for electrical erasability.
- Guaranteed routability.
- Unique single product term sharing and steering.
- Architecture provides complete design flexibility for user assigned pinouts. Even when you make changes to your logic, you will be able to maintain the same pin configuration.
- Significant capacity advantages over all other CPLD architectures.
- Simple one case timing model for easy design and system simulation.
- Everything you liked about the 22V10 now available in high-performance, high-density logic.
- In-System-Reprogrammable™ (ISR™) versions are upward compatible from earlier devices using existing software tools.

Flash370

Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA)	Packages
32-Macrocell Flash CPLD	44	CY7C371	$f_{MAX}/t_S/t_{CO}$=143 MHz/5 ns/6 ns	175	A, J, Y
32-Macrocell Flash CPLD Low Power	44	CY7C371L	$f_{MAX}/t_S/t_{CO}$=83 MHz/6.5 ns/6.5 ns	90	A, J
64-Macrocell Flash CPLD	44, 84, 100	CY7C372/3	$f_{MAX}/t_S/t_{CO}$=100 MHz/6.5 ns/6.5 ns	250	A, G, J, Y
64-Macrocell Flash CPLD Low Power	44, 84, 100	CY7C372L/3L	$f_{MAX}/t_S/t_{CO}$=66 MHz/10 ns/10 ns	125	A, G, J, Y
128-Macrocell Flash CPLD	84, 100, 160	CY7C374/5	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/7 ns/7 ns	300	A, G, J, U, Y
128-Macrocell Flash CPLD Low Power	84, 100, 160	CY7C374L/5L	$f_{MAX}/t_S/t_{CO}$ = 66 MHz/10 ns/10 ns	150	A, G, J, U, Y
32-Macrocell ISR Flash CPLD	44	CY7C371i	$f_{MAX}/t_S/t_{CO}$=143 MHz/5 ns/6 ns	175	A, J, Y
32-Macrocell ISR Flash CPLD Low Power	44	CY7C371iL	$f_{MAX}/t_S/t_{CO}$=83 MHz/6.5 ns/6.5 ns	90	A, J
64-Macrocell ISR Flash CPLD	44, 84, 100	CY7C372i/3i	$f_{MAX}/t_S/t_{CO}$=100 MHz/6.5 ns/6.5 ns	250	A, G, J, Y
64-Macrocell ISR Flash CPLD Low Power	44, 84, 100	CY7C372iL/3iL	$f_{MAX}/t_S/t_{CO}$=66 MHz/10 ns/10 ns	125	A, G, J, Y
128-Macrocell ISR Flash CPLD	84, 100, 160	CY7C374i/5i	$f_{MAX}/t_S/t_{CO}$ = 100 MHz/7 ns/7 ns	300	A, G, J, U, Y
128-Macrocell ISR Flash CPLD Low Power	84, 100, 160	CY7C374iL/5iL	$f_{MAX}/t_S/t_{CO}$ = 66 MHz/10 ns/10 ns	150	A, G, J, U, Y

UltraLogic™ Ultra39000™

- In-System-Reprogrammable CPLDs offering high density and high performance
- Fully compliant to PCI Local Bus Specification
- Simple timing model for easy design and system simulation
- Full JTAG (IEEE 1149.1) compatibility
- Operation at 3.3V or 5V
- Extends the density of FLASH CPLDs up to 512 macrocells
- Supports fixed pin assignments

Ultra39000™

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA)	Packages
192-Macrocell Flash ISR CPLD	84, 160	CY7C39192	$f_{MAX}/t_{PD}/t_S/t_{CO}$=125 MHz/10 ns/5 ns/5.5 ns	TBD	A, J
256-Macrocell Flash ISR CPLD	160, 208	CY7C39256	$f_{MAX}/t_{PD}/t_S/t_{CO}$=125 MHz/10 ns/5 ns/5.5 ns	TBD	A, N
320-Macrocell Flash ISR CPLD	208, 240	CY7C39320	$f_{MAX}/t_{PD}/t_S/t_{CO}$=125 MHz/10 ns/5 ns/5.5 ns	TBD	N
384-Macrocell Flash ISR CPLD	240	CY7C39384	$f_{MAX}/t_{PD}/t_S/t_{CO}$=100 MHz/12 ns/6 ns/6.5 ns	TBD	N
448-Macrocell Flash ISR CPLD	240, 304	CY7C39448	$f_{MAX}/t_{PD}/t_S/t_{CO}$=100 MHz/12 ns/6 ns/6.5 ns	TBD	N
512-Macrocell Flash ISR CPLD	304	CY7C39512	$f_{MAX}/t_{PD}/t_S/t_{CO}$=100 MHz/12 ns/6 ns/6.5 ns	TBD	N

Note: Please contact a Cypress Representative for product availability.

MAX340

- Cypress's first-generation CPLD remains an innovator in the CPLD market.
- Only second-sourced family of CPLDs available.
- Offers a range of general-purpose programmable logic that makes it ideal for replacing large amounts of TTL logic.
- High-volume 0.8µ UV-erasable CMOS process.
- Family offers faster and denser devices than previous generations of Small PLDs and EPLDs.
- CY7C340B devices are 0.65µ shrinks of the original versions offering even faster speed options.

MAX340

Organization	Pins	Part Number	Speed (ns)	I_{CC}/I_{SB} (mA)	Packages
32 Macrocell CPLD	28S	CY7C344/B	$t_{PD/S/CO}$ = 15/10/10, 10/6/5	200/150	H, J, P, W
64 Macrocell CPLD	44	CY7C343/B	$t_{PD/S/CO}$ = 20/12/12, 12/8/6	135/125	H, J, R
128 Macrocell CPLD	68	CY7C342/ 342B	$t_{PD/S/CO}$ = 25/15/14, 12/8/6	250/225	H, J, R
128 Macrocell CPLD	84, 100	CY7C346/B	$t_{PD/S/CO}$ = 25/15/14, 15/10/7	250/225	H, J, N, R
192 Macrocell CPLD	84	CY7C341/ 341B	$t_{PD/S/CO}$ = 25/15/14, 15/10/7	380/360	H, J, R

FPGAs

UltraLogic pASIC380™

- Cypress's ViaLink antifuse technology
- High-speed FPGA
- ViaLink cell has a 50Ω resistance and <1 fF capacitance
  - Time constant is orders of magnitude lower than any other FPGA technology
  - The highest FPGA performance available
  - More consistent timing than in traditional FPGAs
  - Very low power with a typical standby power of 2 mA
- The small cell size of the ViaLink fuse allows 100% link coverage at every wire intersection:
  - Robust routing resources
  - Completely automatic place-and-route capabilities
  - Full use of all the logic resources for the highest utilization of any FPGAs on the market
- The UltraLogic pASIC3380 FPGAs offer all the advantages of the UltraLogic pASIC380 family at 3.3V.
- 1K, 4K, 8K device offers complete PCI compatibility

pASIC380

Organization	Pins	Part Number	Speed Grade	I_{CC}/I_{SB} (mA)	Packages
CMOS 1K Gates FPGA	44, 68, 100	CY7C381P/2P	-X, -0, -1, -2	I_{SB} = 10	A, G, J
3.3V CMOS 1K Gates FPGA	44, 68, 100	CY7C3381A/2A	-X, -0, -1	I_{SB} = 0.65	A, J
CMOS 2K Gates FPGA	68, 84, 100	CY7C383A/4A	-X, -0, -1, -2	I_{SB} = 10	A, G, J
3.3V CMOS 2K Gates FPGA	68, 84, 100	CY7C3383A/4A	-X, -0, -1	I_{SB} = 0.65	A, J
CMOS 4K Gates FPGA	84, 100, 144, 160	CY7C385P/6P	-X, -0, -1, -2	I_{SB} = 10	A, G, J, U
3.3V CMOS 4K Gates FPGA	84, 100, 144	CY7C3385A/6A	-X, -0, -1	I_{SB} = 0.65	A, J
CMOS 8K Gates FPGA	144, 160, 208, 223	CY7C387P/8P	-X, -0, -1, -2	I_{SB} = 10	A, G, N, U
3.3V CMOS 8K Gates FPGA	144, 208	CY7C3387P/8P	-X, -0, -1	I_{SB} = 0.65	A, N

Note: Please contact a Cypress Representative for product availability.

FPGAs (continued)

UltraLogic Ultra38000™

- 0.65µ triple layer metal CMOS process with ViaLink™ programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - Density from 9,000 to 60,000 total available gates
  - 3,000 to 20,000 typically usable “gate array” gates
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 100 MHz consumes 50 mA
  - Minimum I_{OL} and I_{OH} of 24 mA
- Fully PCI compliant inputs & outputs
  - Full 33 MHz system performance
- Full JTAG testability
  - IEEE standard 1149.1.6
- Flexible logic cell architecture
  - Very low cell propagation delay (1.4 ns typical)
  - Fragments into five fine-grained functions for the worlds most efficient synthesis

Ultra38000

Organization	Pins	Part Number	Speed Grade	I_{CC}/I_{SB} (mA)	Packages
CMOS 3K Gates FPGA	84, 144	CY7C38003	-X, -0, -1, -2	I_{SB} = 10	A, J
3.3V CMOS 3K Gates FPGA	84, 144	CY7C338003	-X, -0, -1, -2	I_{SB} = 0.65	A, J
CMOS 5K Gates FPGA	84, 144, 208	CY7C38005	-X, -0, -1, -2	I_{SB} = 10	A, J, N
3.3V CMOS 5K Gates FPGA	84, 144, 208	CY7C338005	-X, -0, -1, -2	I_{SB} = 0.65	A, J, N
CMOS 7K Gates FPGA	144, 208, 256	CY7C38007	-X, -0, -1, -2	I_{SB} = 10	A, N, BGA
3.3V CMOS 7K Gates FPGA	144, 208, 256	CY7C338007	-X, -0, -1, -2	I_{SB} = 0.65	A, N, BGA
CMOS 9K Gates FPGA	144, 208, 256	CY7C38009	-X, -0, -1, -2	I_{SB} = 10	A, N, BGA
3.3V CMOS 9K Gates FPGA	144, 208, 256	CY7C338009	-X, -0, -1, -2	I_{SB} = 0.65	A, N, BGA
CMOS 12K Gates FPGA	208, 352	CY7C38012	-X, -0, -1, -2	I_{SB} = 10	N, BGA
3.3V CMOS 12K Gates FPGA	208, 352	CY7C338012	-X, -0, -1, -2	I_{SB} = 0.65	N, BGA
CMOS 16K Gates FPGA	208, 352	CY7C38016	-X, -0, -1, -2	I_{SB} = 10	N, BGA
3.3V CMOS 16K Gates FPGA	208, 352	CY7C338016	-X, -0, -1, -2	I_{SB} = 0.65	N, BGA
CMOS 20K Gates FPGA	208, 352	CY7C38020	-X, -0, -1, -2	I_{SB} = 10	N, BGA
3.3V CMOS 20K Gates FPGA	208, 352	CY7C338020	-X, -0, -1, -2	I_{SB} = 0.65	N, BGA

Note: Please contact a Cypress Representative for product availability.

Design and Programming Tools

The capabilities of our UltraLogic product line— FLASH370 CPLDs, pASIC380 FPGAs, and *Warp* design tools—greatly simplify your design effort and let you reach the optimal solution to your design problem in the shortest possible time.

- Supports entire Programmable Logic product offering
  - Small PLDs
  - CPLDs
  - FPGAs
- Open, IEEE-STD-1076 VHDL (Very-high-speed Integrated-Circuit Hardware Description Language) for programmable logic design
- Accepts designs as VHDL text, via schematic capture, as EDIF files, or in any combination of these entry modes
- Shortens the design process through its extraordinary capabilities
  - VHDL source code verification
  - Debug
  - Graphical waveform simulation and editing
  - Graphical timing simulation and analysis
- Multiple entry points
  - *Warp2*, low-cost VHDL tool
  - *Warp3*, high-end Viewlogic based tool
- *Impulse3*™ programmer is a low cost, engineering support programmer
  - Supports all of Cypress's programmable devices
  - Gives you the ability to prove your design, in silicon, with a short cycle time

Design and Programming Tools

Description	Type	Part Number
Warp2™ for PC	VHDL Design Tool	CY3120
Warp2 for Sun	VHDL Design Tool	CY3125
Warp3™ for PC	VHDL/CAE Design Tool	CY3130
Warp3 for Sun	VHDL/CAE Design Tool	CY3135
Abel™ Kit for PC	FLASH370 Design Kit	CY3140
PROseries™ for PC	Viewlogic™ Design Kit	CY3141
Abel Kit for SUN	FLASH370 Design Kit	CY3145
Synopsys™ for Sun	pASIC380 Design Kit	CY3146
Impulse3™	Programmer	CY3500

Note: Please contact a Cypress Representative for product availability.

PROMs/EPROMs

- World's fastest PROMs and EPROMs
- 4K to 1M density
- Industry-standard pinouts
- Low-power CMOS technology
- PDIP, PLCC, TSOP, CDIP, LCC packages
- Registered and x16 versions
- Direct replacement for Bipolar PROMs

CMOS PROMs

Density	Organization	Pins Count	Part Number	Access Time t_{AA} (ns)	Feature
8K	1K x 8	24/28	CY7C281A	25/30/45	300-mil DIP
8K	1K x 8	24	CY7C282A	25/30/45	600-mil DIP
16K	2K x 8	24/28	CY7C291A/AL	20/25/35/50	300-mil DIP
16K	2K x 8	24	CY7C292A/AL	20/25/35/50	600-mil DIP
16K	2K x 8	24/28	CY7C293A/AL	20/25/35/50	Power-Down
32K	4K x 8	24/28	CY7C243	20/25/35/45/55	300-mil DIP
32K	4K x 8	24	CY7C244	20/25/35/45/55	600-mil DIP
64K	8K x 8	24/28	CY7C261	20/25/35/45/55	Power-Down
64K	8K x 8	24/28	CY7C263	20/25/35/45/55	300-mil DIP
64K	8K x 8	24	CY7C264	20/25/35/45/55	600-mil DIP
64K	8K x 8	28/32	CY7C266	20/25/35/45	EPROM Pin Out
128K	16K x 8	28/32	CY7C251	45/55/65	Power-Down
128K	16K x 8	28/32	CY7C254	45/55/65	600-mil DIP
256K	32K x 8	28/32	CY7C271A	25/30/35/45/55	Power-Down
256K	16K x 16	44	CY7C276	25/30/35	16 Bit Word Wide

CMOS Registered PROMs

Density	Organization	Pins Count	Part Number	Set-Up t_{SA} (ns)	Clock-to-Out t_{CO} (ns)
4K	512 x 8	24/28	CY7C225A	18/25/30/35/40	12/12/15/20/25
8K	1K x 8	24/28	CY7C235A	18/25/30/40	12/12/15/20
16K	2K x 8	24/28	CY7C245A/AL	15/18/25/35/45	10/12/12/15/25
64K	8K x 8	28	CY7C265	15/25/40/50	12/15/20/25
64K	8K x 8	28	CY7C269	15/25/40/50	12/15/20/25
256K	32K x 8	28/32	CY7C277	30/40/50	15/20/25
512K	64K x 8	28/32	CY7C287	45/55/65	15/20/25

CMOS EPROMs

Density	Organization	Pin Count	Part Number	Access Time tAA (ns)	Feature
64K	8K x 8	28/32	CY27C64	45/55/70/90/120/150/200	High Speed, CY7C266 Algorithm
128K	16K x 8	28/32	CY27C128	45/55/70/90/120/150/200	High Speed, Cypress Proprietary Algorithm
256K	32K x 8	28/32	CY27C256	45/55/70/90/120/150/200	High Speed, Cypress Proprietary Algorithm
256K	32K x 8	28/32	CY27C256A*	45/55/70/90/120/150/200	Industry Standard Algorithm
256K	32K x 8	28/32	CY27H256	25/30/35/45/55/70	High Speed, Industry Standard Algorithm
512K	64K x 8	28/32	CY27C512*	45/55/70/90/120/150/200	Industry Standard Algorithm
512K	64K x 8	28/32	CY27H512	25/30/35/45/55/70	High Speed, Industry Standard Algorithm
1024K	128K x 8	32	CY27C010*	45/55/70/90/120/150/200	Industry Standard Algorithm
1024K	128K x 8	32	CY27H010	25/30/35/45/55/70	High Speed, Industry Standard Algorithm

* Available 2Q96

Note: Please contact a Cypress Representative for product availability.

FIFOs

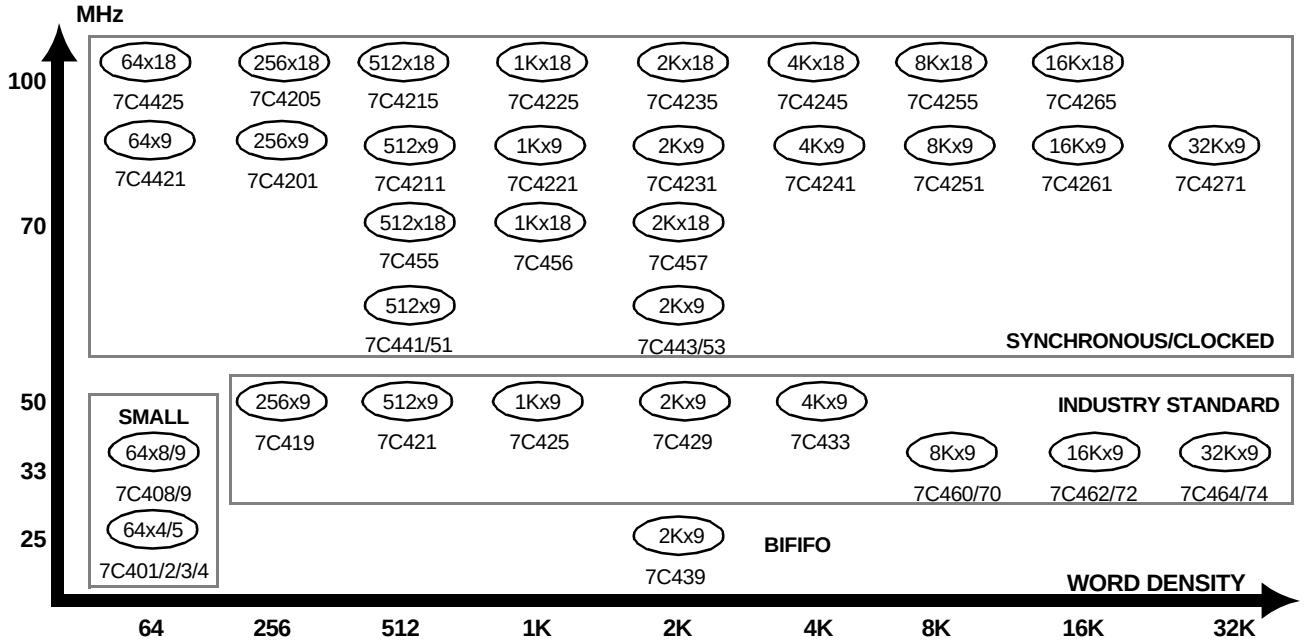
Asynchronous:

- 10-ns access time
- Industry-standard operation and pinout
- Densities up to 32Kx9—all densities pin compatible
- TQFP packaging

Synchronous/Clocked:

- 100 MHz operation
- Programmable flags
- All densities pin compatible
- TQFP packaging

FIFO Product Portfolio



Asynchronous

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ ns)	Packages
64 x 4	16	CY3341	1.2, 2 MHz	45	D, P
64 x 4	16	CY7C401	5, 10, 15, 25 MHz	75	D, L, P
64 x 4—w/$\overline{OE}$	16	CY7C403	10, 15, 25 MHz	75	D, L, P
64 x 5	18	CY7C402	5, 10, 15, 25 MHz	75	D, L, P
64 x 5—w/$\overline{OE}$	18	CY7C404	10, 15, 25 MHz	75	D, L, P
64 x 8—w/$\overline{OE}$ and Almost Flags	28S	CY7C408A	15, 25, 35 MHz	115 @ 15	D, L, P, V
64 x 9—w/Almost Flags	28S	CY7C409A	15, 25, 35 MHz	115 @ 15	D, L, P, V
256 x 9—w/Half Full Flag	28S, 32	CY7C419	10, 15, 20, 25, 30, 40, 65	35 @ 20	A, D, L, P, V
512 x 9—w/Half Full Flag	28	CY7C420	20,25, 30, 40, 65	35 @ 20	D, P
512 x 9—w/Half Full Flag	28S, 32	CY7C421	10, 15, 20,25, 30, 40, 65	35 @ 20	A, D, J, L, P, V
1K x 9—w/ Half Full Flag	28	CY7C424	20,25, 30, 40, 65	35 @ 20	D, P
1K x 9—w/ Half Full Flag	28S, 32	CY7C425	10, 15, 20,25, 30, 40, 65	35 @ 20	A, D, J, L, P, V
2K x 9—w/ Half Full Flag	28	CY7C428	20,25, 30, 40, 65	35 @ 20	D, P
2K x 9—w/ Half Full Flag	28S, 32	CY7C429	10, 15, 20,25, 30, 40, 65	35 @ 20	A, D, J, L, P, V

Note: Please contact a Cypress Representative for product availability.

FIFOs (continued)

Asynchronous (continued)

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ ns)	Packages
4K x 9—w/ Half Full Flag	28	CY7C432	25, 30, 40, 65	35 @ 20	D, P
4K x 9—w/Half Full Flag	28S, 32	CY7C433	10, 15, 20, 25, 30, 40, 65	35 @ 20	A, D, J, L, P, V
8Kx9—w/ Half Full Flag	28	CY7C460	15, 25, 40, 65	105 @ 15	D, J, L, P
8Kx9—w/ Prog. Flags	28	CY7C470	15, 25, 40, 65	105 @ 15	D, J, L, P
16Kx9—w/ Half Full Flag	28	CY7C462	15, 25, 40, 65	105 @ 15	D, J, L, P
16Kx9—w/ Prog. Flags	28	CY7C472	15, 25, 40, 65	105 @ 15	D, J, L, P
32Kx9—w/ Half Full Flag	28	CY7C464	15, 25, 40, 65	105 @ 15	D, J, L, P
32Kx9—w/ Prog. Flags	28	CY7C474	15, 25, 40, 65	105 @ 15	D, J, L, P
2K x 9—Bidirectional	28S	CY7C439	25, 30, 40, 65	147@ 25	D, J, L, P

Clocked

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ MHz)	Packages
512x9—Clocked	28S, 32	CY7C441	14, 20, 30*	70 @ 20	D, J, L, P, V
512x9—Clocked w/ Prog. Flags	32	CY7C451	14, 20, 30*	70 @ 20	D, J, L
2Kx9—Clocked	28S, 32	CY7C443	14, 20, 30*	70 @ 20	D, J, L, P, V
2K x9—Clocked w/ Prog. Flags	32	CY7C453	14, 20, 30*	70 @ 20	D, J, L
512 x 18—Clocked w/Prog. Flags	52	CY7C455	14, 20, 30*	90 @ 20	J, L, N
1K x 18—Clocked w/Prog. Flags	52	CY7C456	14, 20, 30*	90 @ 20	J, L, N
2K x 18—Clocked w/Prog. Flags	52	CY7C457	14, 20, 30*	90 @ 20	J, L, N

Synchronous

Organization	Pins	Part Number	Speed (ns)	I_{CC} (mA @ MHz)	Packages
64 x 9—Synchronous	32	CY7C4421	10, 15, 25, 35*	50 @ 20	A, J
256 x 9—Synchronous	32	CY7C4201	10, 15, 25, 35*	50 @ 20	A, J
512 x 9—Synchronous	32	CY7C4211	10, 15, 25, 35*	50 @ 20	A, J
1K x 9— Synchronous	32	CY7C4221	10, 15, 25, 35*	50 @ 20	A, J
2K x 9—Synchronous	32	CY7C4231	10, 15, 25, 35*	50 @ 20	A, J
4K x 9—Synchronous	32	CY7C4241	10, 15, 25, 35*	50 @ 20	A, J
8K x 9—Synchronous	32	CY7C4251	10, 15, 25, 35*	50 @ 20	A, J
16K x 9—Synchronous	32	CY7C4261	10, 15, 25, 35*	50 @ 20	A, J
32K x 9—Synchronous	32	CY7C4271	10, 15, 15, 35*	50 @ 20	A, J
64 x 18—Synchronous	64, 68	CY7C4425	10, 15, 25, 35*	100 @ 20	A, J
256 x 18—Synchronous	64, 68	CY7C4205	10, 15, 25, 35*	100 @ 20	A, J
512 x 18— Synchronous	64, 68	CY7C4215	10, 15, 25, 35*	100 @ 20	A, J
1K x 18—Synchronous	64, 68	CY7C4225	10, 15, 25, 35*	100 @ 20	A, J
2K x 18—Synchronous	64, 68	CY7C4235	10, 15, 25, 35*	100 @ 20	A, J
4K x 18—Synchronous	64, 68	CY7C4245	10, 15, 25, 35*	100 @ 20	A, J
8K x 18—Synchronous	64, 68	CY7C4255	10, 15, 25, 35*	100 @ 20	A, J
16K x 18—Synchronous	64, 68	CY7C4265	10, 15, 25, 35*	100 @ 20	A, J

* Cycle Times

Note: Please contact a Cypress Representative for product availability.

Communication Products

Description	Pins	Part Number	Speed (MHz)	I_{CC} (mA)	Packages
HOTLink Transmitter	28	CY7B923	160-330	65	J, L, S
HOTLink Receiver	28	CY7B933	160-330	120	J, L, S
SONET/SDH Serial Transceiver	24	CY7B951	51 & 155	50	S
10BASE 2/5 Ethernet Coax Transceiver	16, 20, 28	CY7B8392	10	25	J, P
Fast Ethernet 100BASE-T4 Transceiver	80	CY7C971	10 & 100	300	N
Fast Ethernet 100BASE-TX Transceiver	44	CY7C972	100	200	J
HOTLink Evaluation Card	N/A	CY9266	160-330	—N/A	C, F*, T

* Interface: C-Coax; T-twisted pair; F-fiber

CY7B923 and CY7B933: HOTLink™
- Transmitter/receiver chipset
- 160-330 Mb/s operation
- Fibre Channel/ESCON™ compliant
- On-chip 8B/10B encoding/decoding
- Built-In Self-Test
- Evaluation boards available (CY9266)
- User's Guide available

CY7B951: SONET/SDH Serial Transceiver
- SONET/SDH and ATM compatible
- OC-1 (51.8 MHz) and OC-3 (155.5 MHz) clock/ data recovery
- Loop-back testing

CY7B8392: Low-power Coax Transceiver for Ethernet applications
- Pin compatible to industry standard 8392
- 10BASE5 and 10BASE2 applications
- Auto Attachment Unit Interface (AUI)
- Hybrid collision detection

CY7C971: 100BASE-T4/10BASE-T Fast Ethernet Transceiver
- Three operating modes:100BASE-T4, 10BASE-T Full Duplex, 10BASE-T
- Media Independant Interface (MII)
- N-way auto negotiation
- Receive filter/Adaptive equalization
- Low latency repeater mode
- Category 3 wiring

CY7C973: 100BASE-TX Fast Ethernet Transceiver
- Supports 100 MHz operation
- FDDI TP-PMD compliant
- Category 5 wiring

Note: Please contact a Cypress Representative for product availability.

VMEbus Interface Products

VIC068A and VAC068A
- 32-bit VMEbus operation
- Complete VMEbus interface controller/ arbiter
- Complete master/slave capability
- Commercial/Industrial/Military
- User's Guide available

VIC64
- 64-bit MBLT operation
- Software and pin compatible to VIC068A
- Complete master/slave capability
- Commercial/Industrial/Military
- Design Notes available

CY7C964
- Companion to VIC64 & VIC068A
- Commercial/Industrial/Military
- Design Notes available

CY7C960/1
- 64-bit Slave operation
- Commercial/Industrial/Military

CY7C965: Raceway
- High-speed Crosspoint Interconnect
- Implements Open Bus Standard (VITA 5-1994)
- 160 Mbyte/sec throughput per part

Description	Pins	Part Number	Transfer Rate (MB/s)	I_{CC} (mA)	Packages
VME Interface Controller	144/160	VIC068A	40	150	A, B, G, N, U
VME Address Controller	144/160	VAC068A	—	150	B, G, N, U
64-Bit VIC	144/160	VIC64	80	150	A, B, G, N, U
Bus Interface Logic Circuit	64/68	CY7C964	—	120	A, N, U
Slave VMEbus Interface Controller	64/100	CY7C960/1	80	150	A, G, N, U
Raceway	361	CY7C965	160	100	Ball Grid Array

Timing Technology Products

Today's high-performance digital designs have become increasingly complex. These designs often require multiple clock frequencies in order to control all the functions on the board. In the past, this required the designer to use multiple metal-can oscillators which increased the size and cost of the design. Cypress solves this problem by providing single chips which can synthesize multiple frequencies.

Cypress specializes in the development and production of high-performance frequency synthesis devices. Cypress motherboard frequency synthesizers are specifically designed to provide frequencies used in PC motherboard design. PC graphics frequency products provide frequencies most often required for graphics card designs. Cypress also offers general purpose, programmable clock synthesizers for use in any application that requires multiple clock frequencies and in-system frequency changes.

Cypress QuiXTAL is a field programmable metal can oscillator. QuiXTAL provides the designer with the flexibility to use frequencies not available in standard "off-the-shelf" metal can oscillators. QuiXTAL also provides the ability to make last minute frequency adjustments.

Cypress also provides high precision PLL-based devices for low skew clock distribution. The RoboClock Family ofers programmable skew, frequency multiplication/division, 50% delay cycle, and PCI compliance. These features eliminate the need to redo board layout by compensating for varying PCB traces and varying device set-up and hold times.

CY7B9910/20: RoboClock Jr.
- 1 to 8 clock distribution
- Zero propagation delay

CY7B991/2: RoboClock
- Generates 8 clocks from input frequency of 3.75-80 MHz
- User configurable skew control (over 26,000 configurations)
- Divided/Multiplied Outputs

Note: Please contact a Cypress Representative for product availability.

Timing Technology Products (continued)

Timing Technology Products

Application	Part #	# of PLLs	# of Outputs	Features	Package
Industry Standard Motherboard Frequency Synthesizers	CY2250	1	14	Pentium/Pentium Pro servers: 12 skew controlled CPU clocks (250 ps pin-to-pin), 2 buffered reference clocks, 3.3V	28 SOIC
	CY2252	2	14	Pentium portables: 5 CPU/6 PCI clocks (2 “early” PCI for docking stations), 24 MHz, 2 buffered reference clocks, 3.3V	28 SSOP
	CY2254A	2	14	Intel Triton chipset compatible: 4 CPU/6 PCI clocks, 12 MHz, 24 MHz, 2 buffered reference clocks, 3.3V	28 SOIC
	CY2255	1	14	OPTi Viper chipset compatible: 6 CPU (1 “early”)/6 PCI clocks, 2 buffered reference clocks, 3.3V	28 SOIC
	CY2257	1	14	Ali Aladdin chipset compatible: 6 CPU/6 PCI clocks, 2 buffered reference clocks, 3.3V	28 SOIC
	CY2260	2	14	Intel Natoma/Triton II chipset compatible: 4 CPU/6 PCI clocks, 48 MHz USB clock, 3 buffered reference clocks, 3.3V	28 SOIC 28 SSOP
General Purpose Programmable Products (486 Pentium/Pentium Pro motherboards, peripherals, cable TV, video games, MPEG decoders, etc.)	CY2071	1	3	Factory EPROM programmable single PLL, 0.5-100 MHz, 5V/3.3V	8 SOIC
	CY2081	3	3	Factory EPROM programmable triple PLL, 0.5-100 MHz, 5V/3.3V	8 SOIC
	CY2291	3	8	Factory EPROM progrmmable triple PLL, 0.2-100 MHz, 5V/3.3V	20 SOIC
	CY2292	3	6	Factory EPROM programmable triple PLL, 0.2-100 MHz, 5V/3.3V	16 SOIC
	ICD2051	2	5	User-programmable dual PLL, 0.3-120 MHz, 5V	16 SOIC
	ICD2053B	1	1	User-programmable single PLL, 0.4-100 MHz, 5V	8 SOIC
PC Graphics Frequency Synthesizers	ICD2061A	2	2	User-programmable PC video/memory clocks, 0.4-120 MHz, 5V	16 SOIC
	ICD2062B	2	6	User-programmable PECL video clock for workstations, 0.5-165 MHz, 5V	20 SOIC
	ICD2063	2	2	User-programmable PC video/memory clocks, 0.3-135 MHz, 5V/3.3V	16 SOIC
Programmable Skew Clock Buffer (TTL Output)	CY7B991	1	8	3-80 MHz, Programmable Skew (700 ps increments) 250 ps pin-to-pin skew	J, L
Programmable Skew Clock Buffer (CMOS Output)	CY7B992	1	8	3-80 MHz, Programmable Skew (700 ps increments) 250 ps pin-to-pin skew	J, L
Low Skew Clock Buffer (TTL Output)	CY7B9910	1	8	15-80 MHz, t_{PD} = 500 ps 250 ps pin-to-pin skew	S
Low Skew Clock Buffer (CMOS Output)	CY7B9920	1	8	15-80 MHz, t_{PD} = 500 ps 250 ps pin-to-pin skew	S

Note: Please contact a Cypress Representative for product availability.

PC Chipsets

Description	Pins	Part Number	Package
Single-chip solution for 386/486-based systems with Green features. Supports SMI/CPU interface/cache control/DRAM control/ISA Bus control/VESA control	160	CY82C597	N
Intelligent PCI Bus Bridge Chip. Connects VESA Bus to the PCI Bus	160	CY82C599	N
hyperCache™ Chipset System Controller	208	CY82C691	N
hyperCache Chipset Data-Path with Integrated Cache	208	CY82C692	N
hyperCache Chipset Peripheral Controller	208	CY82C693	N
hyperCache SRAM Expansion	128	CY82C694	A

- 1992 Cypress developed a 386/486 single VESA/ISA chip
- 1993 Cypress introduced the world's first PCI-VESA bridge
- 1994 Cypress updated the chipset with Deep Green features for VESA or VIP systems
- 1995 Cypress introduces the hyperCache™ Chipset for Pentium-class processors

The Cypress hyperCache Chipset is a Pentium-class core logic chipset. It is comprised of three 208-pin chips that include ISA, PCI, system, data, and memory control. It is the most highly integrated chipset on the market and the first chipset available with integrated cache. The hyperCache Chipset includes a 2-way set associative cache tag (capable of addressing up to 1 MB of cache) along with 128 KB of 2-way set associative, synchronous pipelined data cache. This integrated cache gives performance slightly better than 256 KB of external asynchronous direct mapped cache.

The hyperCache Chipset directly drives the DRAM (24 mA with variable drive) and ISA bus (8 mA). Both PCI and ISA use QuietBus logic which reduces the RFI by eliminating spurious bus transitions. The CY82C693 contains IDE with master mode (two separate channels each capable of driving two devices), DMA up to Type F and multi-word 0-2, keyboard controller (full 8042 functionality), Real Time Clock (Dallas 12887 compatible with 256B CMOS), mouse support and 206.

Note: Please contact a Cypress Representative for product availability.

FCT-T Logic Family

The FCT-T CMOS logic family offers the lowest power solution for high speed logic designs. High Drive (64 mA), Balanced Drive (24 mA), or 25Ω Output (12 mA) devices provide a choice of drive capability to meet the applications specific need.

- TTL compatible inputs and outputs provide significant noise reduction over older FCT designs.
- All Cypress FCT-T devices have been designed for use in "Live Insertion" applications.
- All functions are available in space saving QSOP or TSSOP packages as well as the standard 300-mil SOIC.
- Extended temperature range (–40°C to +85°C) is standard on all 16-bit devices and on all Standard, A, or B speed octal devices.

Octal High Drive Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delay (ns) C Com'l	C Mil	B Com'l	B Mil	A Com'l	A Mil	Standard Com'l	Standard Mil	Package
CY29FCT52T	8-Bit Registered Transceiver	24	6.3	7.3	7.5	8.0	10.0	11.0			D, L, P, Q, SO
CY29FCT520T	Multilevel Pipeline Register	24	6.0	7.0	7.5	8.0	14.0	16.0			D, L, P, Q, SO
CY29FCT818T	Diagnostic Scan Register	24	6.0	7.6	7.5	9.0	9.0	12.0	13.0	18.0	D, L, P, Q, SO
CY54/74FCT138T	1-of-8 Decoder	16	5.0	6.0			5.8	7.8	9.0	12.0	D, L, P, Q, SO
CY54/74FCT157T	Quad 2-input Multiplexers	16	4.3	5.0			5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT158T	Quad 2-input Inverting Multiplexers	16	4.3	5.5			5.5	6.3	6.5	7.5	D, L, P, Q, SO
CY54/74FCT163T	4-Bit Binary Counter with Synchronous Reset	16	5.8	6.1			7.2	7.5	11.0	11.5	D, L, P, Q, SO
CY54/74FCT191T	4-Bit Up/Down Binary Counter	16	6.2	8.4			7.8	10.5	12.0	16.0	D, L, P, Q, SO
CY54/74FCT240T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$	20	4.3	4.7			4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT244T	8-Bit Buffer/Line Driver with $\overline{OE}$	20	4.1	4.6			4.8	5.1	6.5	7.0	D, L, P, Q, SO
CY54/74FCT245T	8-Bit Transceiver with $\overline{OE}$	20	4.1	4.5			4.6	4.9	7.0	7.5	D, L, P, Q, SO
CY54/74FCT257T	Quad 2-input Multiplexers with $\overline{OE}$	16	4.3	5.0			5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT273T	8-Bit Register with Asynchronous Reset	20	5.8	6.5			7.2	8.3	13.0	15.0	D, L, P, Q, SO
CY54/74FCT373T	8-Bit Latch with $\overline{OE}$	20	4.2	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT374T	8-Bit Register with $\overline{OE}$	20	5.2	6.2			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT377T	8-Bit Register with Clock Enable	20	5.2	5.5			7.2	8.3	13.0	15.0	D, L, P, Q, SO
CY54/74FCT399T	Quad 2-input Registers	16	6.1	6.6			7.0	7.5	10.0	11.5	D, L, P, Q, SO
CY54/74FCT480T	Dual 8-Bit Odd-Parity Generators/ Checkers	24			5.6	7.0	7.5	9.5	13.0	17.0	D, L, P, Q, SO
CY54/74FCT540T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$ and Flow-Through Pinout	20	4.3	4.7			4.8	5.1	8.5	9.5	D, L, P, Q, SO
CY54/74FCT541T	8-Bit Buffer/Line Driver with $\overline{OE}$ and Flow-Through Pinout	20	4.3	4.7			4.8	5.1	8.5	9.5	D, L, P, Q, SO
CY54/74FCT543T	8-Bit Latched Transceiver with $\overline{OE}$	24	5.3	6.1			6.5	7.5	8.5	10.0	D, L, P, Q, SO
CY54/74FCT573T	8-Bit Latch with $\overline{OE}$ and Flow-Through Pinout	20	4.2	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT574T	8-Bit Register with $\overline{OE}$ and Flow-Through Pinout	20	5.2	6.2			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT646T	8-Bit Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT648T	8-Bit Inverting Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO

Note: Please contact a Cypress Representative for product availability.

FCT-T Logic Family (continued)

Octal High Drive Logic Products (V_{CC}=5 Volts) (continued)

Part Number	Organization	Pins	Propagation Delay (ns) C Com'l	C Mil	B Com'l	B Mil	A Com'l	A Mil	Standard Com'l	Standard Mil	Package
CY54/74FCT652T	8-Bit Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT821T	10-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5			D, L, P, Q, SO
CY54/74FCT823T	9-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5			D, L, P, Q, SO
CY54/74FCT825T	8-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5			D, L, P, Q, SO
CY54/74FCT827T	10-Bit Buffer with $\overline{OE}$	24	4.4	5.0	5.0	6.5	8.0	9.0			D, L, P, Q, SO
CY54/74FCT841T	10-Bit Latch with $\overline{OE}$	24	5.5	6.3	6.5	7.5	9.0	10.0			D, L, P, Q, SO

Bus Switch

Part Number	Organization	Pins	Propagation Delay (ns) Com'l	Packages
CYBUS3384	10-Bit Bus Switch	24	0.25	D, L, P, Q, SO

Octal Logic Products with Resistor (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delay (ns) C Com'l	C Mil	B Com'l	B Mil	A Com'l	A Mil	Standard Com'l	Standard Mil	Packages
CY54/74FCT2240T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.3				4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2244T	8-Bit Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.8	5.1	6.5	7.0	D, L, P, Q, SO
CY54/74FCT2245T	8-Bit Transceiver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.6	4.9	7.0	7.5	D, L, P, Q, SO
CY54/74FCT2257T	Quad 2-input Multiplexers with $\overline{OE}$ and 25Ω Resistor	16	4.3				5.0	5.8	6.0	7.0	D, L, P, Q, SO
CY54/74FCT2373T	8-Bit Latch with $\overline{OE}$ and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2374T	8-Bit Register with $\overline{OE}$ and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2541T	8-Bit Buffer/Line Driver with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.1	4.6			4.8	5.1	8.0	9.0	D, L, P, Q, SO
CY54/74FCT2543T	8-Bit Latched Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.5	6.1			6.5	7.5	8.5	10.0	D, L, P, Q, SO
CY54/74FCT2573T	8-Bit Latch with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5	D, L, P, Q, SO
CY54/74FCT2574T	8-Bit Register with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0	D, L, P, Q, SO
CY54/74FCT2646T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2648T	8-Bit Inverting Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2652T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0	D, L, P, Q, SO
CY54/74FCT2827T	10-Bit Buffer with $\overline{OE}$ and 25Ω Resistor	24	4.4	5.0	5.0	6.5	8.0	9.0			D, L, P, Q, SO

Note: Please contact a Cypress Representative for product availability.

FCT-T Logic Family (continued)

16-Bit High Drive Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delay (ns) C Com'l	B Com'l	A Com'l	Standard Com'l	Package
CY74FCT16240T	16-Bit Inverting Buffer/Line Driver with $\overline{OE}$	48	4.3		4.8	8.0	PA, PV
CY74FCT16244T	16-Bit Buffer/Line Driver with $\overline{OE}$	48	4.1		4.8	6.5	PA, PV
CY74FCT16245T	16-Bit Transceiver with $\overline{OE}$	48	4.1		4.6	7.0	PA, PV
CY74FCT16373T	16-Bit Latch with $\overline{OE}$	48	4.2		5.2	8.0	PA, PV
CY74FCT16374T	16-Bit Register with $\overline{OE}$	48	5.2		6.5	10.0	PA, PV
CY74FCT16444T	16-Bit 244 with Single $\overline{OE}$	48	4.1		4.8	6.5	PA, PV
CY74FCT16445T	16-Bit 245 with Single $\overline{OE}$ and DIR	48	4.1		4.6	7.0	PA, PV
CY74FCT16500T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT16501T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT16543T	16-Bit Latched Transceiver with $\overline{OE}$	56	5.3		6.5	8.5	PA, PV
CY74FCT16646T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT16652T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT16823T	18-Bit Register with $\overline{OE}$	56	6.0	7.5	10.0		PA, PV
CY74FCT16827T	20-Bit Buffer with $\overline{OE}$	56	4.4	5.0	8.0		PA, PV
CY74FCT16841T	20-Bit Latch with $\overline{OE}$	56	5.5	6.5	9.0		PA, PV
CY74FCT16952T	16-Bit Registered Transceiver	56	6.3	7.5	10.0		PA, PV

16-Bit Balanced Drive Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delay (ns) C Com'l	B Com'l	A Com'l	Standard Com'l	Package
CY74FCT162240T	16-Bit Inverting Buffer/Line Driver with $\overline{OE}$	48	4.3		4.8	8.0	PA, PV
CY74FCT162244T	16-Bit Buffer/Line Driver with $\overline{OE}$	48	4.1		4.8	6.5	PA, PV
CY74FCT162245T	16-Bit Transceiver with $\overline{OE}$	48	4.1		4.6	7.0	PA, PV
CY74FCT162373T	16-Bit Latch with $\overline{OE}$	48	4.2		5.2	8.0	PA, PV
CY74FCT162374T	16-Bit Register with $\overline{OE}$	48	5.2		6.5	10.0	PA, PV
CY74FCT162500T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT162501T	18-Bit Universal Bus Transceiver	56	4.6		5.1		PA, PV
CY74FCT162543T	16-Bit Latched Transceiver with $\overline{OE}$	56	5.3		6.5	8.5	PA, PV
CY74FCT162646T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT162652T	16-Bit Registered Transceiver with $\overline{OE}$	56	5.4		6.3	9.0	PA, PV
CY74FCT162823T	18-Bit Register with $\overline{OE}$	56	6.0	7.5	10.0		PA, PV
CY74FCT162827T	20-Bit Buffer with $\overline{OE}$	56	4.4	5.0	8.0		PA, PV
CY74FCT162841T	20-Bit Latch with $\overline{OE}$	56	5.5	6.5	9.0		PA, PV
CY74FCT162952T	16-Bit Registered Transceiver	56	6.3	7.5	10.0		PA, PV

Note: Please contact a Cypress Representative for product availability.

FCT-T Logic Family (continued)

16-Bit Balanced Drive, Bus Hold Logic Products (V_{CC}=5 Volts)

Part Number	Organization	Pins	Propagation Delay (ns) C Com'l	B Com'l	A Com'l	Standard Com'l	Package
CY74FCT162H244T	16-Bit Buffer/Line Driver with $\overline{OE}$ with Bus Hold	48	4.1		4.8	6.5	PA, PV
CY74FCT162H245T	16-Bit Transceiver with $\overline{OE}$ with Bus Hold	48	4.1		4.6	7.0	PA, PV
CY74FCT162H501T	18-Bit Universal Bus Transceiver with Bus Hold	56	4.6		5.1		PA, PV
CY74FCT162H952T	16-Bit Registered Transceiver with Bus Hold	56	6.3	7.5	10.0		PA, PV

Package Code:

A = Thin Quad Flat Pack (TQFP)
B = Plastic Pin Grid Array
D = CerDIP
E = Tape Automated Bond (TAB)
F = Flatpack
G = Pin Grid Array (PGA)
H = Windowed Hermetic LCC
J = PLCC
K = Cerpack
L = Leadless Chip Carrier (LCC)
Q = Windowed LCC
Q = QSOP
R = Windowed PGA
S = SOIC
T = Windowed Cerpack
U = Ceramic Quad Flatpack
V = SOJ
W = Windowed Cerdip
X = DICE
HD = Hermetic DIP (Module)
HG = Ceramic PGA (Module)
PA = TSSOP
PD = Plastic DIP (Module)
PM = Plastic SIMM
PN = Plastic Angled SIMM
PS = Plastic SIP
PV = SSOP
PZ = Plastic ZIP
SO = SOIC

Notes:

Military temperature range (-55×C to +125×C) product processed to MIL-STD-883 Revision C is also available for most products. Speed and power selections may vary from those above. Contact your local sales office for more information.

Commercial grade product is available in plastic, CerDIP, or LCC. Military grade product is available in CerDIP, LCC, or PGA.

Power supplies for most product lines are V_{CC} = 5V ± 10%.

22S, 24S, 28S stands for 300 mil. 22-pin, 24-pin, 28-pin, respectively. 28.4 stands for 28-pin 400 mil, 24.4 stands for 24-pin 400 mil.

PLCC, SOJ, and SOIC packages are available on some products.

F, K, and T packages are special order only.
Please contact a Cypress representative for product availability.

Note: Please contact a Cypress Representative for product availability.