PC System Timing Synthesizer Power-on-Reset

Introduction

This Application Brief outlines the Power-On-Reset (POR) sequence of events that occur within typical Cypress Semiconductor PC System Timing Synthesizers. It is intended to provide system designers with an explanation of the POR events that occur in the devices. This will enable system designers to correctly implement these devices in their systems with reliable results.

This discussion applies to synthesizers that use a 3.3V power supply for the PLL, core logic and some of the clock output buffers, such as PCI, 3V66 etc. Most devices also use a 2.5V power supply for some of the timing signal output buffers, such as CPU, CPU/2 and IOAPIC. In the general case there is no requirement on power supply sequencing but it is assumed that the power supplies ramp up together at a monotonic rate.

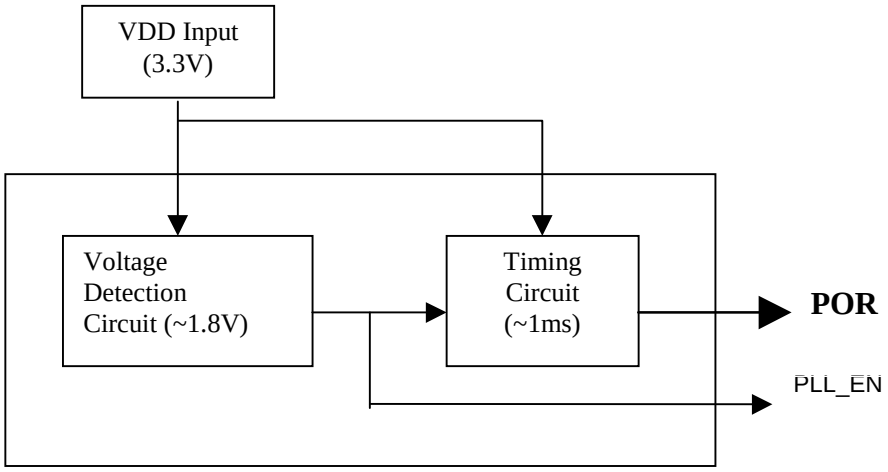

Figure 1. Block Diagram: Power-On-Reset (POR) Generator Block

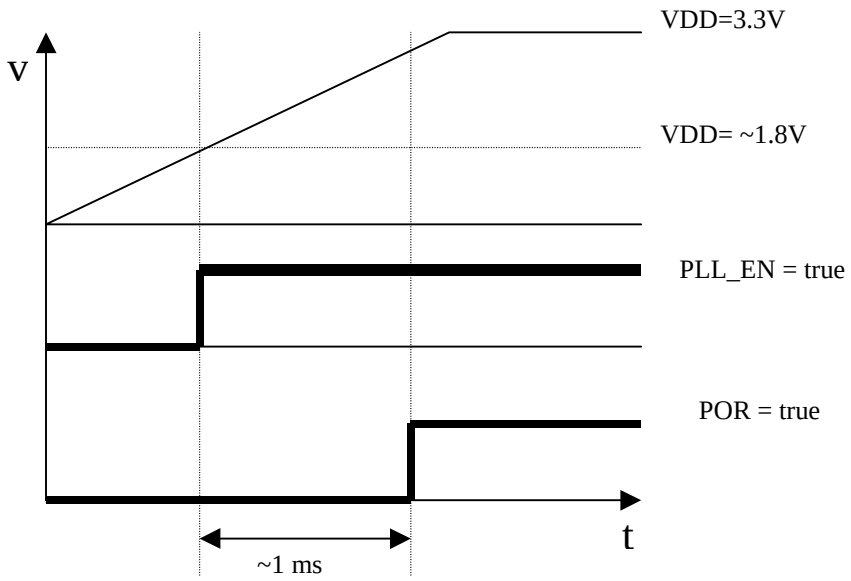

Figure 2. Timing Diagram: Power-On-Reset (not drawn to scale)

POR Sequence

The POR sequence is triggered when the 3.3V supply crosses approximately 1.8V. At this voltage level the Voltage Detection Circuit asserts the PLL_EN signal and starts the sequence of powering up the circuitry of the Clock Synthesizer PLL and the 1ms Timing Circuit. The PLL_EN control signal resets the internal PLL logic and enables the PLL to start from a known initial state. The Timing Circuit waits for –1 ms to permit the device PLL to acquire a stable, locked condition then asserts the POR signal. After the 1 ms time delay the PLL will be locked to the device's Reference signal and produce a stable output frequency. Most device data sheets specify up to 3ms delay (after power-up is detected at 1.8V) for frequency stabilization, to guarantee device settling time. The POR signal enables the clock output buffers to be released from the initial high-Z state and to be put into normal active mode, depending upon any other Output Enable (OE) control signals. Some devices use bi-directional (I/O) pins so that device control inputs can be latched during power-up, then the pin is available as a buffer output during normal operation after power-up. These inputs are latched when POR is asserted true, as shown in the timing diagram, then the pin is switched to function as an output buffer.

Power Supply Characteristics

In this power-on sequence it is required that the power supplies ramp up smoothly and monotonically. For the most reliable operation of PC systems the power supply ramp time should be approximately 6ms to 10ms. Very much faster or slower power supply ramp rates may cause unpredictable system initialization. Also, the monotonic ramp-up requirement is very important. If heavy current loads during system power-up causes the power supply outputs to glitch or droop then the System Timing Synthesizer outputs may be enabled before the power supply is stable. This may cause faulty operation of the system CPU or other devices. If, at any time, the power supply drops below
1.8V (usually referred to as a "brownout") then a complete new POR sequence will be triggered.

Conclusion

For reliable system start-up the system power supplies must ramp-up smoothly and monotonically. The System Timing Synthesizer device will detect power-up at ~1.8V, proceed through a power-on-reset procedure and then release the clock output buffers to provide system timing signals. The correct initialization and signal integrity of the clock output signals is dependent on the stability and quality of the system power supplies.