B9852

High Performance Pentium®III Clock Buffer

Product Features

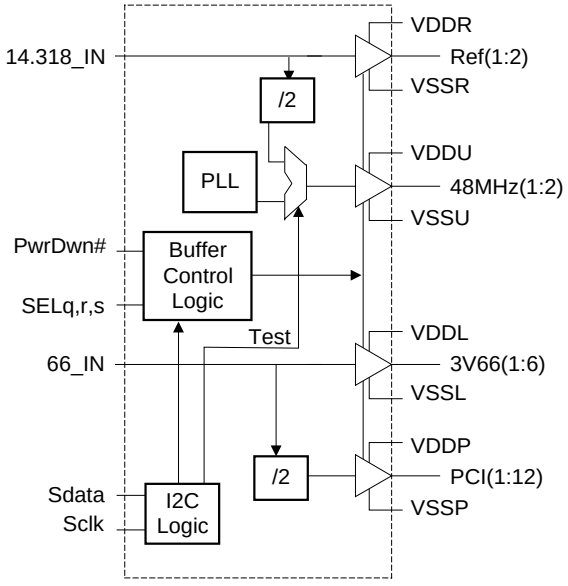
- Six 3V66 clocks
- Twelve 3V, 33 MHz PCI clocks
- Two 48 MHz clocks
- Two 14.318 MHz reference clocks
- Select logic, Hi-Z, and output disable modes
- Power Savings Clock OFF Mode
- 66 MHz reference input for PCI and 3V66 clocks
- 14.318 reference input for REF and 48M clocks
- 56 Pin SSOP and TSSOP Package

Frequency Selection Table

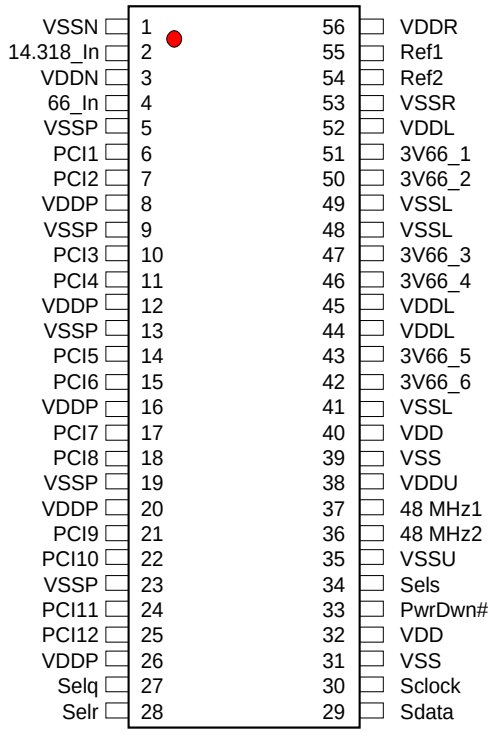
SELq	SELr	SELs	Description
0	0	0	All outputs on
0	0	1	PCI(1:8) off in low state
0	1	0	PCI(1:6) off in low state
0	1	1	All PCI off
1	0	0	All outputs Hi-Z
1	0	1	3V66_1 off in low state
1	1	0	Ref(1:2) off in low state
1	1	1	48MHz1 off in low state

NOTE: all SEL changes cause glitch free output clock transitions to occur.

Block Diagram



Pin Configuration



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Pin Description

PIN No.	Pin Name	I/O	Description
55,54	Ref(1,2)	O	14.318 MHz 3.3V outputs
51, 50, 47, 46, 43, 42	3V66_(1:6)	O	Fixed frequency 66 MHz clocks at 3.3 volt. These are buffered copies of the 66_in clock.
37, 36	48 MHz(1:2)	O	Fixed frequency 48 MHz output clocks.
34, 28, 27	Selq, Selr, Sels	I	Select pins. Contain internal pull down resistors that will insure that the input is sensed as a logic low if it is left disconnected.
33	PwrDwn#	I	Invokes power-down mode. Active Low. Contains internal pull up resistors that will insure that the input is sensed as a logic high if it is left unconnected.
30, 29	Sclock, Sdata	I	SMBUS pins.
25, 24, 22, 21, 18, 17, 15, 14, 11, 10, 7, 6	PCI (1:12)	O	Fixed frequency 33 MHz 3 volt PCI bus clocks. These divide the 66_in clock by 2
4	66_In	I	Input for 3.3V 66 MHz reference clock.
2	14.318_In	I	Input for 14.318 MHz reference clock.
53	VSSR	P	Ground pin for Ref clock buffer.
56	VDDR	P	Power pin for Ref clock buffer.
52, 45, 44	VDDL	P	Power pins for 3V66 buffer.
41, 48, 49	VSSL	P	Ground pins for 3V66 buffer.
38	VDDU	P	Power pins for 48 MHz buffer.
35	VSSU	P	Ground pins for 48 MHz buffer.
26, 20, 16, 12, 8	VDDP	P	Power pins for PCI buffer.
23, 19, 13, 9, 5	VSSP	P	Ground pins for PCI buffer.
32, 40	VDD	P	Power pins for input circuit and core logic.
39, 31	VSS	P	Ground pins for core logic.
3	VDDN	P	Power pin for 14.318_IN and 66_IN.
1	VSSN	P	Ground pin for 14.318_IN and 66_IN.

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: 0ºC to +85ºC
Maximum ESD protection 2000V
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters (VDD = VDDN = VDDP = VDDU = VDDL = VDDR = 3.3V ±5%, , TA = 0ºC to +85ºC)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	Note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL	-66		-5	µA	For pins with internal Pull up resistors, Note 1 and Note 2
Input High Current (@VIL = VDD)	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	160	mA	Note 3
Static Supply Current	Isdd	-	-	400	µA	PwrDwn = LOW, Note 3
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin Inductance	Lpin	-	-	7	nH	

Note1: Applicable to input signals: Selq, Selr, Sels and , PwrDwn.
Note2: Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.
Note3: All outputs loaded as per table 3.

Output name	Max Load (in pF)
REF(1,2), 48MHz(1,2)	20
3V66(1:6), PCI(1:12)	30

Table 3.

Note:
All Buffer characterization data is specified with all outputs connected to those rated loads simultaneously.

AC Parameters

Characteristic	Symbol	Min	Max	Units	Notes
14.318_IN period	TPeriod	69.840	69.844	nS	1, 6
14.318_IN high time	THIGH	20.0	N/A	nS	2, 7
14.318_IN low time	TLOW	20.0	N/A	nS	3, 7
14.318_IN rise time	TRISE	1.0	4.0	nS	5
14.318_IN fall time	TFALL	1.0	4.0	nS	5
66_IN CLK period	TPeriod	15.0	16.0	nS	1, 6
66_IN CLK high time	THIGH	5.25	N/A	nS	2, 7
66_IN CLK low time	TLOW	5.05	N/A	nS	3, 7
66_IN CLK rise time	TRISE	0.5	2.0	nS	5
66_IN CLK fall time	TFALL	0.5	2.0	nS	5
Ref (1,2) period	TPeriod	69.840	69.844	nS	1, 6, 9
Ref (1,2) high time	THIGH	20.0	N/A	nS	2, 7, 9
Ref (1,2) low time	TLOW	20.0	N/A	nS	3, 7, 9
Ref (1,2) rise time	TRISE	1.0	4.0	nS	5
Ref (1,2) fall time	TFALL	1.0	4.0	nS	5
48MHz CLK period	TPeriod	20.082	20.084	nS	1, 6, 9
48MHz CLK high time	THIGH	7.57	N/A	nS	2, 7
48MHz CLK low time	TLOW	7.17	N/A	nS	3, 7
48MHz CLK rise time	TRISE	1.0	4.0	nS	5
48MHz CLK fall time	TFALL	1.0	4.0	nS	5
3V66 CLK period	TPeriod	15.0	16.0	nS	1, 6, 8
3V66 CLK high time	THIGH	5.25	N/A	nS	2, 7, 8
3V66 CLK low time	TLOW	5.05	N/A	nS	3, 7, 8
3V66 CLK rise time	TRISE	0.5	2.0	nS	5
3V66 CLK fall time	TFALL	0.5	2.0	nS	5
PCI CLK period	TPeriod	30.0	N/A	nS	1, 6, 8
PCI CLK high time	THIGH	12.0	N/A	nS	2, 7, 8
PCI CLK low time	TLOW	12.0	N/A	nS	3, 7, 8
PCI CLK rise time	TRISE	0.5	2.0	nS	5
PCI CLK fall time	TFALL	0.5	2.0	nS	5

AC Parameters

Characteristic	Symbol	133 MHz CPU		100 MHz CPU		Units	Notes
		Min	Max	Min	Max		
Output enable delay (all outputs)	tpZL, tpZH	1.0	10.0	1.0	10.0	nS	
Output disable delay (all outputs)	tpLZ, tpHZ	1.0	10.0	1.0	10.0	nS	
All clock Stabilization from power-up	Tstable		3		3	mS	4

Notes:

1. Period, jitter, offset and skew measured on rising edge @1.5V.
2. THIGH is measured at 2.4V.
3. TLOW is measured at 0.4V for all outputs.
4. The time specified is measured from when VDD achieves its nominal operating level (typical condition VDD = 3.15V) till the frequency output is stable and operating within specification.
5. TRISE and TFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.0V JEDEC Specification.
6. The average period over any 1 uS period of time must be greater than the minimum specified period.
7. Calculated at minimum edge-rate (1V/nS) to guarantee 45/55% duty-cycle. Pulsewidth is required to be wider at faster edge-rate to ensure duty-cycle specification is met.
8. Conditional upon all 66_IN CLK specification being met.
9. Conditional upon all 14.318_IN specification being met.

Group Skew and Jitter Limits

Output Group	Pin-Pin Skew or Pair-to-Pair Skew MAX	Cycle-Cycle Jitter	Duty Cycle	Nom VDD	Skew, Jitter Measure Points
48 MHz	N/A	350 pS	45/55	3.3 V	1.5 V
3V66	250 pS	300 pS	45/55	3.3 V	1.5 V*
PCI	500 pS	500 pS	45/55	3.3 V	1.5 V*
REF	N/A	1000 pS	45/55	3.3 V	1.5 V*

*Inputs 66_IN and 14.318_IN jitter and duty cycle must be in 45-55% range and less than 200 pS respectively.

Group Offset Limits

Group	Offset	Measurement Loads (Lumped)	Measure Point
3V66 to PCI	1.5-3.5 nS 3V66 leads	3V66@ 30 pF, PCI @ 30 pF	3V66@ 1.5V, PCI @ 1.5 V

Notes:

1. All offsets are measured at a 1.5 volt level on their rising edges.

Device Test Mode

This device implements a test mode to enhance board level testing. When this mode is enabled the internal PLL is bypassed and the clock that is present on the 14.318_IN is divided by 2 and presented on the 48M1 and 48M2 clock output pins. This function is accessed via the devices SMBUS interface. The feature is enabled by setting Byte 4 Bit 0 to a logic 0 level.

2-Wire SMBUS Control Interface

The 2-wire control interface implements a write slave only interface according to SMBUS specification. (See fig5, page6). The device can be read back by using standard SMBUS command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions, and previously set control registers are retained.

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The "@ Power Up" (@Pup) column gives the state at true power up. Bytes are set to the values shown only on true power up.

The serial bits will be read by the clock driver in the following order:

Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (reserved and N/A) will be designated "don't care". They must be sent and will be acknowledged

Serial Control Registers (Cont.)

Byte 0: Active/Inactive Register (1 = enable, 0 = Stopped Low)

Bit	Name	Pin #	@ Pup	Description
7	PCI1	6	1	1=Active, 0=Inactive
6	PCI2	7	1	1=Active, 0=Inactive
5	PCI3	10	1	1=Active, 0=Inactive
4	PCI4	11	1	1=Active, 0=Inactive
3	PCI5	14	1	1=Active, 0=Inactive
2	PCI6	15	1	1=Active, 0=Inactive
1	PCI7	17	1	1=Active, 0=Inactive
0	PCI8	18	1	1=Active, 0=Inactive

Byte 1: Active/Inactive Register (1 = enable, 0 = Stopped Low)

Bit	Name	Pin#	@ Pup	Description
7	PCI9	21	1	1=Active, 0=Inactive
6	PCI10	22	1	1=Active, 0=Inactive
5	PCI11	24	1	1=Active, 0=Inactive
4	PCI12	25	1	1=Active, 0=Inactive
3	48 MHz_2	36	1	1=Active, 0=Inactive
2	48 MHz_1	37	1	1=Active, 0=Inactive
1	Ref2	54	1	1=Active, 0=Inactive
0	Ref1	55	1	1=Active, 0=Inactive

Byte 2: Active/Inactive Register (1 = enable, 0 = Stopped Low)

Bit	Name	Pin#	@ Pup	Description
7	3V66_6	42	**1**	1=Active, 0=Inactive
6	3V66_5	43	1	1=Active, 0=Inactive
5	3V66_4	46	1	1=Active, 0=Inactive
4	3V66_3	47	1	1=Active, 0=Inactive
3	3V66_2	50	1	1=Active, 0=Inactive
2	3V66_1	51	1	1=Active, 0=Inactive
1	-	-	x	Reserved (Intel)
0	-	-	x	Reserved (Intel)

Byte 3: Active/Inactive Register

Bit	Name	Pin#	@ Pup	Description
7	-	-	**x**	Reserved (Intel)
6	-	-	x	Reserved (Intel)
5	-	-	x	Reserved (Intel)
4	-	-	x	Reserved (Intel)
3	-	-	x	Reserved (Intel)
2	-	-	x	Reserved (Intel)
1	-	-	x	Reserved (Intel)
0	-	-	x	Reserved (Intel)

Byte 4: Active/Inactive Register

Bit	Name	Pin#	@ Pup	Description
7	-	-	**x**	Reserved
6	-	-	x	Reserved
5	-	-	x	Reserved
4	-	-	x	Reserved
3	-	-	x	Reserved
2	-	-	x	Reserved
1	-	-	x	Reserved
0	-	-	1	1=normal, 0=test mode

Notes:
Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operations.

The "@ Power Up" (@Pup) column defines the state of the bits in these registers immediately after the device has been powered up. X is a "don't care" condition.

When "test mode" is enabled (Byte 4 Bit 0 is set true (logic low) state, the 48MHz output clocks become 7.159 MHz (REF/2) clocks. These clocks are then defined from the REF clock (14.318MHz in).

Buffer Characteristics

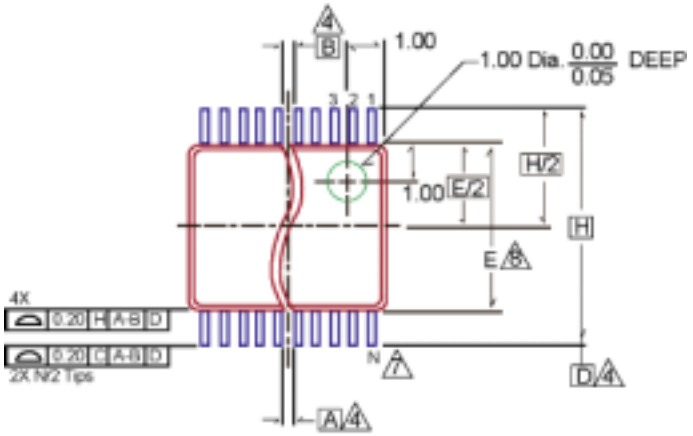
Buffer Characteristics for 48 MHz(1:2) and Ref(1:2)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-11	-16	-	mA	VDD-0.5
Pull-Up Current	IOH_2	-30	-40	-	mA	1.5V
Pull-Down Current	IOL_1	13	18	-	mA	0.4V
Pull-Down Current	IOL_2	32	42	-	mA	1.5V
Output Impedance	Z0	20		60	Ω	

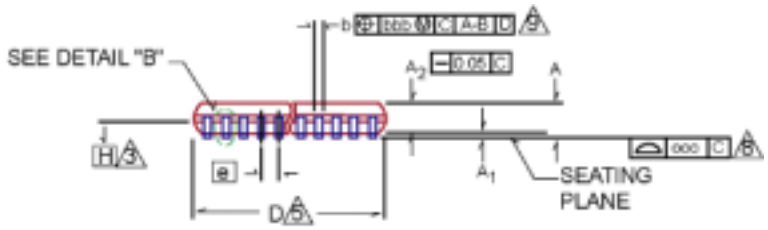
Buffer Characteristics for PCI(1:10), 3V66(1:6)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-14	-20	-	mA	VDD-0.5
Pull-Up Current	IOH_2	-44	-57	-	mA	1.5V
Pull-Down Current	IOL_1	18	25	-	mA	0.4V
Pull-Down Current	IOL_2	50	65	-	mA	1.5V
Output Impedance	Z0	12		55	Ω	

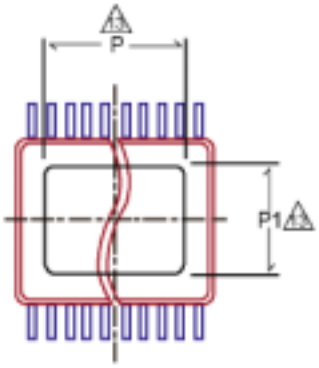
Package Drawing and Dimensions (56 Pin TSSOP)



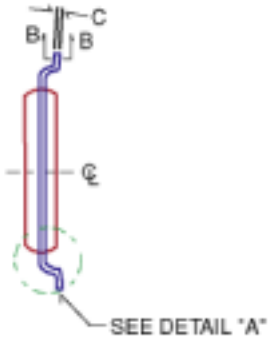
TOP VIEW



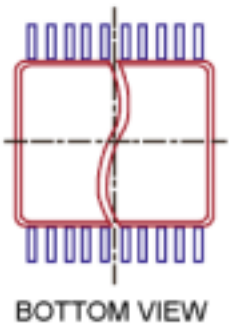
SIDE VIEW



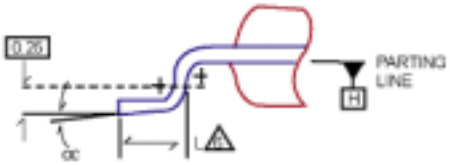
EXPOSED PAD VIEW



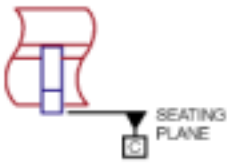
END VIEW



BOTTOM VIEW

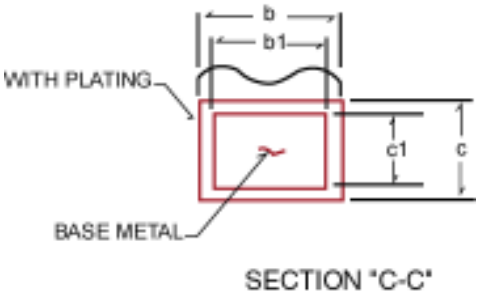


DETAIL "A"

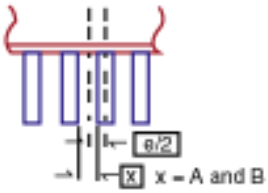


DETAIL "B"

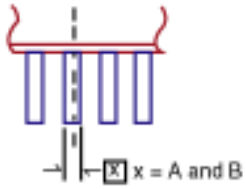
Package Drawing and Dimensions (Cont.)



SECTION "C-C"



EVEN LEAD SIDES
TOPVIEW



ODD LEAD SIDES
TOPVIEW

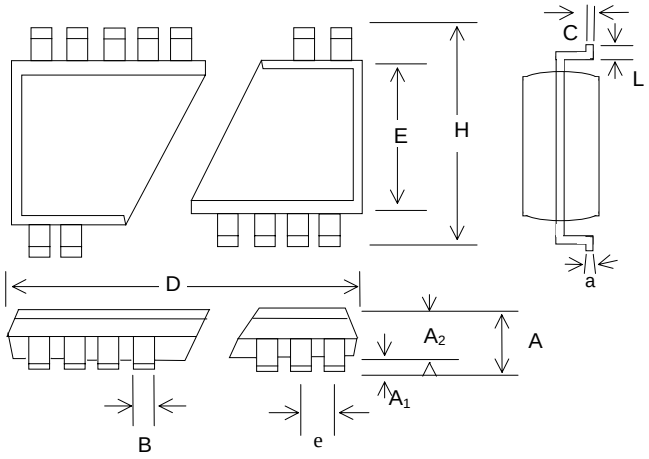
56 Pin TSSOP Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.043	-	-	1.10
A1	.00197	.00394	.0059	0.05	0.10	0.15
A2	0.0335	0.0354	0.0374	0.85	0.90	0.95
000		0.00394			0.10	
b	0.0067	-	0.106	0.17	-	0.27
b1	0.0067	0.0079	0.0091	0.17	0.20	0.23
bbb		0.0031			0.08	
c	0.0035	-	0.0079	0.09	-	0.20
c1	0.0035	0.0050	0.0063	0.09	0.127	0.16
θ	0°	-	8°	0°	-	8°
e		0.0197 BSC			0.50 BSC	
H		0.3189 BSC			8.10 BSC	
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.236	0.240	0.244	6.00	6.10	6.20
L	0.0197	0.236	0.0295	0.50	0.60	0.75

Notes:

1. Die thickness allowable is 0.279 +/- 0.0127 (0.0110 +/- .005 inches)
2. Dimensions & tolerance per ASME. Y14, 5M-1994.
3. Datum Plane H located at mold parting line and coincident with lead. Where lead exits plastic body at bottom of parting line.
4. Datums A-B and D to be determined where centerline between leads exits plastic body at Datum Plane H.
5. "D" and "E" are reference datums and do not include mode flash or protrusions, and are measured at the bottom parting line. Mold flash or protrusions shall not exceed 0.15mm on D and 0.25mm on E per side.
6. Dimension is the length of terminal for soldering to a substrate.
7. Terminal positions are shown for reference only.
8. Formed leads shall be planar with respect to one another within 0.076mm at seating plane.
9. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the lead width dimension located on the lower radius or the foot. Minimum space between protrusions and an adjacent lead to be 0.08mm for 0.50mm pitch.
10. Section "C-C" to be determined at 0.10 to 0.25mm from the lead tip.
11. This part is compliant with JEDEC specification MO-153, variations DB, DC, DE ED, EE, and FE.

Package Drawing and Dimensions (56 Pin SSOP)



56 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	.720	.725	.730	18.29	18.42	18.54
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

Ordering Information

Part Number	Package Type	Production Flow
B9852AYB	56 Pin SSOP	Commercial, 0ºC to +85ºC
B9852ATB	56 Pin TSSOP	Commercial, 0ºC to +85ºC

Marking: Example: Cypress
B9852
Date Code, Lot #

B9852AYB

Flow
B = Commercial, 0ºC to + 85ºC

Package
Y = SSOP
T = TSSOP

Revision

Device Number

Notice

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