

Product Features

- 160MHz Clock Support
- LVCMOS/LVTTL Compatible Inputs
- 9 Clock Outputs: Drive up to 18 Clock Lines
- Synchronous Output Enable
- Output Tri-state Control
- 350ps Maximum Output-to-Output Skew
- Pin Compatible with MPC947
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin TQFP Package

Description

The B9947 is a low voltage clock distribution buffer with the capability to select one of two LVCMOS/LVTTL compatible clock inputs. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The nine outputs are 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9947 has an effective fan-out of 1:18. The outputs can also be tri-stated via the tri-state input TS#. Low output-to-output skews make the B9947 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The B9947 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram

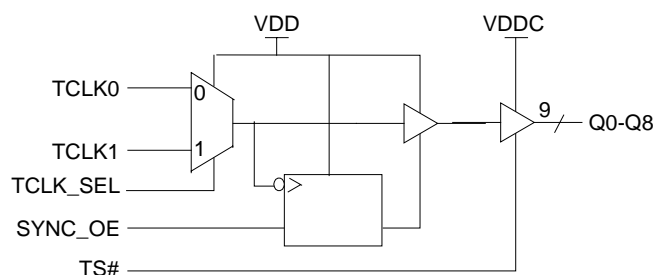
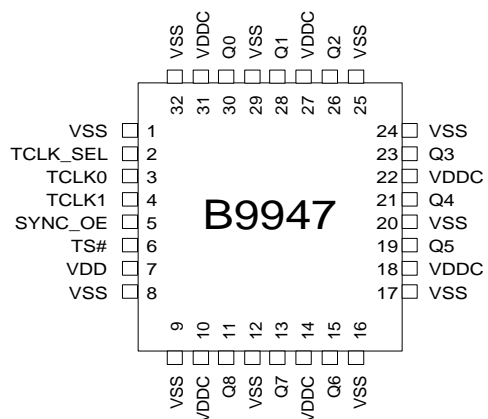


Figure 1

Pin Configuration



**Pin Description**

PIN	NAME	PWR	I/O	Description
3	TCLK0		I, PU	Test Clock Input.
4	TCLK1		I, PU	Test Clock Input.
2	TCLK_SEL		I, PU	Test Clock Select Input. When low, TCLK0 is selected. When asserted high, TCLK1 is selected.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q(8:0)	VDDC	O	Clock Outputs.
5	SYNC_OE		I, PU	Output Enable Input. When asserted high, the outputs are enabled and when set low the outputs are disabled in a low state.
6	TS#		I, PU	Tri-state Control Input. When asserted low, the output buffers are tri-stated. When set high, the output buffers are enabled.
10, 14, 18, 22, 27, 31	VDDC			3.3V Power Supply for Output Clock Buffers.
7	VDD			3.3V Power Supply
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	VSS			Common Ground

PU = Internal Pull-Up.

3.3V, 160MHz, 1:9 Clock Distribution Buffer

Maximum Ratings

Maximum Input Voltage Relative to VSS: $V_{SS} - 0.3V$
 Maximum Input Voltage Relative to VDD: $V_{DD} + 0.3V$
 Storage Temperature: $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature: $-40^{\circ}C$ to $+85^{\circ}C$
 Maximum ESD protection: 2KV
 Maximum Power Supply: 5.5V
 Maximum Input Current: $\pm 20mA$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage		V_{SS}		0.8	V	
Input High Voltage		2.0		V_{DD}	V	
Input Low Current (@ $V_{IL} = V_{SS}$)	I_{IL}			-100	μA	Note 1
Input High Current (@ $V_{IH} = V_{DD}$)	I_{IH}			10	μA	
Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 20mA$, Note 2
Output High Voltage	V_{OH}	2.5			V	$I_{OH} = -20mA$, $V_{DDC} = 3.3V$ Note 2
Quiescent Supply Current	I_{DD}	-	1	2	mA	All V_{DDC} and V_{DD}
Input Capacitance	C_{in}	-	-	4	pF	
$V_{DDC} = 3.3V \pm 10\%$, $V_{DD} = 3.3V \pm 10\%$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$						

Note 1: Inputs have pull-up resistors that effect input current

Note 2: Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

AC Parameters¹

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Fmax	Maximum Input Frequency ²	160			MHz	
Tpd	TCLK to Q Delay ²	4.75	-	9.25	ns	
FoutDC	Output Duty Cycle ^{2,3}	TCYCLE/2 – 800		TCYCLE/2 + 800	ps	Measured at VDDC/2
tpZL, tpZH	Output enable time (all outputs)	2		10	ns	
tpLZ, tpHZ	Output disable time (all outputs)	2		10	ns	
Tskew	Output-to-Output Skew ^{2,5}			350	ps	
Tskew (pp)	Part to Part Skew ⁶			2.0	ns	
Ts	Setup Time ^{2,4}	0.0			ps	SYNC_OE to TCLK
Th	Hold Time ^{2,4}	1.0			ps	TCLK to SYNC_OE
Tr / Tf	Output Clocks Rise / Fall Time ⁵	0.20		1.0	ns	0.8V to 2.0V
VDDC = 3.3V +/- 10%, VDD = 3.3V +/- 10%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.

Note 2: Outputs driving 50Ω transmission lines.

Note 3: 50% input duty cycle.

Note 4: Setup and Hold times are relative to the falling edge of the input clock

Note 5: Outputs loaded with 30pF each

Note 6: Part to Part Skew at a given temperature and voltage

Output Enable/ Disable

The B9947 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted low, the outputs are disabled in a low state. When SYNC_OE is set high, the outputs are enabled as shown in Figure 2.

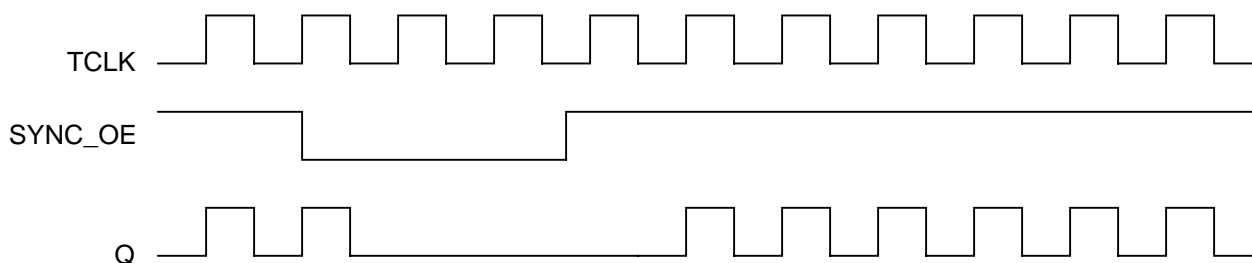
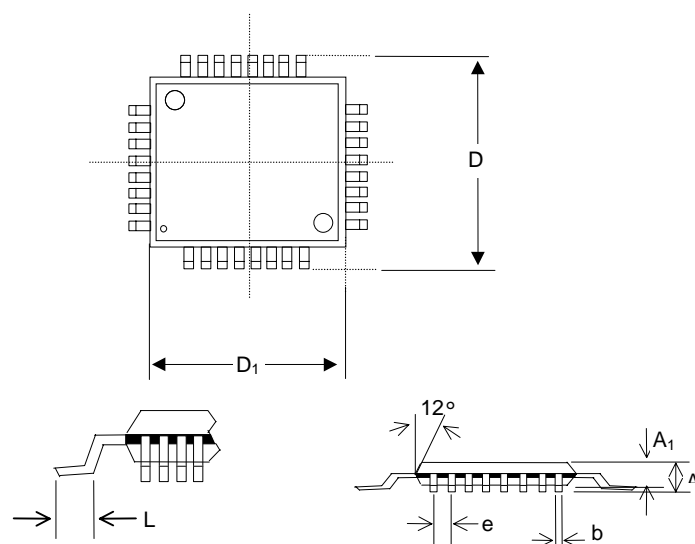


Figure 2. SYNC_OE Timing Diagram

Package Drawing and Dimensions



32 Pin TQFP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A ₁	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D ₁	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75



B9947

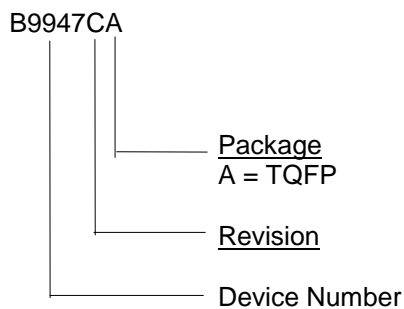
3.3V, 160MHz, 1:9 Clock Distribution Buffer

Ordering Information

Part Number	Package Type	Production Flow
B9947CA	32 PIN TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
B9947CA
Date Code, Lot #



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**B9947****3.3V, 160MHz, 1:9 Clock Distribution Buffer****Document Title:** B9947 3.3V, 160 MHz, 1:9 Clock Distribution Buffer**Document Number:** 38-07078

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107114	06/06/01	IKA	Convert from IMI to Cypress
*A	108058	07/03/01	NDP	Changed Commercial to Industrial (See page 6)