B9948

3.3V, 160MHz, 1:12 Clock Distribution Buffer

Product Features

- 160MHz Clock Support
- LVPECL or LVCMOS/LVTTL Clock Input
- LVCMOS/LVTTL Compatible Inputs
- 12 Clock Outputs: Drive up to 24 Clock Lines
- Synchronous Output Enable
- Output Tri-state Control
- 350ps Maximum Output-to-Output Skew
- Pin Compatible with MPC948
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin TQFP Package

Description

The B9948 is a low voltage clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The twelve outputs are 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9948 has an effective fan-out of 1:24. The outputs can also be tri-stated via the tri-state input TS#. Low output-to-output skews make the B9948 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The B9948 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram

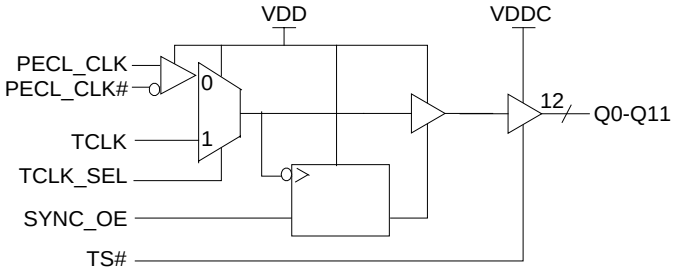
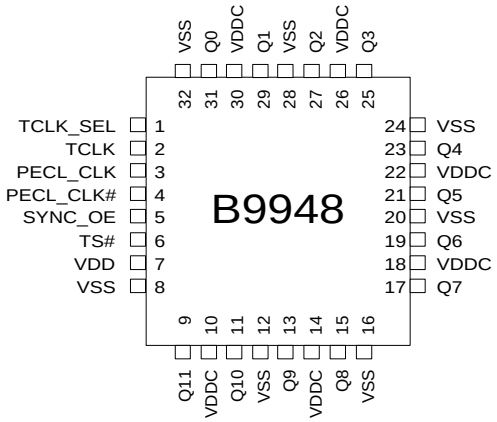


Figure 1

Pin Configuration



Cypress Semiconductor Corporation
525 Los Coches St.
Milpitas, CA 95035. Tel: 408-263-6300, Fax: 408-263-6571
http://www.cypress.com

Pin Description

PIN	NAME	PWR	I/O	Description
3	**PECL_CLK**		I, PU	PECL Input Clock.
4	**PECL_CLK#**		I, PD	PECL Input Clock.
2	**TCLK**		I, PU	External Reference/Test Clock Input.
9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	**Q(11:0)**	VDDC	O	Clock Outputs.
1	**TCLK_SEL**		I, PU	Clock Select Input. When low, PECL clock is selected and when high TCLK is selected.
5	**SYNC_OE**		I, PU	Output Enable Input. When asserted high, the outputs are enabled and when set low the outputs are disabled in a low state.
6	**TS#**		I, PU	Tri-state Control Input. When asserted low, the output buffers are tri-stated. When set high, the output buffers are enabled.
10, 14, 18, 22, 26, 30	**VDDC**			3.3V Power Supply for Output Clock Buffers.
7	**VDD**			3.3V Power Supply
8, 12, 16, 20, 24, 28, 32	**VSS**			Common Ground

PD = Internal Pull-Down, PU = Internal Pull-Up.

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: -40°C to +85°C
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V
Maximum Input Current: ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	1.49	-	1.825	V	PECL_CLK, Single Ended
		VSS		0.8		All other inputs
Input High Voltage	VIH	2.135	-	2.42	V	PECL_CLK, Single Ended
		2.0		VDD		All other inputs
Input Low Current (@VIL = VSS)	IIL			-100	µA	Note 1
Input High Current (@VIL =VDD)	IIH			100	µA	
Peak-to-Peak Input Voltage PECL_CLK	VPP	300		1000	mV	Note 2
Common Mode Range PECL_CLK	VCMR	VDD-2.0	-	VDD-0.6	V	
Output Low Voltage	VOL			0.4	V	IOL = 20mA, Note 3
Output High Voltage	VOH	2.5			V	IOH = -20mA, VDDC = 3.3V Note 3
Quiescent Supply Current	IDD	-	1	2	mA	All VDDC and VDD
Input Capacitance	Cin	-	-	4	pF	
VDDC = 3.3V ±10%, VDD = 3.3V ±10%, TA = -40°C to +85°C						

Note 1: Inputs have pull-up resistors that effect input current, PECL_CLK# has a pull-down resistor.
Note 2: The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the VCMR range and the input lies within the VPP specification.
Note 3: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Fmax	Maximum Input Frequency[2]	160			MHz	
Tpd	PECL_CLK to Q Delay[2]	4.0	-	8.0	ns	
	TCLK to Q Delay[2]	4.4	-	8.9		
FoutDC	Output Duty Cycle[2,3]	TCYCLE/2 – 800		TCYCLE/2 + 800	ps	Measured at VDDC/2
tpZL, tpZH	Output enable time (all outputs)	2		10	ns	
tpLZ, tpHZ	Output disable time (all outputs)	2		10	ns	
Tskew	Output-to-Output Skew[2,5]			350	ps	
Tskew (pp)	Part to Part Skew [6]			1.5	ns	PECL_CLK to Q
				2.0		TCLK to Q
Ts	Setup Time[2,4]	1.0			ns	SYNC_OE to PECL_CLK
		0.0				SYNC_OE to TCLK
Th	Hold Time[2,4]	0.0			ns	PECL_CLK to SYNC_OE
		1.0				TCLK to SYNC_OE
Tr / Tf	Output Clocks Rise / Fall Time[5]	0.2		1.0	ns	0.8V to 2.0V
VDDC = 3.3V +/- 10%, VDD = 3.3V +/- 10%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
Note 2: Outputs driving 50Ω transmission lines.
Note 3: 50% input duty cycle.
Note 4: Setup and Hold times are relative to the falling edge of the input clock
Note 5: Outputs loaded with 30pF each
Note 6: Part to Part Skew at a given temperature and voltage

Output Enable/ Disable

The B9948 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted low, the outputs are disabled in a low state. When SYNC_OE is set high, the outputs are enabled as shown in Figure 2.

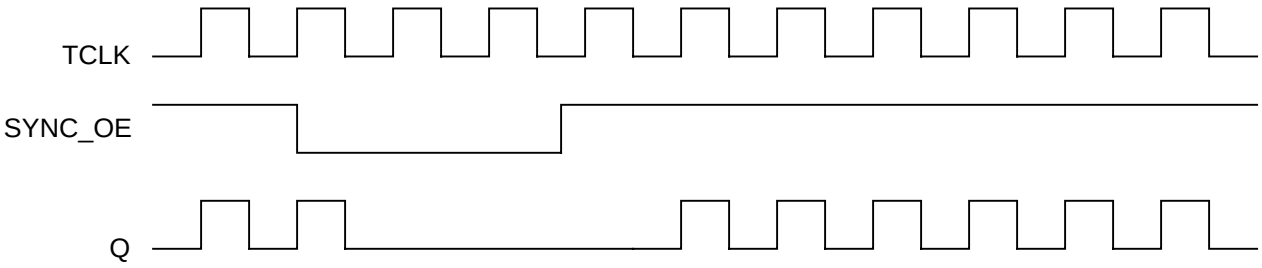
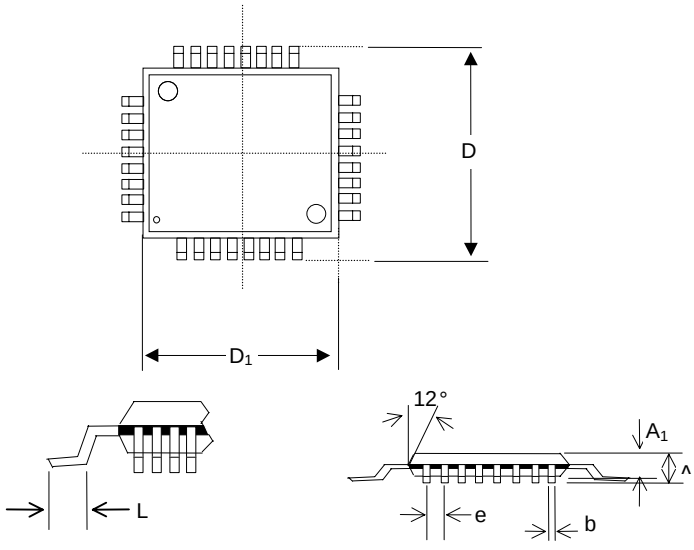


Figure 2. SYNC_OE Timing Diagram

Package Drawing and Dimensions



32 Pin TQFP Outline Dimensions

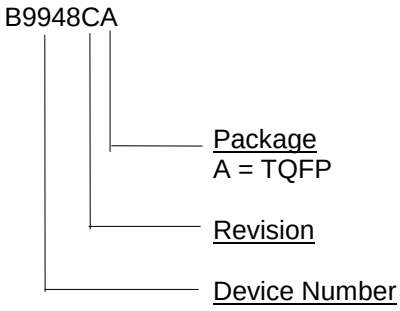
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D_1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
B9948CA	32 PIN TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
B9948CA
Date Code, Lot #



Notice

Cypress Semiconductor Corporation reserves the right to make changes to its products in order to improve design, performance or reliability. Cypress Semiconductor Corporation assumes no responsibility for the use of its products in life supporting and medical applications where the failure or malfunction of the product could cause failure of the life supporting and medical systems. Products are not authorized for use in such applications unless a written approval is requested by the manufacturer and an approval is given in writing by Cypress Semiconductor Corporation for the use of its products in the life supporting and medical applications.

Document Title: B9948 3.3V, 160 MHz, 1:12 Clock Distribution Buffer
Document Number: 38-07079

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107115	06/06/01	IKA	Convert from IMI to Cypress
*A	108060	07/03/01	NDP	Changed Commercial to Industrial (See page 6)