B9949

3.3V, 160MHz, 1:15 Clock Distribution Buffer

Product Features

- 160MHz Clock Support
- LVPECL or LVCMOS/LVTTL Clock Input
- LVCMOS/LVTTL Compatible Inputs
- 15 Clock Outputs: Drive up to 30 Clock Lines
- 1X and 1/2X Configurable Outputs
- Output Tri-state Control
- 350ps Maximum Output-to-Output Skew
- Pin Compatible with MPC949
- Industrial Temp. Range: -40°C to +85°C
- 52-Pin TQFP Package

Description

The B9949 is a low voltage clock distribution buffer with the capability to select either a differential LVPECL or LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 15 outputs are 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9949 has an effective fan-out of 1:30.

The B9949 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:D) inputs allow flexibility in selecting the ratio of 1X to1/2X outputs.

The B9949 outputs can also be tri-stated via MR/OE# input. When MR/OE# is set high, it resets the internal flip-flops and tri-states the outputs.

Block Diagram

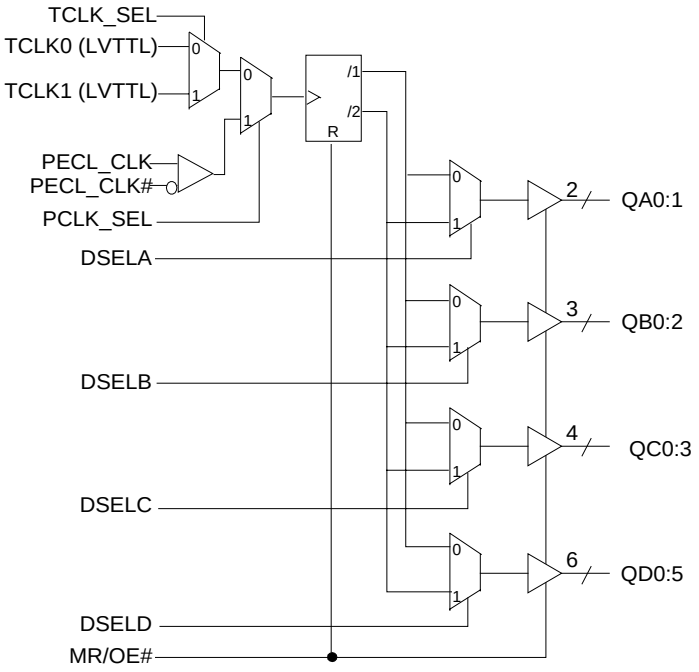
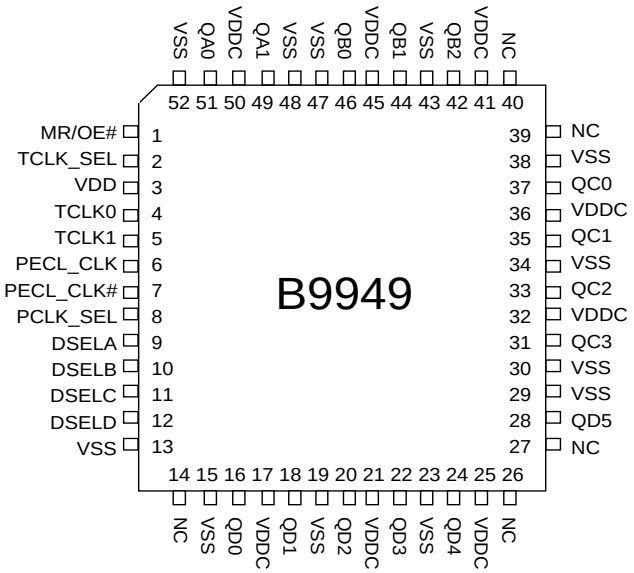


Figure 1

Pin Configuration



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Pin Description

PIN	NAME	PWR	I/O	Description
6	**PECL_CLK**		I, PD	PECL Input Clock.
7	**PECL_CLK#**		I, PU	PECL Input Clock.
4, 5	**TCLK(0,1)**		I, PU	External Reference/Test Clock Input.
49, 51	**QA(1,0)**	VDDC	O	Clock Outputs.
42, 44, 46	**QB(2:0)**	VDDC	O	Clock Outputs.
31, 33, 35, 37	**QC(3:0)**	VDDC	O	Clock Outputs.
16, 18, 20, 22, 24, 28	**QD(5:0)**	VDDC	O	Clock Outputs.
9, 10, 11, 12	**DSEL(A:D)**		I, PD	Divider Select Inputs. When high, selects ÷2 input divider. When low, selects ÷1 input divider.
2	**TCLK_SEL**		I, PD	TCLK Select Input. When low, TCLK0 clock is selected and when high TCLK1 is selected.
8	**PCLK_SEL**		I, PD	PECL Select Input. When high, PECL clock is selected and when low TCLK(0,1) is selected
1	**MR_OE#**		I, PD	Output Enable Input. When asserted low, the outputs are enabled and when asserted high, internal flip-flops are reset and the outputs are tri-stated.
17, 21, 25, 32, 36, 41, 45, 50	**VDDC**			3.3V Power Supply for Output Clock Buffers.
3	**VDD**			3.3V Power Supply
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	**VSS**			Common Ground
14, 26, 27, 39, 40,	**NC**			Not Connected

PD = Internal Pull-Down, PU = Internal Pull-Up.

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: -40°C to +85°C
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V
Maximum Input Current: ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	1.49	-	1.825	V	PECL_CLK, Single Ended
		VSS		0.8		All other inputs
Input High Voltage	VIH	2.135	-	2.42	V	PECL_CLK, Single Ended
		2.0		VDD		All other inputs
Input Low Current (@VIL = VSS)	IIL			-100	µA	Note 1
Input High Current (@VIL =VDD)	IIH			100	µA	
Peak-to-Peak Input Voltage PECL_CLK	VPP	300		1000	mV	Note 2
Common Mode Range PECL_CLK	VCMR	VDD-2.0	-	VDD-0.6	V	
Output Low Voltage	VOL			0.4	V	IOL = 20mA, Note 3
Output High Voltage	VOH	2.5			V	IOH = -20mA, VDDC = 3.3V Note 3
Quiescent Supply Current	IDD	-	1	2	mA	All VDDC and VDD
Input Capacitance	Cin	-	-	4	pF	
VDDC = 3.3V ±5%, VDD = 3.3V ±5%, TA = -40°C to +85°C						

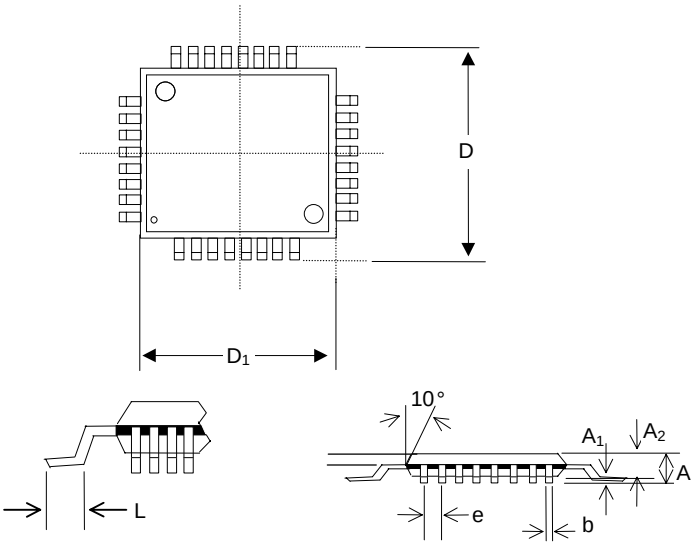
Note 1: Inputs have pull-up/pull-down resistors that effect input current.
Note 2: The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification.
Note 3: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Fmax	Maximum Input Frequency[2]	160			MHz	
Tpd	PECL_CLK to Q Delay[2]	4.0	-	8.6	ns	
	TCLK to Q Delay[2]	4.2	-	10.5		
FoutDC	Output Duty Cycle[2,3]	TCYCLE/2 – 1		TCYCLE/2 + 1	ns	Measured at VDDC/2
tpZL, tpZH	Output enable time (all outputs)	2		10	ns	
tpLZ, tpHZ	Output disable time (all outputs)	2		10	ns	
Tskew	Output-to-Output Skew[2,4]			350	ps	Fin<130MHz
Tskew (pp)	Part to Part Skew [5]		1.5	2.75	ns	PECL_CLK to Q
			2.0	4.0		TCLK to Q
Tr / Tf	Output Clocks Rise / Fall Time[4]	0.10		1.0	ns	0.8V to 2.0V
VDDC = 3.3V +/- 5%, VDD = 3.3V +/- 5%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
Note 2: Outputs driving 50Ω transmission lines.
Note 3: 50% input duty cycle.
Note 4: Outputs loaded with 30pF each
Note 5: Part to Part Skew at a given temperature and voltage

Package Drawing and Dimensions (52 TQFP)



52 Pin TQFP Outline Dimensions

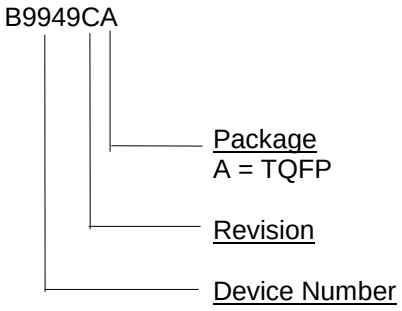
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.472	-	-	12.00	-
D_1	-	0.394	-	-	10.00	-
b	0.009	-	0.015	0.22	-	0.38
e	0.026 BSC			0.65 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
B9949CA	52 PIN TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
B9949CA
Date Code, Lot #



Notice

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Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107117	06/06/01	IKA	Convert from IMI to Cypress
*A	108062	07/03/01	NDP	Changed Commercial to Industrial