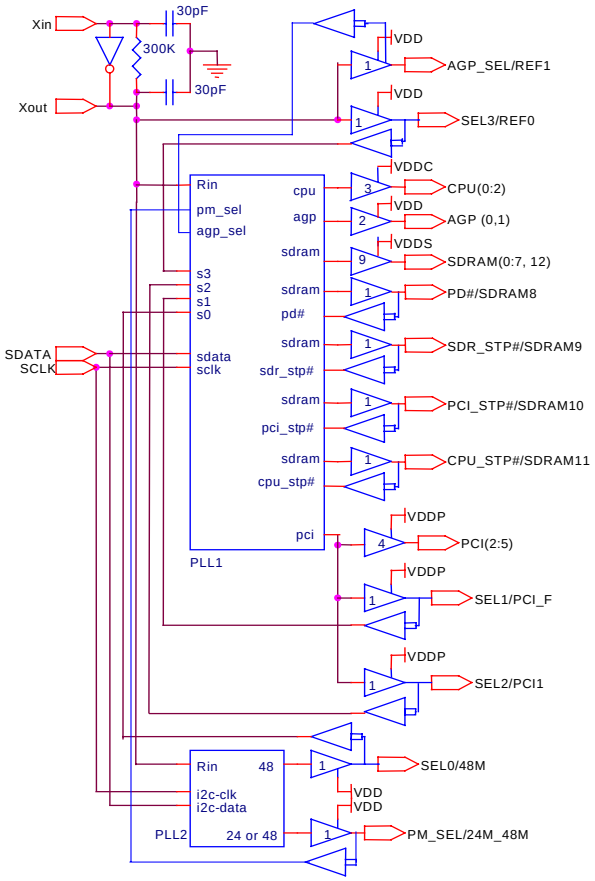
C9631

Low EMI 166MHz Clock Generator for SiS630S/Pentium®III/Celeron® Chipsets

Product Features

- 166MHz Clock Support
- Supports Pentium® III and Celeron CPU's
- Designed to SiS630S Chipset Requirements
- 3 CPU Clocks
- 13 SDRAM Clocks (3 DIMM Support)
- 6 PCI Clocks, One free running
- 2 AGP Clocks
- 2 REF Clocks (1x or 2x strength via SMBus)
- 1 48MHz USB Clock (Non SSC)
- 1 Programmable SIO 24MHz/ 48MHz (Non SSC)
- Cypress Spread Spectrum for best EMI reduction
- SMBus Support with read back capabilities
- Dial-A-Frequency™ Feature
- Dial-A-dB™ Feature
- 48 Pin SSOP package

Block Diagram



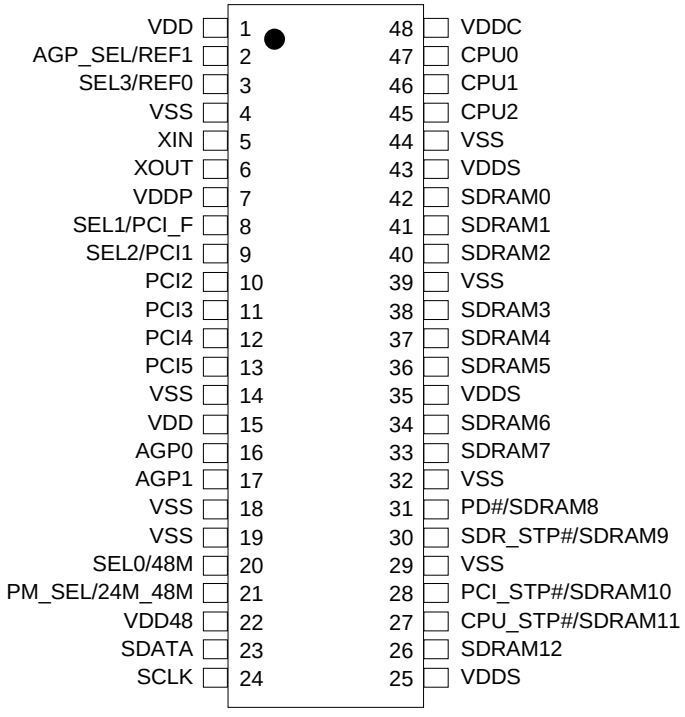
Frequency Table (MHz)

SEL (3:0)*	CPU (0:2)	SDRAM (0:12)	PCI (_F, 1:5)	REF (0:1)	AGP(0,1)	
					AGP_SEL=0	AGP_SEL=1
0000	66.67	66.67	33.34	14.31	66.67	50.00
0001	100.00	100.00	33.33	14.31	66.67	50.00
0010	166.67	166.67	33.33	14.31	66.67	55.56
0011	133.30	133.30	33.33	14.31	66.65	49.99
0100	66.67	100.01	33.34	14.31	66.67	50.00
0101	100.00	66.67	33.33	14.31	66.67	50.00
0110	100.00	133.33	33.33	14.31	66.67	50.00
0111	133.30	99.98	33.33	14.31	66.65	49.99
1000	112.00	112.00	33.60	14.31	67.20	56.00
1001	124.00	124.00	31.00	14.31	62.00	46.50
1010	138.00	138.00	34.50	14.31	69.00	51.75
1011	150.00	150.00	30.0	14.31	60.00	50.00
1100	66.67	133.34	33.34	14.31	66.67	50.00
1101	100.00	150.00	30.00	14.31	60.00	50.00
1110	150.00	100.00	30.00	14.31	60.00	50.00
1111	160.00	120.00	30.00	14.31	60.00	48.00

Table 1

* Can also be programmed via SMBus interface.

Pin Configuration



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Pin Description

Pin	Name	PWR	I/O	TYPE	Description
5	**XIN**	VDD	I		Oscillator Buffer Input. Connect to a crystal or to an external clock.
6	**XOUT**	VDD	O		Oscillator Buffer Output. Connect to a crystal. Do not connect when an external clock is applied at XIN.
2	**AGP_SEL/REF1**	VDD	I/O	PD	Power-on Bi-directional Input / Output. At power-up, AGP_SEL is the input. When the power supply voltage exceeds the input buffer threshold voltage, REF1 becomes the buffered output of XIN. AGP-SEL selects the AGP(0,1) output frequency. See Frequency Table. REF1 is the buffered output of XIN. Select 1x or 2x strength via SMBus Byte6 Bit 7. Default is 1x.
20	**SEL0/48M**	VDD	I/O	PD	Power-on Bi-directional Input / Output. At power-up, SEL0 is the input. When the power supply voltage exceeds the input buffer threshold voltage, 48M becomes the output. See Frequency Table for SEL0 selections. 48M is a 48MHz clock output.
8	**SEL1/PCI_F**	VDD	I/O	PD	Power-on Bi-directional Input / Output. At power-up, SEL1 is the input. When the power supply voltage exceeds the input buffer threshold voltage, PCI_F becomes the free Running PCI Clock output. See Frequency Table for SEL1 selections. PCI_F is the free running PCI clock. This clock is not affected by PCI_STP#.
9	**SEL2/PCI1**	VDD	I/O	PD	Power-on Bi-directional Input / Output. At power-up, SEL2 is the input. When the power supply voltage exceeds the input buffer threshold voltage, PCI1 becomes the output. See frequency Table for SEL2 selections.
3	**SEL3/REF0**	VDD	I/O	PD	Power-on Bi-directional Input / Output. At power-up, SEL3 is the input. When the power supply voltage exceeds the input buffer threshold voltage, REF0 becomes the buffered output of XIN. See Frequency Table for SEL3 selections. REF0 is the buffered output of XIN. Select 1x or 2x strength via SMBus Byte6 Bit 7. Default is 1x.
21	**PM_SEL/24M_48M**	VDD	I/O	PD	Power-on Bi-directional Input / Output. At power-up, PM_SEL is the input. When the power supply voltage exceeds the input buffer threshold voltage, 24M_48M becomes the output. If PM_SEL = 0, then pins 27,28,30,31 are SDRAM clocks. If PM_SEL = 1, then pins 27,28,30,31 are Power Management pins. 24M_48M is SIO/USB clock output. It is programmable to 24MHz or 48MHz clock output. Default is 24MHz, but also provide 48MHz by programming SMBus.

Pin Description (Cont.)

Pin	Name	PWR	I/O	TYPE	Description
27	**CPU_STP#/ SDRAM11**	VDD	I/O	PU	Bi-directional Input / Output. If PM_SEL = 0, then SDRAM11 is the output. If PM_SEL = 1, then CPU_STP# is the input. When CPU_STP# = 0, CPU clock is stopped.
28	**PCI_STP#/ SDRAM10**	VDD	I/O	PU	Bi-directional Input / Output. If PM_SEL = 0, then SDRAM10 is the output. If PM_SEL = 1, then PCI_STP# is the input. When PCI_STP# = 0, then PCI(1:5) clock outputs are set low.
30	**SDR_STP#/ SDRAM9**	VDD	I/O	PU	Bi-directional Input / Output. If PM_SEL = 0, then SDRAM9 is the output. If PM_SEL =1, then SDR_STP# is the input. When SDR_STP# = 0, then SDRAM(0:12) clock outputs are set low.
31	**PD#/SDRAM8**	VDD	I/O	PU	Bi-directional Input / Output. If PM_SEL = 0, then SDRAM8 is the output. If PM_SEL = 1, then PD# is the input. When PD# = 0, then all clock outputs are set low.
23	**SDATA**		I		Serial Data Input. Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
24	**SCLK**		I		Serial Clock Input. Conforms to the SMBus specification.
46, 47	**CPU(1,0)**	VDDC	O		Host Clock Outputs. See Frequency Table.
45	**CPU2**	VDDC	O		CPU Clock Output. This clock is used for the chipset. See Frequency Table.
26, 33, 34, 36, 37, 38, 40, 41, 42	**SDRAM (12, 7:0)**	VDDS	O		SDRAM Clock Outputs. Are synchronous to CPU clocks. See Frequency Table.
10, 11, 12, 13	**PCI(2:5)**	VDDP	O		PCI Clock Outputs. Are synchronous to CPU clocks. See Frequency Table.
16, 17	**AGP(0,1)**	VDD	O		AGP Clock Outputs. Are synchronous to CPU clocks. See Frequency Table
48	**VDDC**				2.5V Power Supply for CPU(0:2).
25, 35, 43	**VDDS**				3.3V Power Supply for SDRAM(0:12)
7	**VDDP**				3.3V Power Supply for PCI(_F, 1:5)
22	**VDD48**				3.3V Power Supply for 48M_USB, 24MHz-48MHz output.
1, 15	**VDD**				3.3V Common Power Supply
4, 14, 18, 19, 29, 32, 39, 44	**VSS**				Common Ground

A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

PU = Internal Pull-Up. PD = Internal Pull-Down. Typically 120K (70K to 170K).

Device Clock Phase Relationships

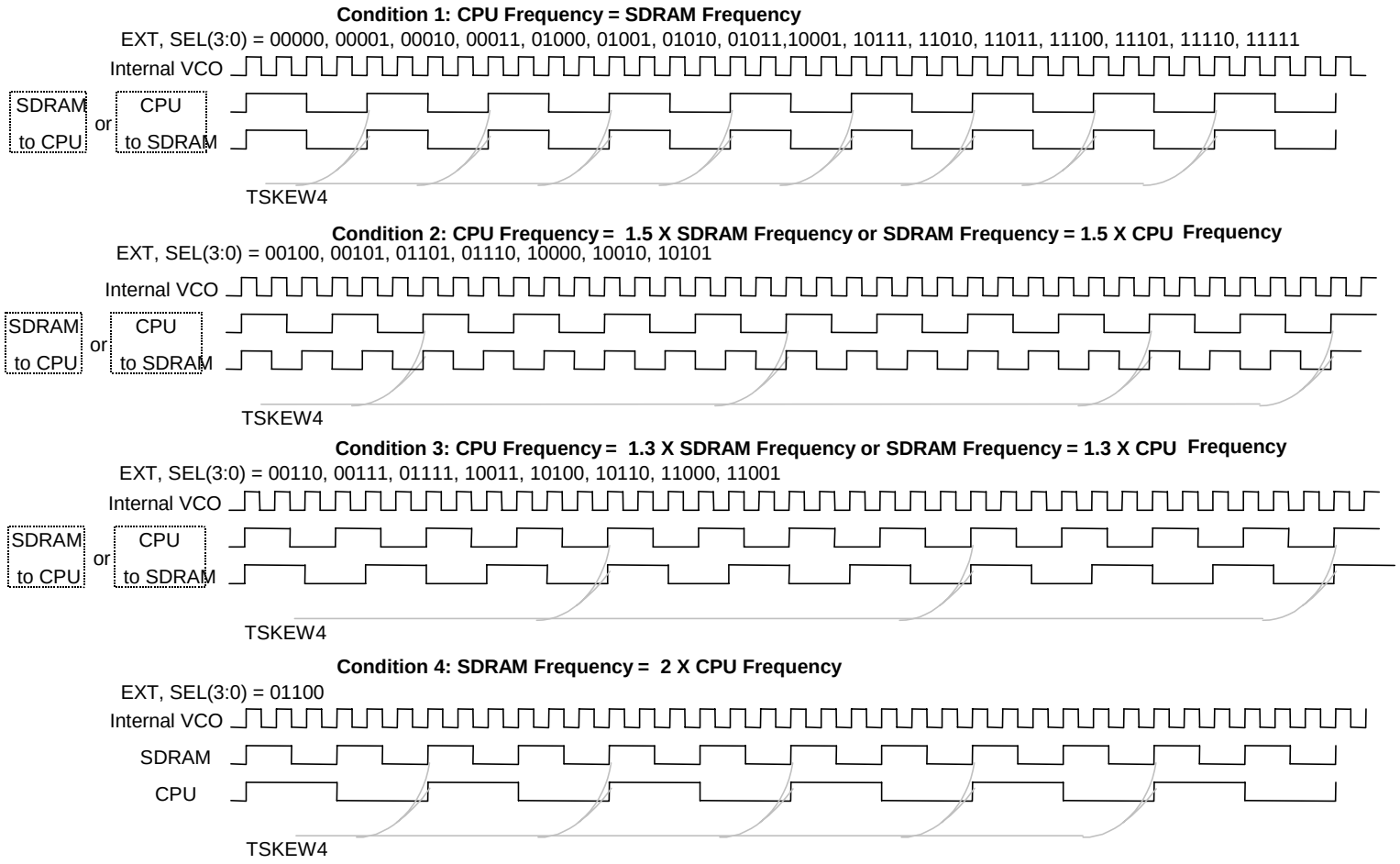


Figure 1

Frequency Smooth Switching Groups

Group	EXT, SEL(3:0) (Byte 0, Bits 2, 7, 6, 5, 4)
1	00000, 00100, 01100, 10000, 10101
2	00001, 00101, 00110, 10001, 10011, 10100, 10110, 11000, 11001
3	00010, 01011, 01110, 10010, 11111
4	00011, 00111, 01000, 01001, 01010, 01101, 01111, 10111, 11010, 11011, 11100, 11101, 11110

Table 2

Table 2 above describes 4 different groups of frequencies. Within the same group, frequency may be switched through SMBus byte 0 without causing any glitching or clock discontinuity at the CPU(0:2) outputs, therefore allowing frequency smooth switching of the clock.

Switching frequency from one group to another is permitted but will cause the CPU(0:2) clocks to jump immediately to the next frequency. (non smooth switching.).

Power on Bi-Directional Pins

Power Up Condition:

Pins 2, 3, 8, 9, 20, and 21are Power up Bi-directional pins used for selecting the host frequencies (Table 1), AGP clocks, and Power Management. During power-up of the device, these pins are in input mode (see Figure 2), therefore; they are considered input select pins internal to the IC. After the power supply voltage crosses the input threshold voltage, the input data is latch into the internal control register and these pins become outputs.

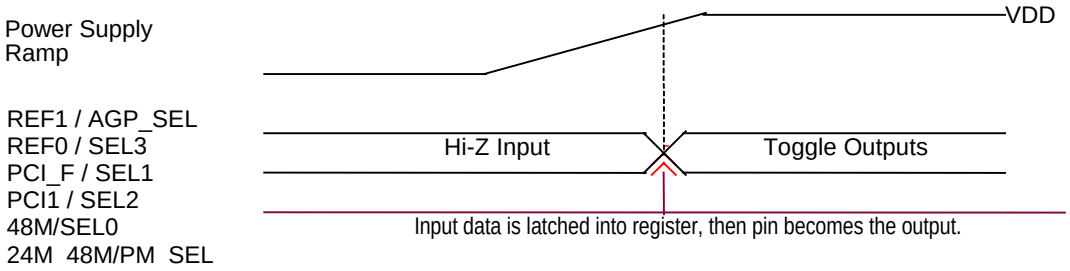


Figure 2

Strapping Resistor Options:

The power up bi-directional pins have a large value pull-down each (250KΩ), therefore, a selection "0" is the default. If the system uses a slow power supply (over 5mS settling time), then **it is recommended** to use an external Pull-Down (Rdn) in order to insure a Low selection. In this case, the designer may choose one of two configurations, see Figures 3a and 3b.

Figure 3a represents an additional pull down resistor Rdn = 50KΩ connected from the pin to the ground plane, which allows a faster pull to a low level.
If a selection "1" is desired, then a jumper is placed on JP1 to a Rup = 10KΩ resistor as implemented as shown in Figure 3a. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Figure 3b represent a single resistor 10KΩ connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 3 and 2.

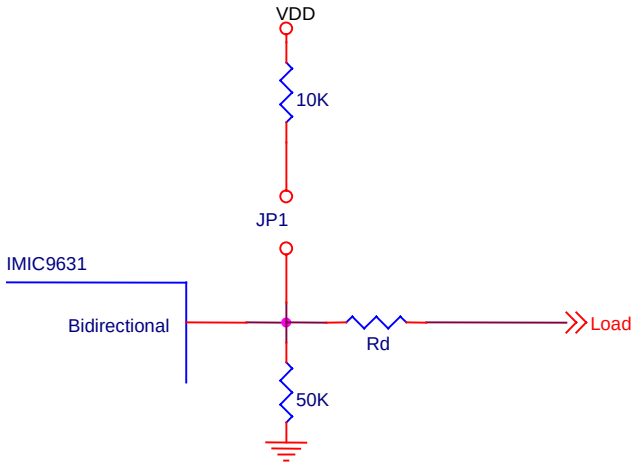


Figure 3a

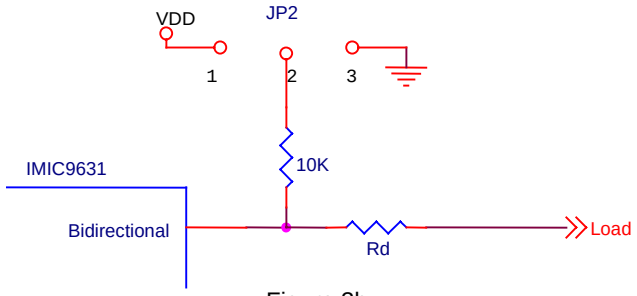


Figure 3b

Power Management Functions

Power Management on this device is controlled by the PD#, CPU_STP#, PCI_STP#, and SDR_STP# pins. When PD# is high (default) the device is in normal running mode and all signals are active. The PD# signal is used to bring all clocks to a low level in an orderly fashion. When in power down all outputs are synchronously stopped in a low state, all PLLs are shut off, and the crystal oscillator is disabled. When in shutdown, the SMBus function is also disabled. When the device is powered down through the SMBus interface by activating PD# the oscillator is not turned off. This will enable the user to power up the clock generator through SMBus.

CPU_STP#, PCI_STP#, and SDR_STP# are inputs to the clock generator and are used to turn off the CPU, PCI, and SDRAM clocks respectively. These inputs are made synchronous to the clock driver PCI_F output. Only one rising edge of PCI_F occurs after the clock control logic is switched for the output clocks to become enabled/disabled.

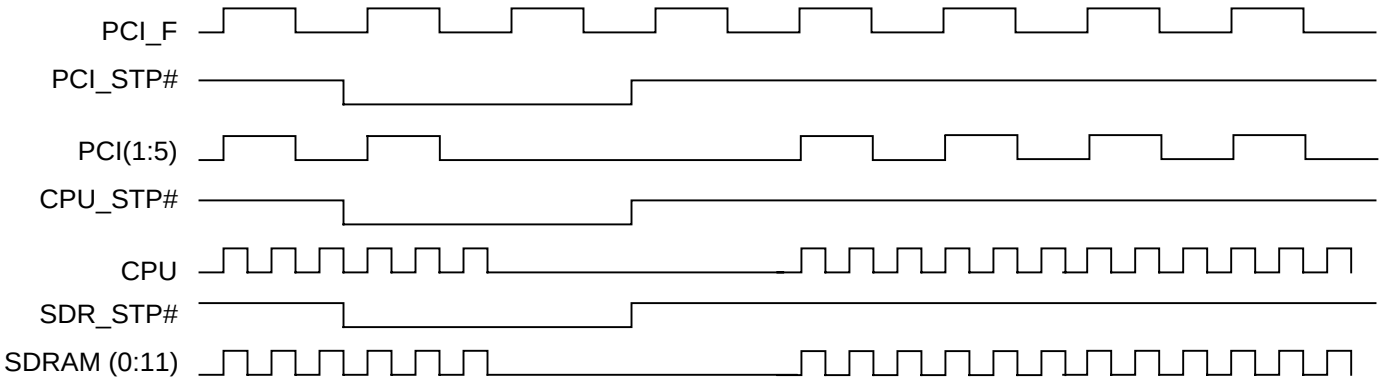


Figure 4

2-Wire SMBus Control Interface

The 2-wire control interface implements a read/write slave only interface according to SMBus specification (IC12, 1996). The device can be read back by using standard SMBus command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledgement is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 1 in read mode. R/W# = 0 in write mode.

A maximum of 10 bytes of data may be written/Read Data is transferred MSB first at a max rate of 100kbits/S.The device will not respond to any other control interface conditions.

In the Write mode (See figure 5a), the clock gen. acknowledges Address Byte, D2, then receives two additional bytes:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged. Subsequently, the below-described sequence (Byte 0, Byte 1, Byte2,) will be valid and acknowledged.

In the Read Mode (See figure 5b), the clock gen. acknowledges Address D3, and immediately transmits data starting with Byte count, then Byte 0, 1, 2, ... After each transmitted byte, this device waits for an acknowledge before transmitting the next byte.

Serial Control Registers

NOTE: Power up conditions for each bit are listed in the "@Pup" column.

Byte 0: Frequency, Function Select Register

Bit	@Pup	Pin#	Description	
7	0	-	SEL3 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
6	0	-	SEL2 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
5	0	-	SEL1 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
4	0	-	SEL0 (for frequency table 3, selection by software via SMBus), selection valid if bit3 = 1	
3	0	-	0 = frequency selected by hardware, pins 3, 8, 9, and 20	1 = frequency selection via SMBus byte0 bits 2, 7:4
2	0	-	EXT (for extended frequencies), selection valid if bit 3 = 1. Default = 0.	
1	1	-	0 = Spread Spectrum disabled	1 = Spread spectrum enabled
0	0	-	0 = Running	1 = Tri-state all outputs

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0), MSB0=MSB1 =1, SSTS = 1

EXT	SEL3	SEL2	SEL1	SEL0	Description					
Bit 2	Bit7	Bit6	Bit5	Bit4	CPU	SDRAM	PCI	AGP(0,1)		Spread Spectrum
								AGP_SEL=0	AGP_SEL=1	
0	0	0	0	0	66.67	66.67	33.34	66.67	50.00	0 to –0.5
0	0	0	0	1	100.0	100.0	33.33	66.67	50.00	0 to –0.5
0	0	0	1	0	166.7	166.6	33.33	66.67	55.56	+/- 0.25
0	0	0	1	1	133.3	133.3	33.33	66.65	49.99	0 to –0.5
0	0	1	0	0	66.67	100.1	33.34	66.67	50.00	0 to –0.5
0	0	1	0	1	100.0	66.67	33.33	66.67	50.00	0 to –0.5
0	0	1	1	0	100.0	133.3	33.34	66.67	50.00	+/-0.25
0	0	1	1	1	133.3	99.98	33.33	66.65	49.99	0 to –0.5
0	1	0	0	0	112.0	112.0	33.60	67.20	56.00	+/-0.25
0	1	0	0	1	124.0	124.0	31.00	62.00	46.50	0 to –0.5
0	1	0	1	0	138.0	138.0	34.50	69.00	51.75	+/-0.25
0	1	0	1	1	150.0	150.0	30.00	60.00	50.00	+/-0.25
0	1	1	0	0	66.67	133.3	33.34	66.67	50.00	+/-0.25
0	1	1	0	1	100.0	150.0	30.00	60.00	50.00	+/-0.25
0	1	1	1	0	150.0	100.0	30.00	60.00	50.00	0 to –0.5
0	1	1	1	1	160.0	120.0	30.00	60.00	48.00	0 to –0.5
1	0	0	0	0	66.80	100.2	33.40	66.80	50.10	+/-0.25
1	0	0	0	1	100.2	100.2	33.40	66.80	50.10	+/-0.25
1	0	0	1	0	166.7	111.1	33.33	66.67	55.56	+/-0.25
1	0	0	1	1	100.2	133.6	33.40	66.80	50.10	+/-0.25
1	0	1	0	0	75.00	100.0	37.50	60.00	50.00	+/-0.25
1	0	1	0	1	83.30	124.9	31.24	62.48	49.98	+/-0.25
1	0	1	1	0	105.0	140.0	35.00	70.00	52.50	+/-0.25
1	0	1	1	1	133.6	133.6	33.40	66.80	50.10	+/-0.25
1	1	0	0	0	110.3	147.1	36.77	73.53	55.15	+/-0.25
1	1	0	0	1	115.0	153.3	38.33	76.67	57.50	+/-0.25
1	1	0	1	0	120.0	120.0	30.00	60.00	45.00	+/-0.25
1	1	0	1	1	138.0	138.0	34.50	69.00	51.75	+/-0.25
1	1	1	0	0	140.0	140.0	35.00	70.00	52.50	+/-0.25
1	1	1	0	1	145.0	145.0	36.25	72.50	54.38	+/-0.25
1	1	1	1	0	147.5	147.5	36.88	73.75	55.31	+/-0.25
1	1	1	1	1	160.0	160.0	32.00	64.00	53.33	+/-0.25

Table 3

Serial Control Registers (Cont.)

Byte 1: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	21	24M_48M 1 = selects 24MHz (default) 0 = selects 48MHz
6	1	-	SSTS, See Table 6
5	1	-	MSB1. See Table 6
4	1	-	MSB0. See Table 6
3	1	47	CPU0 enable/stopped
2	1	46	CPU1 enable/stopped
1	1	45	CPU2 enable/stopped
0	1	-	Reserved for CYPRESS test

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	13	PCI5 enable/stopped
4	1	12	PCI4 enable/stopped
3	1	11	PCI3 enable/stopped
2	1	10	PCI2 enable/stopped
1	1	9	PCI1 enable/stopped
0	1	8	PCI_F enable/stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	33	SDRAM7 enable/Stopped
6	1	34	SDRAM6 enable/Stopped
5	1	36	SDRAM5 enable/Stopped
4	1	37	SDRAM4 enable/Stopped
3	1	38	SDRAM3 enable/Stopped
2	1	40	SDRAM2 enable/Stopped
1	1	41	SDRAM1 enable/Stopped
0	1	42	SDRAM0 enable/Stopped

Byte 4: Additional SDRAM Clock Register (1=enable, 0=Stopped)

Bit	@Pup	Pin#	Description
7	1	-	R5
6	1	21	24_48MHz enable/Stopped
5	1	20	48MHz enable/stopped
4	1	26	SDRAM12 enable/Stopped
3	1	27	SDRAM11 enable/Stopped
2	1	28	SDRAM10 enable/Stopped
1	1	30	SDRAM9 enable/Stopped
0	1	31	SDRAM8 enable/Stopped

Byte 5: AGP Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	3	SEL3, Readback H/W Strapping Status
6	0	9	SEL2, Readback H/W Strapping Status
5	0	8	SEL1, Readback H/W Strapping Status
4	0	20	SEL0, Readback H/W Strapping Status
3	1	2	REF1 enable/stopped
2	1	3	REF0 enable/stopped
1	1	17	AGP1 enable/stopped
0	1	16	AGP0 enable/stopped

*****Inverted read back of hardware settings.

Byte 6: Control Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	2,3	REF_1X2X_Control
6	0	45	CPU_STOP_Control. Controls CPU2 clock to stop/run when CPU_STP# is active.
5	0	2	AGP_SEL#
4	0	21	PM_SEL , Read Only
3	1	27	CPU_STP#
2	1	28	PCI_STP#
1	1	30	SDR_STP#
0	1	31	PD#

Byte 7: Vender Information / R Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	-	Vender Identity. See Table 5
6	1	-	Vender Identity. See Table 5
5	1	-	Vender Identity. See Table 5
4	0	-	PIN / R4*
3	0	-	PIN / R3*
2	0	-	PIN / R2*
1	0	-	PIN / R1*
0	0	-	PIN / R0, LSB*

PIN = Product ID number (read only)
*When R(4:0) are programmed into this register, they will override the PIN values.

Byte 8: Dial-a-Frequency™ N Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	0	-	N6
6	0	-	N5
5	0	-	N4
4	0	-	N3
3	0	-	N2
2	0	-	N1
1	0	-	N0 , LSB
0	0	-	1 = Enable SMBus N and R

TEST Function Table: Applicable only when Byte 1, bit0=0.

CPU (0:2)	PCI (0:6)	SDRAM (0:13)	REF(0,1)	48MHz	24_48MHz	AGP
= Xin / 3	= Xin / 8	= Xin / 2	= Xin	= Xin	= Xin / 2	= Xin/6

Table 4

Dial-a-Frequency™ Feature

SMBus Dial-a-frequency feature is available in this device via byte 6, byte 7, and byte 8. See Application Note AN-0025.

Dial-a-Frequency™ P Values Table

EXT, SEL(3:0)	P
00000, 00100, 01100, 10000, 10101	32005333
00001, 00101, 00110, 10001, 10011, 10100, 10110, 11000, 11001	48008000
00010, 01011, 01110, 10010, 11111	96016000
00011, 00111, 01000, 01001, 01010, 01101, 01111, 10111, 11010, 11011, 11100, 11101, 11110	64010667

SMBus Communication Waveform

For information regarding SMBus Communication Waveforms see Application Note AN-0022

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from (Figure 6a) or around the center (Figure 6b) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting SMBus byte0, bit1 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have SMBus accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SSTS and MBS(1,0) in I²C Byte 1 as indicated below in Table 6.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (eg.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Spread Spectrum Clock Generation (SSCG) (Cont.0

Spread Spectrum Selection Table

SSTS	MBS1	MBS0	Spread%
0	0	0	-0.25*
0	0	1	-1.0
0	1	0	-0.7**
0	1	1	-0.5
1	0	0	+/-0.125
1	0	1	+/- 0.5
1	1	0	+/- 0.35
1	1	1	See Table 3

Table 6

*Maximum frequency is offset by –0.125%
**Maximum frequency is offset by –0.15%

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V

Maximum Input Voltage Relative to VDD: VDD + 0.3V

Storage Temperature: -65°C to + 150°C

Operating Temperature: 0°C to +70°C

Maximum ESD protection 2KV

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters (VDD =VDDS=VDDP=VDD48= 3.3V ±5%, VDDC = 2.5V ±5%, TA = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	1.0	V	Note 2
Input High Voltage	VIH	2.2	-	-	V	
Input Low Current (@VIL = VSS)	IIL			-5	µA	For internal Pull down resistors, Notes 1,3
Input High Current (@VIL =VDD)	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	440	mA	
Dynamic Supply Current	Idd2.5V	-	-	40	mA	
Power Down Supply Current	Ipd3.3V			1	mA	PD# = '0'
Power Down Supply Current	Ipd2.5V			1	mA	PD# = '0'
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	XIN/XOUT	28	30	32	pF	Measured from Pin to Ground. Note 5
Crystal Startup time	Txs	-	-	40	µs	From Stable 3.3V power supply.

Note1: Applicable to SEL(0:3), AGP_SEL, PM_SEL, CPU_STP#, PCI_STP#, SDR_STP#,PD#.
Note2: Applicable to SDATA, SCLK.
Note3: Although internal pull-down resistors have a typical value of 120K, this value may vary between 70K and 170K.
Note4: All outputs loaded as per Table 4 below.
Note5: Although the device will reliably interface with crystals of a 15pF – 20pF C_L range, it is optimized to interface with a typical C_L = 16pF crystal specifications.

Clock Name	Max Load (in pF)
CPU, REF	20
PCI, SDRAM, AGP	30
24MHz, 48MHz	15

Table 4

AC Parameters

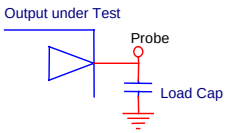
Symbol	Parameter	133 MHz Host		100 MHz Host		Units	Notes
		Min	Max	Min	Max		
TPeriod	CPU(0:2) period	7.5	8.0	10.0	10.5	ns	5, 6, 8
THIGH	CPU(0:2) high time	1.87	-	3.0	-	ns	6,10
TLOW	CPU(0:2) low time	1.67	-	2.8	-	ns	6, 11
Tr / Tf	CPU(0:2) rise and fall times	0.4	1.6	0.4	1.6	ns	6, 7
TSKEW0	Any CPU to Any CPU Skew time	-	175	-	175	ps	6, 8, 9
TCCJ	CPU(0:2) Cycle to Cycle Jitter	-	250	-	250	ps	6, 8, 9
TPeriod	SDRAM[0:12] period	7.5	8.0	10.0	10.5	ns	5, 6, 8
THIGH	SDRAM[0:12] high time	1.87	-	3.0	-	ns	6,10
TLOW	SDRAM[0:12] low time	1.67	-	2.8	-	ns	6, 11
Tr / Tf	SDRAM[0:12] rise and fall times	0.4	1.6	0.4	1.6	ns	6, 7
TSKEW1	Any SDRAM to Any SDRAM	-	250	-	250	ps	6, 8, 9
TCCJ	SDRAM[0:12] Cycle to Cycle Jitter	-	250	-	250	ps	6, 8, 9
TPeriod	PCI(_F, 1:5) period	30.0	-	30.0	-	ns	5, 6, 8
THIGH	PCI(_F, 1:5) high time	12.0	-	12.0	-	ns	6,10
TLOW	PCI(_F, 1:5) low time	12.0	-	12.0	-	ns	6, 11
Tr / Tf	PCI(_F, 1:5) rise and fall times	0.5	2.0	0.5	2.0	ns	6, 7
TSKEW2	(Any PCI clock) to (Any PCI clock)	-	500	-	500	ps	6, 8, 9
TCCJ	PCI(_F, 1:5) Cycle to Cycle Jitter	-	500	-	500	ps	6, 8, 9
TPeriod	AGP(0,1) period	15.0	16.0	15.0	16.0	ns	5, 6, 8
THIGH	AGP(0,1) high time	5.25	-	5.25	-	ns	6,10
TLOW	AGP(0,1) low time	5.05	-	5.05	-	ns	6, 11
Tr / Tf	AGP(0,1 rise and fall times	0.5	2.0	0.5	2.0	ns	6, 7
TSKEW3	(Any AGP clock) to (Any AGP clock)	-	175	-	175	ps	6, 8, 9
TCCJ	AGP(0,1) Cycle to Cycle Jitter	-	500	-	500	ps	6, 8, 9
TPeriod	48MHz period (conforms to +167ppm max)	20.8299	20.8333	20.8299	20.8333	ns	5, 6, 8
Tr / Tf	48MHz rise and fall times	1.0	4.0	1.0	4.0	ns	6, 7
TCCJ	48MHz Cycle to Cycle Jitter	-	500	-	500	ps	6, 8, 9
TPeriod	24MHz period	41.6598	41.6666	41.6598	41.6666	ns	5, 6, 8
Tr / Tf	24MHz rise and fall times	1.0	4.0	1.0	4.0	ns	6, 7
TCCJ	24 MHz Cycle to Cycle Jitter	-	500	-	500	ps	6, 8, 9

AC Parameters (Cont.)

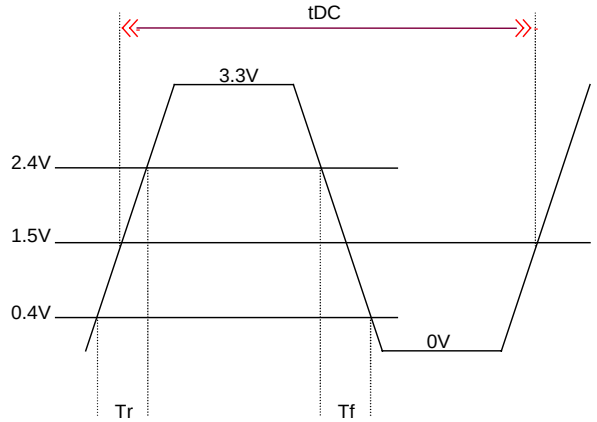
Symbol	Parameter	133 MHz Host		100 MHz Host		Units	Notes
TPeriod	REF(0,1) period	69.8413	71.0	69.8413	71.0	ns	5, 6, 8
Tr / Tf	REF(0,1) rise and fall times (2x)	1.0	2.0	1.0	2.0	ns	6, 7
Tr / Tf	REF(0,1) rise and fall times (1x)	1.0	4.0	1.0	4.0	ns	6, 7
TCCJ	REF(0,1) Cycle to Cycle Jitter	-	1000	-	1000	ps	6, 8
tpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	ns	13
tpLZ, tpHZ	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	ns	13
tstable	All clock Stabilization from power-up		3		3	ms	12
TSKEW4	Any CPU to Any SDRAM (see fig. 1)	0	250	0	250	ps	5, 6, 8

Note 5: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 6: All outputs loaded as per Table 7.
Note 7: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals. (See Figures 7)
Note 8: Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals. (See Figures 7)
Note 9: This measurement is applicable with Spread ON or Spread OFF.
Note 10: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals. (See Figures 7)
Note 11: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 12: The time specified is measured from when all VDD's reach their respective supply rail (3.3V) till the frequency output is stable and operating within the specifications
Note 13: Measured from when both SEL1 and SEL0 are low

Test and Measurement Condition



3.3V signals



2.5V signals

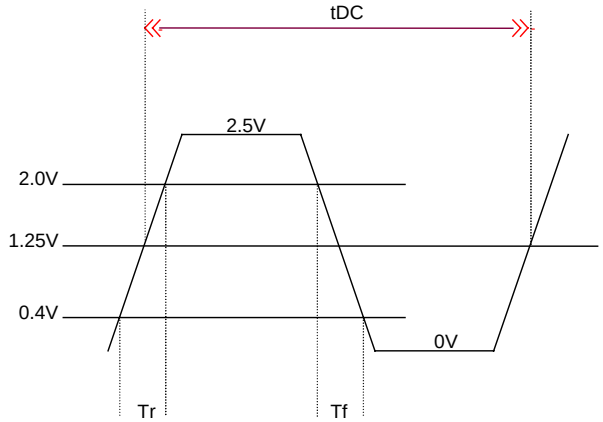


Figure 7

Output Buffer Characteristics,

CPU

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-15	-31	-51	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	-26	-58	-101	mA	Vout = 1.2V
Pull-Down Current	IOL_1	12	24	40	mA	Vout = 0.4V
Pull-Down Current	IOL_2	27	56	93	mA	Vout = 1.2V
Dynamic Output Impedance	Z0	13.5		45	Ω	

PCI, AGP

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-20	-25	-33	mA	Vout =VDD – 0.5V
Pull-Up Current	IOH_2	-30	-54	-184	mA	Vout = 1. 5V
Pull-Down Current	IOL_1	9.4	18	38	mA	Vout = 0.4V
Pull-Down Current	IOL_2	28	55	148	mA	Vout = 1.5V
Dynamic Output Impedance	Z0	12		55	Ω	

24MHz, 48MHz, and REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-12	-16	-28	mA	Vout =VDD – 0.5V
Pull-Up Current	IOH_2	-27	-43	-92	mA	Vout = 1. 5V
Pull-Down Current	IOL_1	9	13	27	mA	Vout = 0.4V
Pull-Down Current	IOL_2	26	39	79	mA	Vout = 1.5V
Dynamic Output Impedance	Z0	20		60	Ω	

SDRAM

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-28	-40	-60	mA	Vout =VDD – 0.5V
Pull-Up Current	IOH_2	-67	-107	-184	mA	Vout = 1. 4 V
Pull-Down Current	IOL_1	23	34	53	mA	Vout = 0.4V
Pull-Down Current	IOL_1	64	98	159	mA	Vout = 1.5V
Dynamic Output Impedance	Z0	10		24	Ω	
VDD=VDDS=VDDP=VDD48=3.3V ±5%, VDDC= 2.5V ±5% TA=0 to 70°C						

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
	T_A	-	-	5	PPM	Aging (first year @ 25C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	16	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

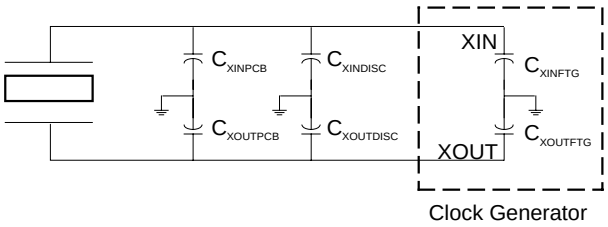
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit traces (C_{PCB}), and any onboard discrete load capacitors (C_{DISC}).

The following formula and schematic may be used to understand and calculate either the loading specification of a crystal for a design or the additional discrete load capacitance that must be used to provide the correct load to a known load rated crystal.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground



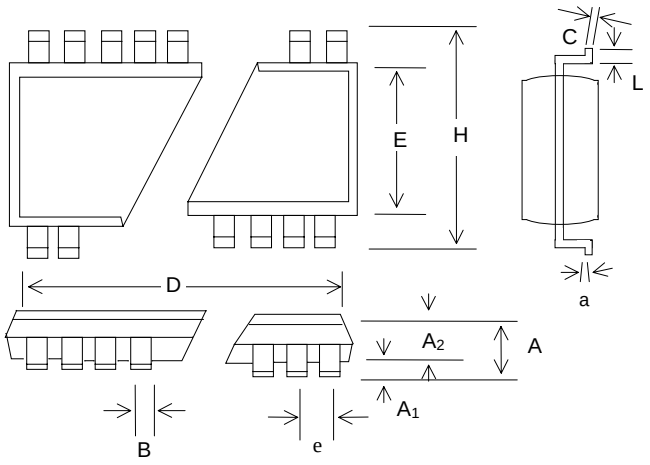
Suggested Oscillator Crystal Parameters

As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 2pF (typical value) would calculate as:

$$C_L = \frac{(2pF + 30pF + 0pF) \times (2pF + 30pF + 0pF)}{(2pF + 30pF + 0pF) + (2pF + 30pF + 0pF)} = \frac{32 \times 32}{32 + 32} = 16\ pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal, with C_L = 16pF.

Package Drawing and Dimensions



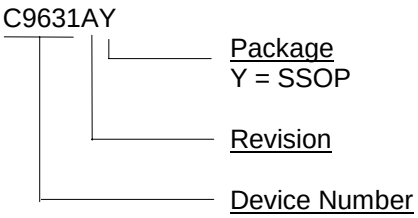
48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
B9631AY	48 Pin SSOP	Commercial, 0° C to +70°C

Marking: Example: Cypress
C9631AY
Date Code, Lot #



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Document Title: C9631 Low EMI 166 MHz Clock Generator for SiS630S/Pentium® III/Celeron® Chipsets
Document Number: 38-07036

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	106964	06/11/01	IKA	Convert from IMI to Cypress