C9777

Low EMI Clock Generator for 440BX, ALi1631 & Via Pro133+ / Pentium®III Systems

Product Features

- Supports Pentium® II and Pentium® III CPU's.
- Designed to meet Intel 440BX/ZX chipset specification
- Supports Via Pro 133+ and ALi1631 chipsets
- 4 CPU clocks with isolated power supply
- 8 PCI clocks
- 2 48 MHz for USB clock
- 3 Reference clocks
- 2 IOAPIC clocks
- < 175 pS Max. Skew among CPU clocks.
- < 500 pS Max. Skew among PCI clocks.
- Smooth frequency switching for jumperless application
- 48-pin SSOP package
- Spread Spectrum for EMI reduction

Frequency Table

S2	S1	S0	CPU	PCI
0	0	0	133.63	33.4
0	0	1	143.18	35.79
0	1	0	153.92	38.48
0	1	1	66.82	33.41
1	0	0	124.09	41.36
1	0	1	133.63	44.54
1	1	0	112.16	37.39
1	1	1	100.23	33.41

Table 1

Block Diagram

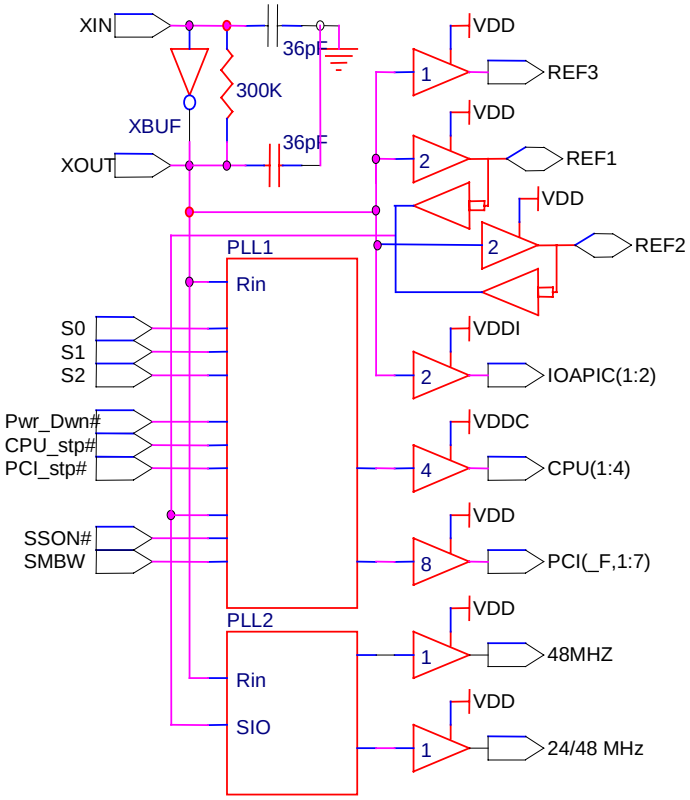
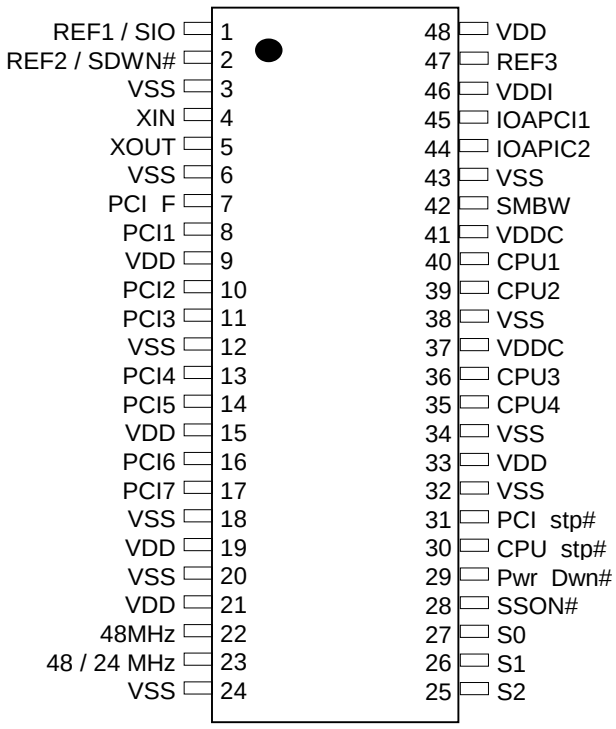


Fig.1

Pin Configuration



Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
1	**SI0**		I		This is a bi-directional pin (see app. note, p.4). At power up, it is an input select pin, SI0 for Selecting the frequency at pin23. When the power reaches the rail, the data is latched into the control registers, and this pin becomes
	REF1	VDD	O		A buffer output of the reference signal at Xin (typically a crystal).
2	**SDWN#**		I	PU	This is a bi-directional pin (see app. note, p.4). At power up, it is an input select pin, SDWN# for Selecting the center or down spread spectrum. When the power reaches the rail, the data is latched into the control registers, and this pin becomes
	REF2	VDD	O		A buffer output of the reference signal at Xin (typically a crystal).
4	**Xin**	VDD	I	OSC1	Reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC1	Reference oscillator output pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin remains unconnected.
7,8,10,11, 13,14,16,17	**PCI(_F,1:7)**	VDD	O		PCI clock outputs. They are Synchronous to the CPU clocks. See table 1 on page 1 for frequency and PCI to CPU ratio.
22	**48M**	VDD	O		a 48MHz USB clock output
23	**24M / 48M**	VDD	O		This output clock frequency is selected by Strapping SIO on pin 1 as follows: If SIO = 1, then this pin is a 48MHz USB clock If SIO = 0, then this pin is a 24 MHz SIO clock.
25,26,27	**S2,S1,S0**		I	PU	Input Select Lines for frequency selection. They have internal Pull-ups. See table1, p.1.
28	**SSON#**	VDD	I	PU	Input Line for enabling Spread Spectrum function When asserted Low.
29,30,31	**PWR_dwn#** **CPU_stp#** **PCI_stp#**	VDD	I	PU	These pins are for power management, and are typically controlled by the chipset South bridge. They have internal Pull-ups, and are active LOW. (see page 3) When CPU_stp# = 0, then CPU (1:4) are stopped in a low state synchronously. When PCI_stp# = 0, then PCI (1:7) are stopped in a low state synchronously. When PWR_dwn# = 0, then all clocks are stopped as well as internal circuitry.
35,36,39,40	**CPU(1:4)**	VDDC	O		Host (CPU) Clock outputs. See Table 1,p.1 for frequency selection.
44,45	**IOAPIC(1:2)**	VDDI	O		Buffered output clock of reference oscillator at Xin. (typically a crystal at 14.31818MHz)
47	**REF3**	VDD	O		REF buffer output of the reference clock at Xin. (typically a crystal at 14.31818MHz)

Pin Description (Cont.)

PIN No.	Pin Name	PWR	I/O	TYPE	Description
3,6,12,18, 20,24,32,3 8,43	**VSS**	-	P		Common Ground pins.
9,15,19,21 , 33,48	**VDD**	-	P		3.3V power supply pins.
37,41	**VDDC**	-	P		2.5V power supply pin for CPU (1:4) clocks.
46	**VDDI**	-	P		2.5V power supply pin for IOAPIC (1:2) clocks.
42	**SMBW**	VDD	I	PU	Spread mode bandwidth control. Selects width of SSCG modulation. See table 5 on page 5.

Table 2

A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductances of the traces.

PU: Pull Up – Typically 250K Ω. Value ranges between 200KΩ – 500 KΩ.

Power Management Functions

Power management function is controlled at pins 29, 30, and 31 inputs PD# (PWR_DWN#), CS# (CPU_STOP#), and PS# (PCI_STOP#) respectively. These inputs have internal pull ups, and are active LOW. Therefore, if these pins are floating, they will default to a high state and do not effect the device. Typically these inputs are controlled by the South Bridge chipset.

The clocks may be disabled according to the following tables 3 and 4 in order to reduce power consumption. All clocks are stopped in the low state, see fig.2. All clocks maintain a valid high period on transitions from running to stopped. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge of their own clock. PCI_F is the clock that times the power management function in the South Bridge, therefore it does not stop until PD# = 0.

CS#	PS#	PD#	CPU(1:4)	PCI(1:7)	OTHER CLKs	XTAL & VCOs
x	x	0	LOW	LOW	LOW	OFF
0	0	1	LOW	LOW	RUNNING	RUNNING
0	0	1	LOW	LOW	RUNNING	RUNNING
0	1	1	LOW	RUNNING	RUNNING	RUNNING
0	1	1	LOW	RUNNING	RUNNING	RUNNING
1	0	1	RUNNING	LOW	RUNNING	RUNNING
1	0	1	RUNNING	LOW	RUNNING	RUNNING
1	1	1	RUNNING	RUNNING	RUNNING	RUNNING
1	1	1	RUNNING	RUNNING	RUNNING	RUNNING

Table 3

NOTE1: All clocks can be individually enabled / stopped via the SMBUS interface. In this case all clocks are stopped asynchronously in the low state.

Power Management Functions

Power Management Timing Table

Signal	Signal State	Latency
CS#	1 (disabled)	1 rising edge of CPU_F
	0 (enabled)	1 rising edge of CPU_F
PS#	1 (disabled)	1 rising edge of PCI_F
	0 (enabled)	1 rising edge of PCI_F
PD#	1 (disabled)	2 mS
	0 (enabled)	1 rising edge of PCI_F

Table 4

Power Management Timing

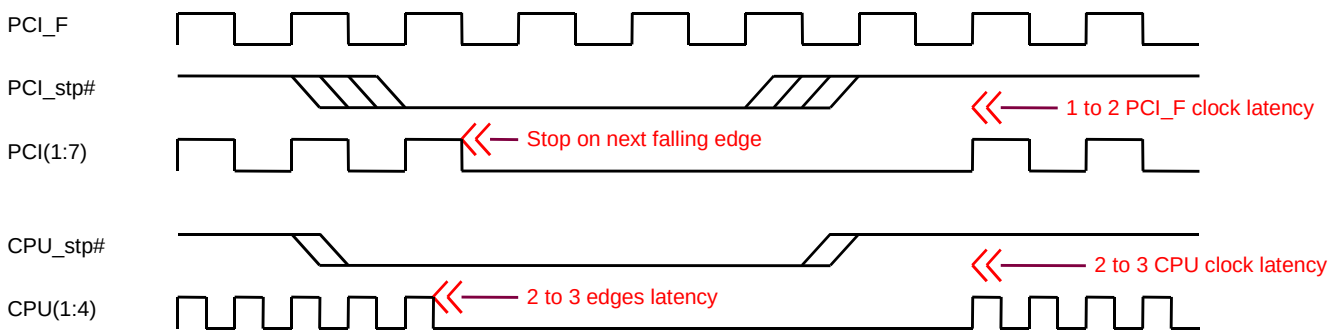


Fig. 2

Power on Bi-Directional Pins

Power Up Condition:

Pins 1, and 2 are Power up bi-directional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode (see Fig 3, below), therefore; they are considered input select pins internal to the IC. After a settling time, the Selection data is latch into internal control registers and these pins become toggling clock outputs.

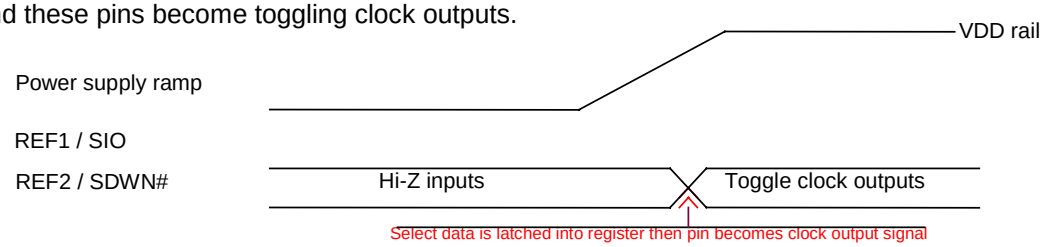


Fig.3

Strapping resistor options:

The power up bidirectional pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 5mS settling time), then **it is recommended** to use an external Pull-up (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see Fig.4A and Fig. 4B.

Fig4A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.

If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig.4A. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig4B represent a single resistor 10KΩ connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

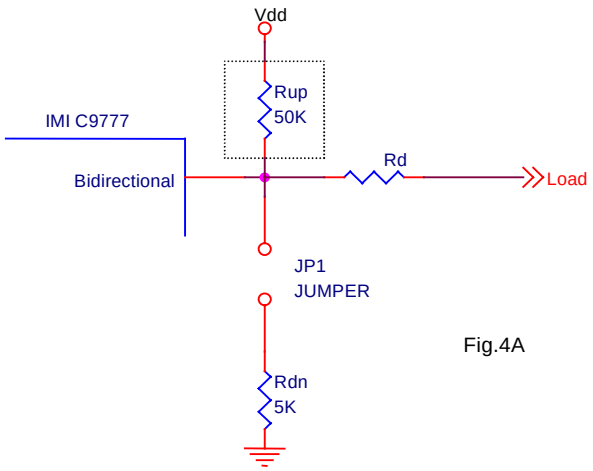


Fig.4A

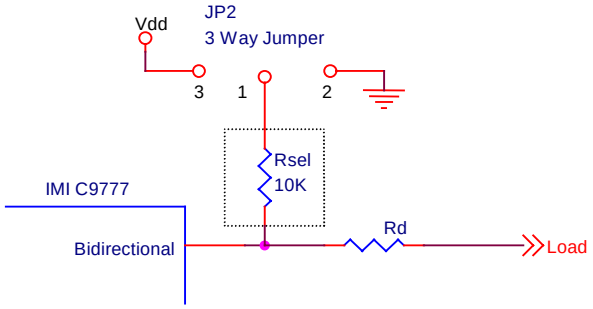


Fig.4B

Spectrum Spread Clocking

Center Spread *Down Spread*

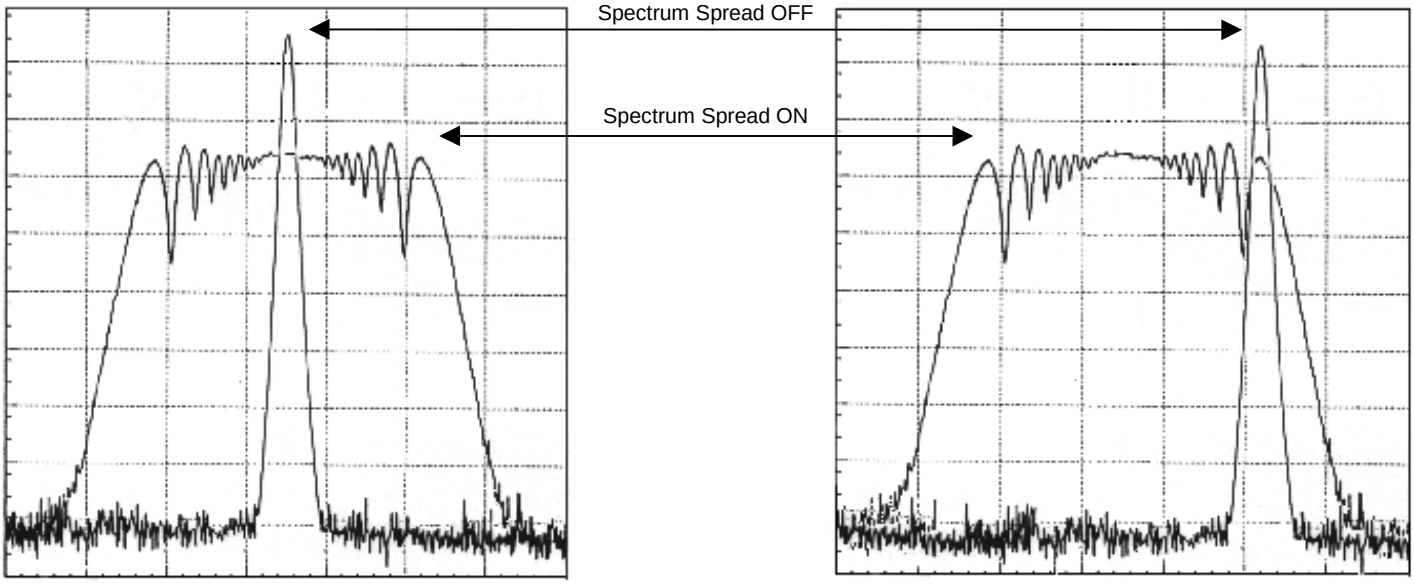


Fig.5a Fig.5B

Description

Spread Spectrum is a modulation technique for distributing clock period over a certain bandwidth (called Spread Bandwidth). This technique allows the distribution of the energy (EMI) over a range of frequencies therefore reducing the radiation generated from clocks. As the spread is a percentage of the center (non-spread) frequency, it is effective at the fundamental and all its harmonics.

In this device Spread Spectrum is enabled through pin 28 (SSON#). As the name suggests, spread spectrum is enabled when SSON# is low. This pin has an internal pull up, therefore, defaults to a high (Spread Spectrum disabled) unless externally forced to a low state.

SSON#	SMBW	SDWN#	Spread %	Direction
1	x	x	0	Spread OFF
0	0	0	+/-0.125	Center
0	0	1	+/-0.35	Center**, See note 1 below**
0	1	0	-0.5	Down
0	1	1	+/- 0.25	Center, default, **See note 2 below**

Table 5

Note1: This spread selection is NOT applicable when S (2:0) = 010. The device will be in TEST MODE.
Note 2: When frequency selection is 000, 011 and 101, the spread is –0.5%, otherwise it is +/- 0.25% as listed it Table 5 above.

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: 0ºC to +85ºC
Maximum ESD protection 2000V
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	0.8	Vdc	Applicable to Pins 25,26,27,28,29,30,31
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL	-66		-5	µA	Pull up
Input High Current (@VIL = VDD)	IIH			5	µA	Pull up
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	170	mA	CPU = 100.23 MHz, Note 1
Dynamic Supply Current	Idd2.5V	-	-	100	mA	CPU = 100.23 MHz, Note 2
Static Supply Current	Isdd	-	-	600	µA	-
VDD = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V for 3.3V signals Measured at 1.25V for 2.5 Volt signals
CPU – PCI Offset	tcp	1.5	-	4.0	nS	See note 5
Skew (CPU-CPU)	tSKEW1	-	-	175	pS	See note 3
Skew (PCI-PCI)	tSKEW2	-	-	500	pS	See note 3
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	pS	See note 4
VDD = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC						

Note 1: Measures current consumption through all vdd pins supplied with 3.3V (VDD, VDDS). All outputs loaded as per table7 below.
Note 2: Measures current consumption through all vdd pins supplied with 2.5V (VDDC, VDDI). All outputs loaded as per table7 below.
Note 3: All outputs loaded as per table 7 below. Probes are placed on the pins and taken at 1.5V levels.
Note 4: This measurement is applicable with Spread Spectrum ON or OFF.
Note 5: CPU clock leads. Cpu measured at rising edge 1.25 V, PCI at 1.5V.

Output Name	Max Load (in pF)
CPU(1:4), IOAPIC(1:2), REF3	20
PCI(_F,1:7)	30
48 MHz, REF(1:2)	15

Table 7.

Output Buffer Characteristics

CPU (1:4)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-25.96	-	-	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	-32.16	-	-	mA	Vout = VDDC/2
Pull-Down Current	IOL_1	14	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL2	33.68	-	-	mA	Vout = VDDC/2
Rise/Fall Time, @ 0.4V-2.0V	Tr, Tf	0.4	-	1.6	nS	See table 7 page 8

PCI(1:7, _F)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-13.88	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-35.5	-	-	mA	Vout = VDD/2
Pull-Down Current	IOL_1	13	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	39.9	-	-	mA	Vout = VDD/2
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	2	nS	See table 7 page 8

48 MHz and REF(1:3)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-5.8	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-16.56	-	-	mA	Vout = VDD/2
Pull-Down Current	IOL_1	6.07	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	22.16	-	-	mA	Vout = VDD/2
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	4	nS	See table 7 page 8

IOAPIC(1:2)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-13.42	-	-	mA	Vout =VDDI - 0.5V
Pull-Up Current	IOH_2	-25.4	-	-	mA	Vout = VDDI/2
Pull-Down Current	IOL_1	11.1	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	25.3	-	-	mA	Vout = VDDI/2
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	1.6	nS	See table 7 page 8

VDD = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0ºC to +70ºC

Suggested Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant, Note 1
Load Capacitance	CL	-	18	-	pF	The crystals rated load. Note 1
Effective Series resistance (ESR)	R1	-	40	-	Ohms	Note 1
Power Dissipation	DL	-	-	0.10	mW	Note 1
Shunt Capacitance	CO	-	--	8	pF	Crystal's internal package capacitance (total)

Note1: For best performance and accurate Center frequencies of this device, It is recommended but not mandatory that the chosen crystal meets these specifications.

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Device pin capacitance: Cxtal = 34pF
In order to meet the specification for CL = 18pF following the formula:

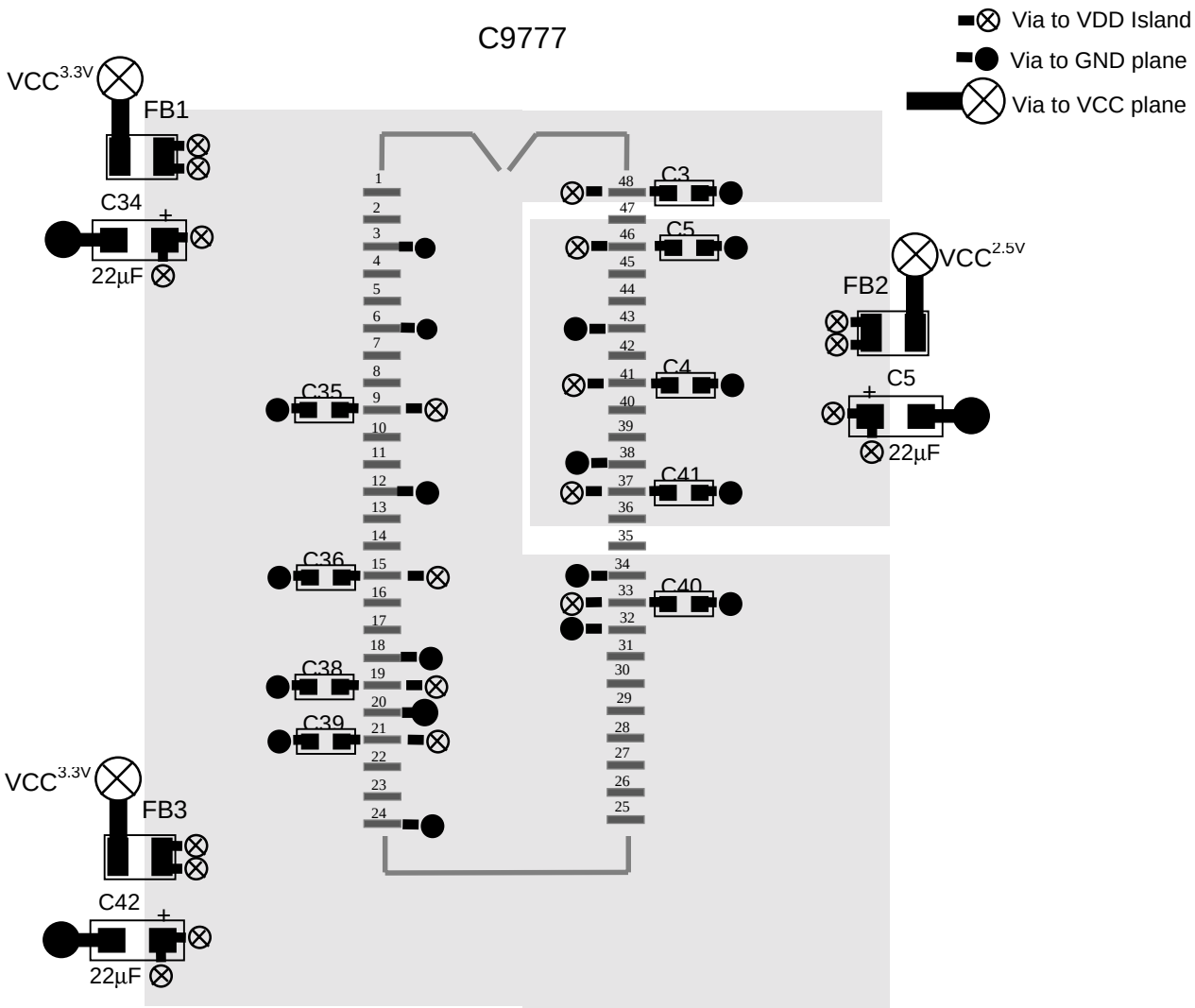
$$C_L = \frac{C_{XIN} x C_{XOUT}}{C_{XIN} + C_{XOUT}}$$

Then the board trace capacitance between Xin and the crystal should be no more than 2pF. (same is applicable to the trace between Xout and the crystal)

In this case the total capacitance from the crystal to Xin will be 36pF. Similarly the total capacitance between the crystal and Xout will be 36pF. Hence using the above formula:

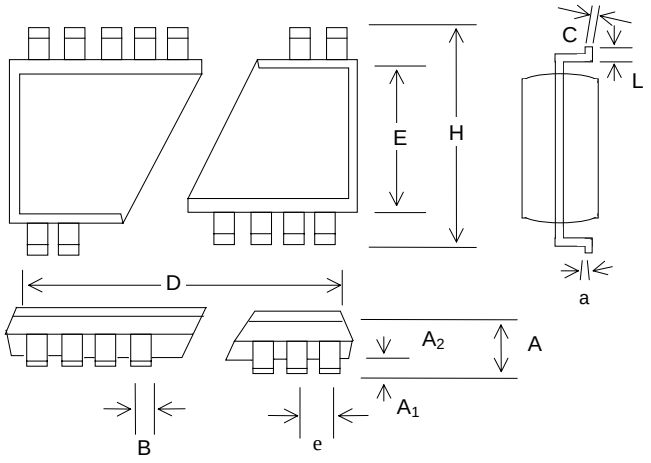
$$C_L = \frac{36\,pF x 36\,pF}{36\,pF + 36\,pF} = 18\,pF$$

PCB Layout Suggestion



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C3, C4, C5, C35, C36, C37, C38, C39, C40 and C41 (all are 0.1µf) should always be used and placed as close as possible to their VDD pins.

Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
B	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0º	5º	8º	0º	5º	8º

Ordering Information

Part Number	Package Type	Production Flow
C9777BYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Marking: Example: Cypress
C9777
Date Code, Lot #

C9777BYB

Flow
B = Commercial, 0ºC to + 70ºC

Package
Y = SSOP

Revision

Device Number

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Document Title: C9777 Low EMI Clock Generator for 440BX, Ali1631 & Via Pro133+ / Pentium®III Systems
Document Number: 38-07048

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107056	06/12/01	IKA	Convert from IMI to Cypress