# C9926

## Low EMI Clock Generator for Intel® 133MHz/ 2DIMM Chipset Systems

### Product Features

- Designed for Intel's 133MHz/SDRAM chipset
- 2 copies of CPU Clock (CPU[0:1])
- 9 copies of SDRAM Clock (SDRAM[0:8])
- 5 copies of PCI Clocks
- 3 copies of 3V66 Clock
- 1 IOAPIC Clock, synchronous to PCI Clock
- 1 REF Clock
- 1 USB Clock (Non SSC)
- 1 DOT Clock (Non SSC)
- Cypress Spread Spectrum for best EMI reduction
- Dial-a-Frequency™ Feature
- Dial-a-dB™ Feature
- 48 Pin SSOP

### Block Diagram

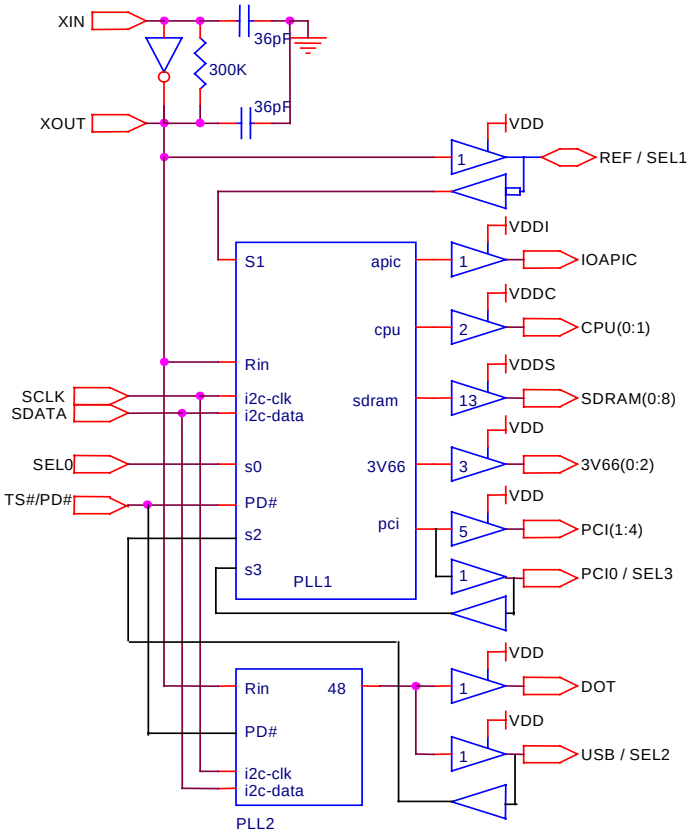



Fig.1

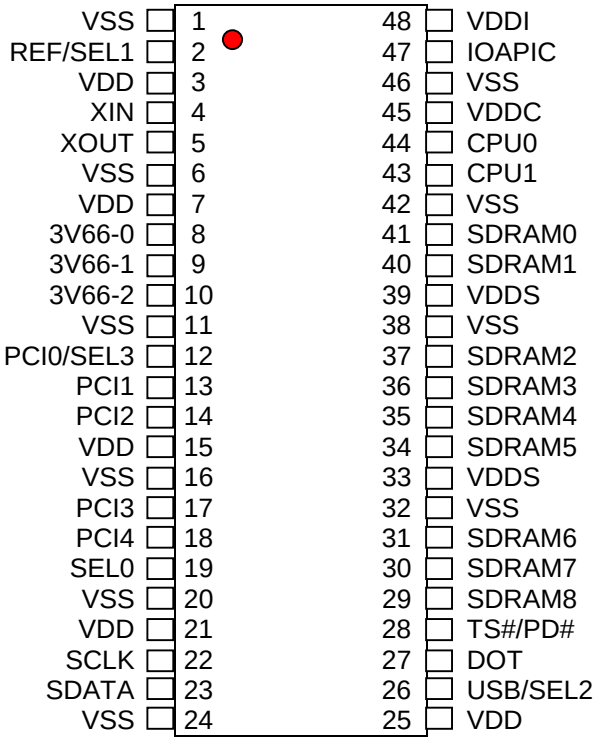
### Frequency Table (MHz)

| SEL (3:0)** | CPU | SDRAM | 3V66 | PCI /IOAPIC | REF | DOT | USB |
|---|---|---|---|---|---|---|---|
| 0000 | 66.67 | 100.00* | 66.67 | 33.33 | 14.318 | 48 | 48 |
| 0001 | 100.00 | 100.00* | 66.67 | 33.33 | 14.318 | 48 | 48 |
| 0010 | 133.33 | 133.33 | 66.67 | 33.33 | 14.318 | 48 | 48 |
| 0011 | 133.33 | 100.00* | 66.67 | 33.33 | 14.318 | 48 | 48 |
| 0100 | 83.35 | 125.02 | 83.35 | 41.67 | 14.318 | 48 | 48 |
| 0101 | 106.91 | 106.91 | 71.27 | 35.64 | 14.318 | 48 | 48 |
| 0110 | 150.00 | 150.00 | 75.00 | 37.50 | 14.318 | 48 | 48 |
| 0111 | 120.96 | 120.96 | 80.64 | 40.32 | 14.318 | 48 | 48 |
| 1000 | 89.90 | 134.86 | 89.90 | 44.95 | 14.318 | 48 | 48 |
| 1001 | 125.02 | 125.02 | 83.35 | 41.67 | 14.318 | 48 | 48 |
| 1010 | 200.00 | 200.00 | 100.00 | 50.00 | 14.318 | 48 | 48 |
| 1011 | 116.87 | 116.87 | 77.91 | 38.96 | 14.318 | 48 | 48 |
| 1100 | 100.00 | 133.33 | 66.67 | 33.33 | 14.318 | 48 | 48 |
| 1101 | 112.00 | 112.00 | 74.67 | 37.33 | 14.318 | 48 | 48 |
| 1110 | 166.53 | 166.53 | 83.27 | 41.63 | 14.318 | 48 | 48 |
| 1111 | 140.00 | 105.00 | 70.00 | 35.00 | 14.318 | 48 | 48 |

Table1

*Contingent upon the SMBus Byte3, Bit0 configuration.
**SEL also controls TS# functionality if TS# is 0 at power up.

### Pin Configuration

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## Pin Description

| PIN No. | Pin Name | PWR | I/O | TYPE | Description |
|---|---|---|---|---|---|
| 47 | **IOAPIC** | VDDI | O | | 2.5V IOAPIC clock output. See fig.3 p.4 for timing relationship. |
| 2 | **SEL1/REF** | VDD | I/O | PD | This is a bi-directional pin (see app. note, p.6). At power up, it is an input pin SEL1 for frequency selection (see table 1 p.1). When the power reaches the rail, the state of SEL1 is latched, and this pin becomes REF, a buffer output of the signal applied at Xin, typically 14.318MHz. |
| 4 | **XIN** | VDD | I | OSC1 | On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318MHz) or externally generated reference signal |
| 5 | **XOUT** | VDD | O | | On-chip reference oscillator pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at XIN, this pin remains unconnected. |
| 12 | **SEL3/PCI0** | VDD | I/O | PD | This is a bi-directional pin (see app. note, p.6). At power up, it is an input pin SEL3 for frequency selection (see table 1 p.1). When the power reaches the rail, the state of SEL3 is latched, and this pin becomes PCI clock output. |
| 13,14,17,18 | **PCI(1:4)** | VDD | O | | 3.3V PCI clock outputs. They are Synchronous to CPU clocks. See fig.3, p. 4. |
| 8, 9, 10 | **3V66(0:2)** | VDD | O | | 3.3V Hub/AGP clock outputs. See fig.3 p.4. |
| 26 | **SEL2/USB** | VDD | I/O | PD | This is a bi-directional pin (see app. note, p.6). At power up, it is an input pin SEL2 for frequency selection (see table 1 p.1). When the power reaches the rail, the state of SEL2 is latched, and this pin becomes a fixed 48MHz clock output for USB. |
| 27 | **DOT** | VDD | O | | 3.3V Fixed 48MHz DOT clock output |
| 19 | **SEL0** | VDD | I | PU1 | 3.3V LVTTL input for frequency selection, see table 1 p.1. SEL0 also controls TS# functionality if TS# is 0 at power up. See fig.6 p.7. |
| 23 | **SDATA** | VDD | I | | Serial data input pin. Conforms to the SMBus specification of a Slave Receive/Transmit device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting data. See SMBus function description, p. 8. |
| 22 | **SCLK** | VDD | I | | Serial clock input pin. Conforms to the SMBus specification. |
| 28 | **TS#/PD#** | VDD | I | PU2 | This is a dual function input pin. During power up, if TS# is low, it serves as a Tri-state control (TS#). Once high, this pin becomes a Power Down control (PD#). See fig.6 p.7. |
| 29,30,31,34, 35,36,37,40, 41 | **SDRAM (0:8)** | VDDS | O | | 3.3V SDRAM DIMM clock outputs. See table1, p.1 for frequency selection. See fig.3, p.3 for timing relationship and SMBus Byte3, Bit0. |
| 43,44 | **CPU(0:1)** | VDDC | O | | 2.5V Host clock outputs. See table1, p.1 for frequency selection. |
| 3,7,15,21,25 | **VDD** | - | | | 3.3V Common Power Supply |
| 45, 48 | **VDDC,VDDI** | - | | | 2.5V Power Supply for CPU(0:1) and IOAPIC respectively. |
| 1,6,11,16,20,24 , 32, 38, 42, 46 | **VSS** | - | | - | Common Ground pins. |
| 39,33 | **VDDS** | - | | - | 3.3V power support for SDRAM(0:8) clock output drivers. |

PU1 = Internal Pull-Up. Typical 250KΩ (range 200KΩ to 500KΩ). PD = Internal Pull-Down. Typical 50KΩ (range 25KΩ to 75KΩ)
PU2 = Internal Pull-Up Typical 50kΩ (range 25kΩ to 75kΩ)

## Test Mode Function

### Test Mode Functionality

| TS# | SEL0 | CPU | SDRAM | 3V66 | PCI | DOT/USB | REF | IOAPIC |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | TCLK/2 | TCLK/2 | TCLK/3 | TCLK/6 | TCLK/2 | TCLK | TCLK/6 |
| 0 | 0 | Tri-state | Tri-state | Tri-state | Tri-state | Tri-state | Tri-state | Tri-state |

Table 2

**Note:** TCLK is a test clock over driven on the XIN input during test mode. Test Mode/Tri-state mode set during power up and if TS# is low. Also can be set through SMBus when Byte3 Bit6 = 1, Byte0 Bit0 = 1, and Bit4 = 0 or 1.

## Power Management Functions

Power Management on this device is controlled by a single pin, PD# (pin28). When PD# is high (default) the device is in normal running mode and all signals are active.

When PD# is asserted (forced) low, the device is in shutdown (or in power down) mode and all power supplies may be removed. When in power down, all outputs are synchronously stopped in a low state (see Fig.2 below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown, the I²C function is also disabled.

## Power Management Timing

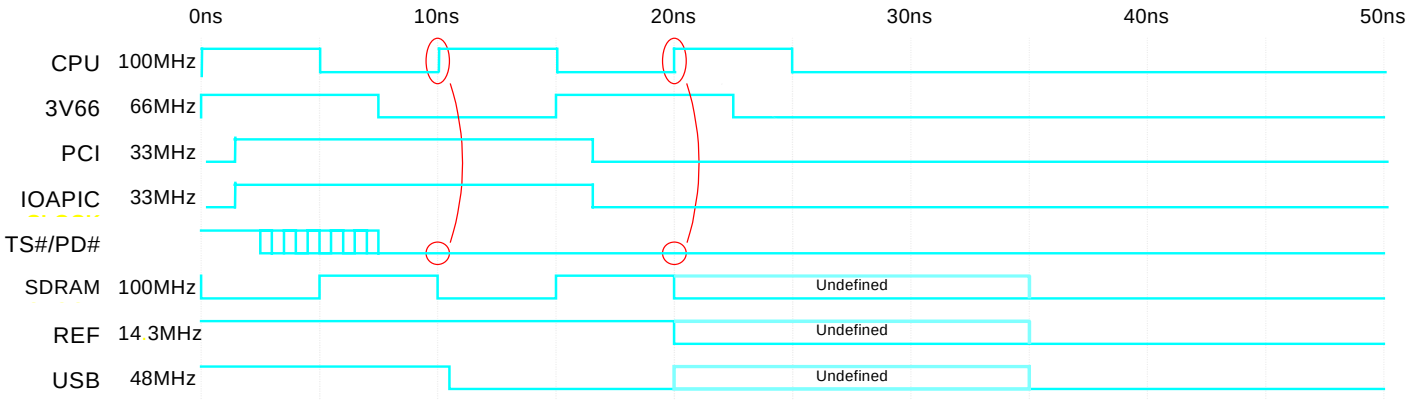



Fig.2

## Power Management Current

| PD#, SEL(3:0) | Maximum 2.5 Volt Current Consumption (VDDC = VDDI =2.625V) | Maximum 3.3 Volt Current Consumption (VDD = VDDA = VDDS = 3.465V) |
|---|---|---|
| 0XXXX (Power down) | 10mA | 10mA |
| 10000 (66MHz) | 70mA | 280mA |
| 10001 (100MHz) | 100mA | 280mA |
| 1001X (133MHz) | 133mA | 365mA |

Table 3

When exiting the power down mode, the designer must supply power to the VDD pins first, a minimum of 200ms before releasing the PD# pin high.

## IOAPIC Clock Synchronization and Phase Alignment

This device incorporates IOAPIC clock synchronization. With this feature, the IOAPIC clocks are derived from the CPU clock. The IOAPIC clock lags the CPU clock by the specified 1.5ns to 3.5ns. Figure 3 shows the relationship between the CPU and IOAPIC clocks.

## Clock Phase Relationships

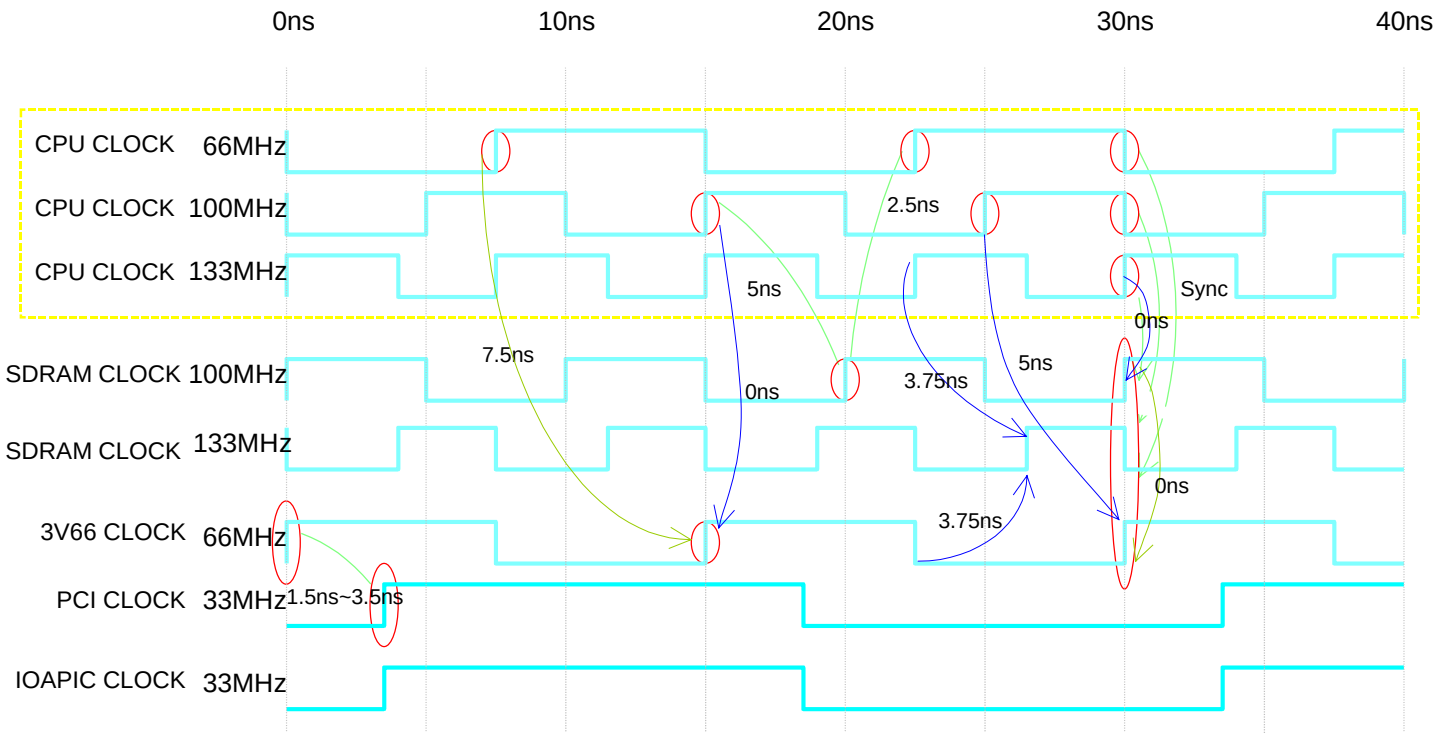



Fig.3

## Group Timing Relationships and Tolerances

| | CPU = 66.6MHz, SDRAM = 100MHz | | |
|---|---|---|---|
| | **Offset (ns)** | **Tolerance (ps)** | **Conditions** |
| CPU to SDRAM | 2.5 | 500 | |
| CPU to 3V66 | 7.5 | 500 | 180 degrees phase shift |
| SDRAM to 3V66 | 0 | 500 | When rising edges line-up |
| 3V66 to PCI | 1.5-3.5 | 500 | 3V66 leads |
| PCI to IOAPIC | 0 | 1000 | |
| | **CPU = 100MHz, SDRAM = 100MHz** | | |
| | **Offset (ns)** | **Tolerance (ps)** | **Conditions** |
| CPU to SDRAM | 5 | 500 | 180 degrees phase shift |
| CPU to 3V66 | 5 | 500 | |
| SDRAM to 3V66 | 0 | 500 | When rising edges line-up |
| 3V66 to PCI | 1.5-3.5 | 500 | 3V66 leads |
| PCI to IOAPIC | 0 | 1000 | |
| | **CPU = 133.3MHz, SDRAM = 100MHz** | | |
| | **Offset (ns)** | **Tolerance (ps)** | **Conditions** |
| CPU to SDRAM | 0 | 500 | When rising edges line-up |
| CPU to 3V66 | 0 | 500 | |
| SDRAM to 3V66 | 0 | 500 | When rising edges line-up |
| 3V66 to PCI | 1.5-3.5 | 500 | 3V66 leads |
| PCI to IOAPIC | 0 | 1000 | |
| | **CPU = 133.3MHz, SDRAM = 133.3MHz** | | |
| | **Offset (ns)** | **Tolerance (ps)** | **Conditions** |
| CPU to SDRAM | 3.75 | 500 | 180 degrees phase shift |
| CPU to 3V66 | 0 | 500 | |
| SDRAM to 3V66 | 3.75 | 500 | |
| 3V66 to PCI | 1.5-3.5 | 500 | 3V66 leads |
| PCI to IOAPIC | 0 | 1000 | |

## Power on Bi-Directional Pins

### Power Up Condition:

Pins 2, 12, 26 are Power up bi-directional pins and are used for selecting the host frequency in p.1, table 1. During power-up of the device, these pins are in input mode (see Fig 4, below), therefore; they are considered input select pins, SEL(1:3) internal to the IC. After a settling time, the selection data is latch into the internal control register and these pins become a clock output.

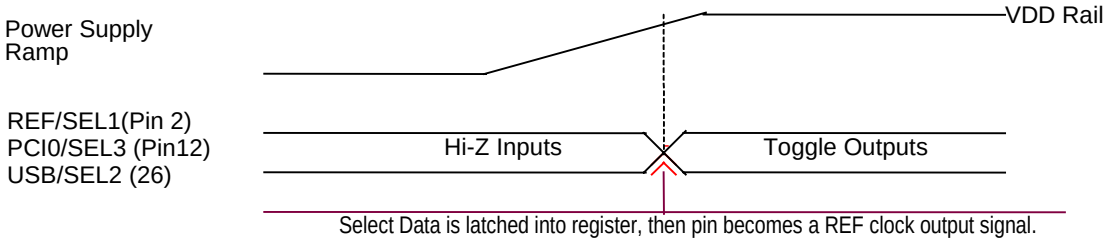



Fig.4

### Strapping Resistor Options:

The power up bi-directional pins have a large value pull-down (50KΩ+/–25KΩ), therefore, a selection "0" is the default. If the system uses a slow power supply (over 10mS settling time), then **it is recommended** to use an external Pull-down (Rdn) in order to insure a low selection. In this case, the designer may choose one of two configurations, see Fig.5A and B.

Fig. 5A represents an additional pull down resistor 5KΩ connected from the pin to the power line, which allows a faster down to a high level.
If a selection "1" is desired, then a jumper is placed on JP1 to a 1 KΩ resistor as shown in Fig.5A. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

Fig. 5B represent a single resistor 5KΩ connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

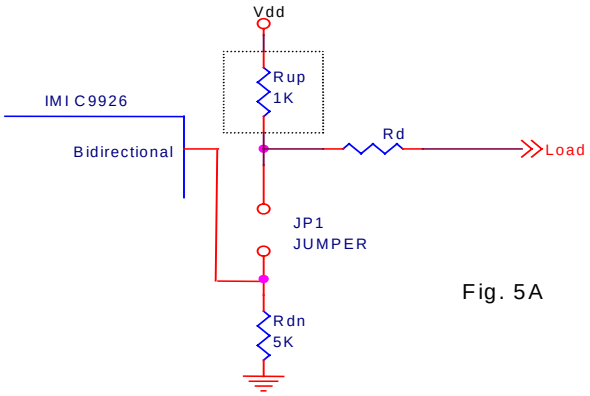



Fig. 5A

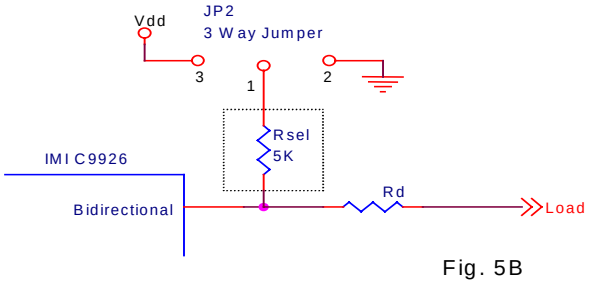



Fig. 5B

## Power on Bi-Functional Pins (Cont.)

Pin 28 (TS#/PD#) is a bi-functional pin, See Fig.6. If this pin is externally held low during power up, the device is forced into Tri-state/or test mode depending on the state of SEL0 (pg. 3).

In Tri-state mode, all outputs assume the high impedance (Hi-Z) state. In test, all outputs toggle as described in table 2, p. 3.

All outputs remain in their Hi-Z state (or test mode) until the external signal applied to TS#/PD# is released (set high). TS# should remain high for a minimum of 1.5mS after a stable 3.3V power supply. Then TS#/PD# changes from a Tri-state controller (TS#) to Power Down controller (PD#) and remains in that function unless otherwise programmed through the SMBus to return to the TS# function by setting Byte3, Bit1 to a "0". Once the TS# signal is released (high), TS#/PD# may be toggled repetitively to force the device in and out of power down mode.

The device is considered in power down when PD# is asserted low, consequently, all clocks are stopped synchronously and after the completion of a full period (glitch-free).

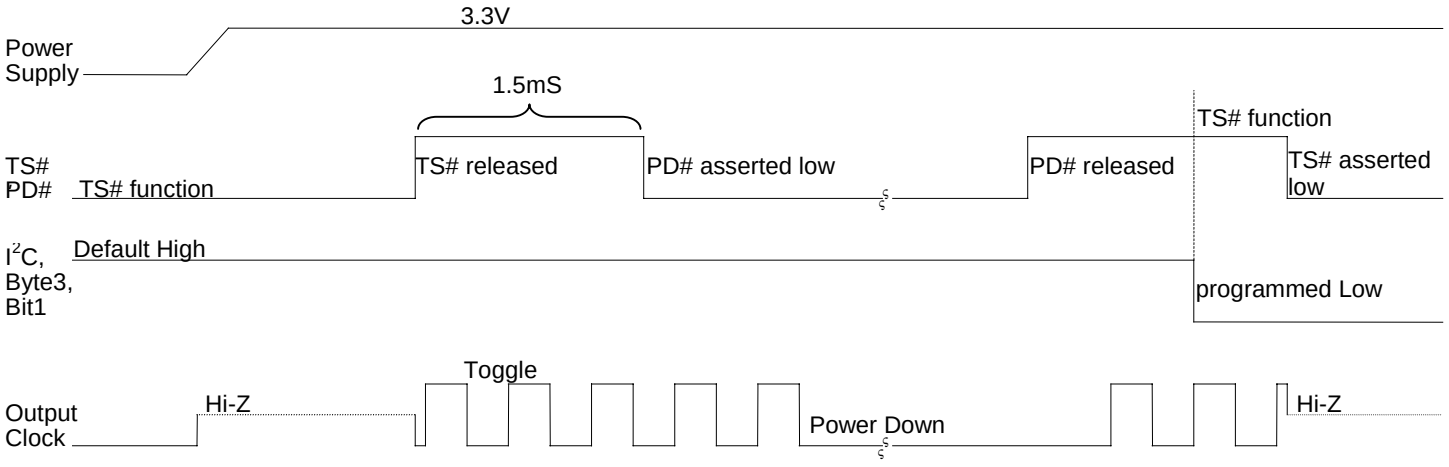



Fig.6

## 2-Wire SMBus Control Interface

The 2-wire control interface implements a read/write slave only interface according to SMBus specification. (See Fig. 7 below). The device can read back by using standard SMBus command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an 8-bit address. The LSB address Byte = 0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. Data is transferred MSB first at a max rate of 100kbits/S. This device will also respond to a **D3** address which sets it in a read mode. It will not respond to any other control interface conditions, and previously set control registers are retained.

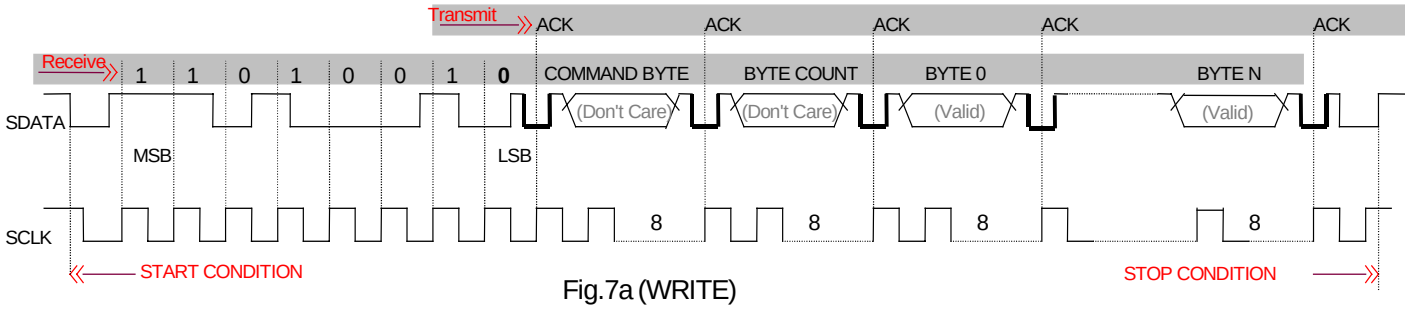



Fig.7a (WRITE)

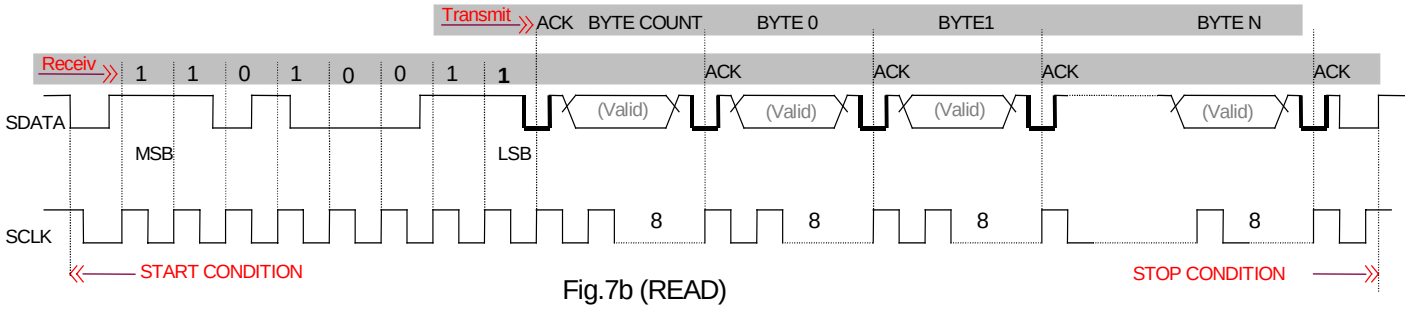



Fig.7b (READ)

Figure 7
SMBus Communications Waveforms

## Serial Control Registers

**NOTE:** The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the following sequence (Byte 0, Byte 1, and Byte2) will be valid and acknowledged.

**Byte 0: CPU Clock Register** (1=Enable, 0=Disable)

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 0 | - | SEL3 frequency selector |
| 6 | 0 | - | SEL2 frequency selector |
| 5 | 0 | - | SEL1 frequency selector |
| 4 | 0 | - | SEL0 frequency selector |
| 3 | 0 | - | 1 = Spread Spectrum Enabled<br>0 = Spread Spectrum Disabled |
| 2 | 1 | 27 | DOT |
| 1 | 1 | 26 | USB |
| 0 | 0 | - | High enables bit(7:4) selectors. |

**Byte 2: SDRAM Clock Register** (1=Enable, 0=Disable)

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 1 | 10 | 3V66-2 |
| 6 | 1 | - | RESERVED (drive to "0") |
| 5 | 1 | - | RESERVED (drive to "0") |
| 4 | 1 | 29 | SDRAM8 |
| 3 | 1 | 30 | SDRAM7 |
| 2 | 1 | 31 | SDRAM6 |
| 1 | 1 | 13 | PCI1 |
| 0 | 0 | - | RESERVED |

**Byte 4: PCI Clock Register** (1=Enable, 0=Disable)

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 0 | - | RESERVED |
| 6 | 0 | - | RESERVED |
| 5 | 0 | - | RESERVED |
| 4 | 1 | - | RESERVED (drive to "0") |
| 3 | 1 | - | RESERVED (drive to "0") |
| 2 | 1 | 18 | PCI4 |
| 1 | 1 | 17 | PCI3 |
| 0 | 1 | 14 | PCI2 |

**Byte 1: SDRAM Clock Register** (1=Enable, 0=Disable)

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 1 | - | RESERVED (drive to "0") |
| 6 | 1 | - | RESERVED (drive to "0") |
| 5 | 1 | - | SDRAM5 |
| 4 | 1 | - | SDRAM4 |
| 3 | 1 | - | SDRAM3 |
| 2 | 1 | - | SDRAM2 |
| 1 | 1 | - | SDRAM1 |
| 0 | 1 | - | SDRAM0 |

**Byte 3: Reserved Register**

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 0 | - | RESERVED |
| 6 | 0 | - | High puts the device in TEST mode. |
| 5 | 0 | - | RESERVED |
| 4 | 0 | - | RESERVED |
| 3 | 0 | - | RESERVED |
| 2 | 0 | - | RESERVED |
| 1 | 1 | 28 | 1 enables std. Functionality TS#/PD#<br>0 enables TS# only |
| 0 | 0 | - | 0 = SDRAM runs at 100MHz<br>1= SDRAM runs at 133.3MHz |

**Byte 5: SSCG Control Register**

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 0 | - | Spread Mode (0=down, 1=center) |
| 6 | 0 | - | Selects spread bandwidth. Ref. Table 4 |
| 5 | 0 | - | Selects spread bandwidth. Ref. Table 4 |
| 4 | 0 | - | RESERVED |
| 3 | 0 | - | RESERVED |
| 2 | 0 | - | RESERVED |
| 1 | 0 | - | RESERVED |
| 0 | 0 | - | RESERVED |

**Byte 6: Dial-a-Frequency™ Register**

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 0 | - | N9, MSB |
| 6 | 0 | - | N8 |
| 5 | 0 | - | N7 |
| 4 | 0 | - | N6 |
| 3 | 0 | - | N5 |
| 2 | 0 | - | N4 |
| 1 | 0 | - | N3 |
| 0 | 0 | - | N2 |

**Byte 7: Dial-a-Frequency™ Register**

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 0 | - | N1 |
| 6 | 0 | - | N0, LSB |
| 5 | 0 | - | Enable SMBus N values |
| 4 | 0 | - | Enable SMBus R values |
| 3 | 0 | - | Reserved |
| 2 | 0 | - | Reserved |
| 1 | 0 | - | Reserved |
| 0 | 0 | - | Reserved |

**Byte 8: Dial-a-Frequency™ Register**

| Bit | @Pup | Pin# | Description |
|---|---|---|---|
| 7 | 0 | - | R7, MSB |
| 6 | 0 | - | R6 |
| 5 | 0 | - | R5 |
| 4 | 0 | - | R4 |
| 3 | 0 | - | R3 |
| 2 | 0 | - | R2 |
| 1 | 0 | - | R1 |
| 0 | 0 | - | R0, LSB |

## Dial-a-Frequency™ Feature

SMBus Dial-a-frequency feature is available in this device via Bytes 6, 7 and 8.
These bytes allow the user to enter the N and R values that will enable them to program any CPU frequency desired following the formula:

$$Fcpu = \frac{P \times N}{R}$$

Where N and R values are programmed in binary into Bytes 6 & 7 for N and Byte 8 for R. See table below for min and max allowed values.

| R | Min N | Max N |
|---|---|---|
| 42 | 44 | 87 |
| 43 | 45 | 90 |
| 44 | 46 | 92 |
| 45 | 47 | 94 |
| 46 | 48 | 96 |
| 47 | 49 | 98 |
| 48 | 50 | 100 |
| 49 | 51 | 102 |
| 50 | 52 | 104 |
| 51 | 53 | 107 |

## Dial-a-Frequency™ Feature (Cont.)

P is a large value PLL constant that depends on the last frequency selection achieved through the hardware selectors (SEL3, SEL2, SEL1, SEL0) or through the software selectors (Byte0, Bits7, 6, 5, 4). P value may be determined from the following table:

| SEL(3:0) | P |
|---|---|
| 0000 | 32005333 |
| 0001, 1100 | 48008000 |
| 0010, 0011, 0100, 1000, 1111 | 64010666 |
| 0110, 0111, 0101, 1001, 1010, 1011, 1101, 1110 | 96016000 |

Therefore, if a 145MHz (use $145x10^6$) value is desired, then we should apply 145 into equation 1, and start by choosing R to be 47 (assume the last frequency selection has the value P = 96016000):

$$145X10^6 = \frac{96016000 \times N}{47} \quad => \quad N = 70.97775371$$

Since this N number must be entered in Binary, it can only be an integer, so it must be rounded up or down. Here we can rounded it up to 71, which will give us an exact CPU frequency of:

$$Fcpu = \frac{96016000 \times N}{47} = 145.045 \text{ MHz (accuracy +310 ppm)}$$

If the above frequency is not accurate enough, then you must choose another R value and start from the beginning. For example choose R = 49 and this will yield an N = 73.99808365, which is rounded to 74. If the 74 is applied in the formula 1, then Fcpu = 145.0038MHz(accuracy +26 ppm).

Other R values within the above limits may also be evaluated.

## Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from (Fig.8A) or around the center (Fig.8B) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting SMBus Byte0, Bit3 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have SMBus accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SMBus Byte 5, Bits 5, 6 & 7 following tables 4A, and 4B below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (eg.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

## Spread Spectrum Clock Generation (SSCG) (Cont.)

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Down Spread

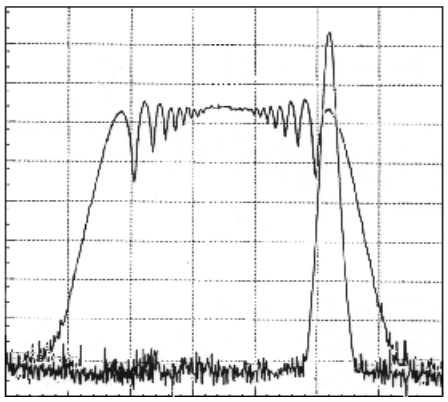


Fig.8A

Center Spread

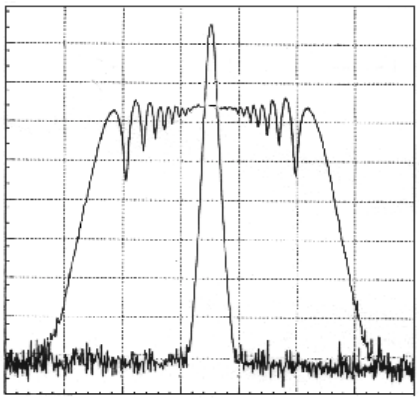


Fig.8B

### Spread Spectrum Selection Tables

| **I²C BYTE5** Bit[7:5] | Spread % |
|---|---|
| 000 | - 0.5 |
| 001 | - 0.7 |
| 010 | N/A |
| 011 | - 0.25 |

Table 4A

| **I²C BYTE5** Bit[7:5] | Spread % |
|---|---|
| 100 | ± 0.25 |
| 101 | ± 0.35 |
| 110 | ± 0.5 |
| 111 | +/- 0.125 |

Table 4B

## Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V

Maximum Input Voltage Relative to VDD: VDD + 0.3V

Storage Temperature: -65°C to + 150°C

Operating Temperature: 0°C to +85°C

Maximum ESD protection 2KV

Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD)

.

## DC Parameters

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL1 | - | - | 1.0 | V | Note 1 |
| Input High Voltage | VIH1 | 2.0 | - | - | V | |
| Input Low Voltage | VIL2 | - | - | 1.0 | V | Note 2 |
| Input High Voltage | VIH2 | 2.2 | - | - | V | |
| Input Low Current (@VIL = VSS) | IIL1 | -66 | | -5 | µA | For internal Pull up resistors, Notes 1,3 |
| Input High Current (@VIL =VDD) | IIH1 | -5 | | 5 | µA | |
| Input Low Current (@VIL = VSS) | IIL2 | -5 | | 5 | µA | For internal Pull Down resistor Note 4 |
| Input High Current (@VIL =VDD) | IIH2 | 5 | | 66 | µA | |
| Tri-State leakage Current | Ioz | - | - | 10 | µA | TS# = SEL0 = 0, Vo = VDD or VSS |
| Dynamic Supply Current | Idd3.3V | - | - | 360 | mA | SEL(3:0) = 0001 |
| Dynamic Supply Current | Idd2.5V | - | - | 100 | mA | SEL(3:0) = 0001 |
| Static Supply Current | Isdd | - | - | 10 | mA | PD# = 0. SEL(3:0) = X |
| Input pin capacitance | Cin | - | - | 5 | pF | |
| Output pin capacitance | Cout | - | - | 6 | pF | |
| Pin inductance | Lpin | - | - | 7 | nH | |
| Crystal pin capacitance | Cxtal | 32 | 34 | 38 | pF | Measured from Pin to Ground. Note 5 |
| Crystal DC Bias Voltage | $V_{BIAS}$ | 0.3Vdd | Vdd/2 | 0.7Vdd | V | |
| Crystal Startup time | Txs | - | - | 40 | µs | From Stable 3.3V power supply. |
| **VDD=VDDS = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0º to +70ºC** | | | | | | |

Note1: Applicable to input signals: SEL(0:3), TS#/PD#

Note2: Applicable to Sdata, and SCLK.

Note3: Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.

Note4: Although internal pull-down resistor has a typical value of 50K, this value may vary between 30K and 70K.

Note5: Although the device will reliably interface with crystals of a 17pF – 20pF $C_L$ range, it is optimized to interface with a typical $C_L$ = 18pF crystal specifications.

| Clock Name | Max Load (pF) |
|---|---|
| CPU(0:1), IOAPIC, REF, USB | 20 |
| PCI(0:4), SDRAM(0:8),3V66(0:2) | 30 |
| DOT | 15 |

Table 5.

## SMBus Test Circuitry

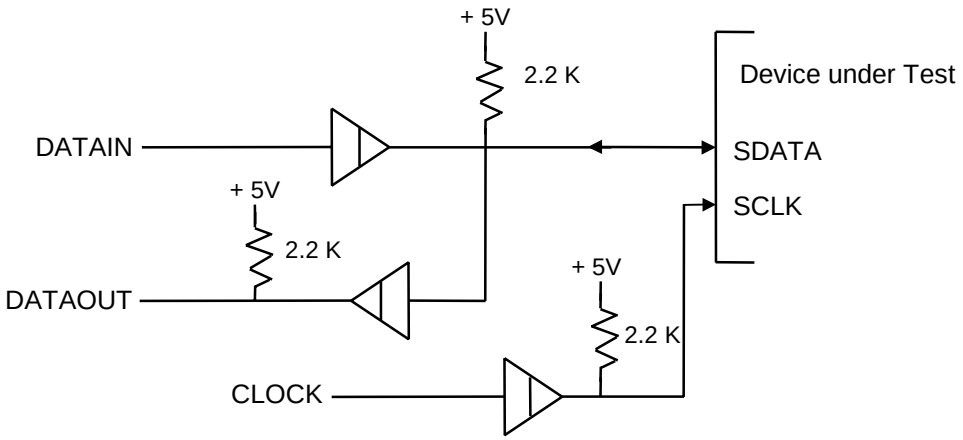
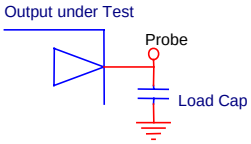



Fig.9

Note: Buffer is 7407 with VCC @ 5.0V

## Test and Measurement Condition




**3.3V signals**

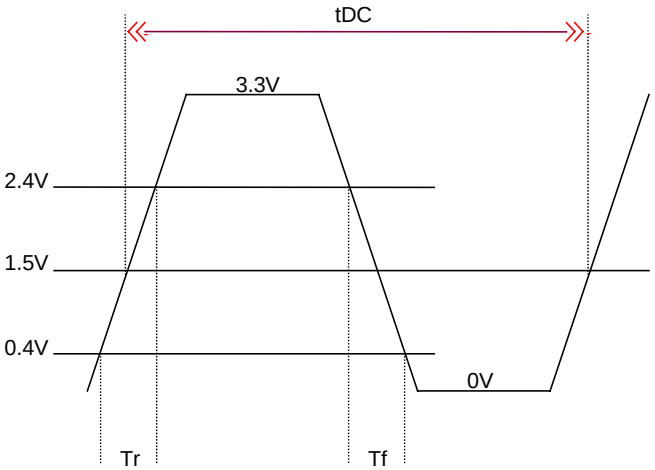



Fig.10A

**2.5V signals**

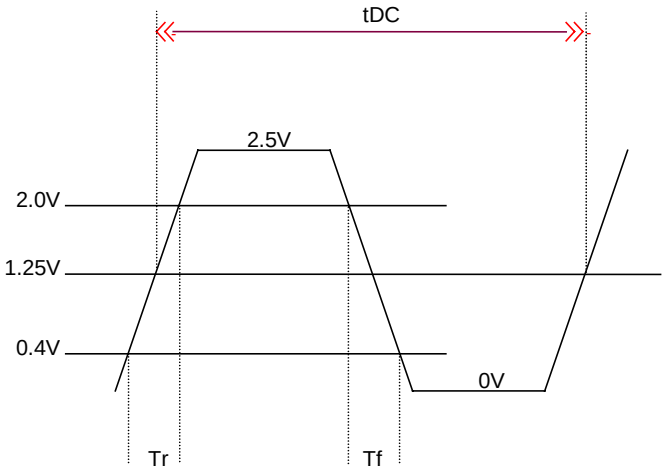



Fig.10B

## AC Parameters

| Symbol | Parameter | 133MHz Host | | 100MHz Host | | 66MHz Host | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| TPeriod | CPU(0:1) period[1,2] | 7.5 | 8.0 | 10.0 | 10.5 | 15.0 | 15.5 | ns |
| THIGH | CPU(0:1) high time[6] | 1.87 | - | 3.0 | - | 5.2 | - | ns |
| TLOW | CPU(0:1) low time[7] | 1.67 | - | 2.8 | - | 5.0 | - | ns |
| Tr / Tf | CPU(0:1) rise and fall times[3] | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns |
| TSKEW | CPU0 to CPU Skew[2,5] | - | 175 | - | 175 | - | 175 | ps |
| TCCJ | CPU(0:1) Cycle to Cycle Jitter[2,5] | - | 250 | - | 250 | - | 250 | ps |
| TPeriod | SDRAM(0:8) period[1,2] | 7.5 | 8.0 | 10.0 | 10.5 | 10.0 | 10.5 | ns |
| THIGH | SDRAM(0:8) high time[6] | 1.87 | - | 3.0 | - | 3.0 | - | ns |
| TLOW | SDRAM(0:8) low time[7] | 1.67 | - | 2.8 | - | 2.8 | - | ns |
| Tr / Tf | SDRAM(0:8) rise and fall times[3] | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns |
| TSKEW | (Any SDRAM) to (any SDRAM) Skew[2,5] | - | 250 | - | 250 | - | 250 | ps |
| TCCJ | SDRAM(0:8) Cycle to Cycle Jitter[2,5] | - | 250 | - | 250 | - | 250 | ps |
| TPeriod | IOAPIC period[1,2] | 30.0 | - | 30.0 | - | 30.0 | - | ns |
| THIGH | IOAPIC high time[6] | 12.0 | - | 12.0 | - | 12.0 | - | ns |
| TLOW | IOAPIC low time[7] | 12.0 | - | 12.0 | - | 12.0 | - | ns |
| Tr / Tf | IOAPIC rise and fall times[3] | 0.4 | 1.6 | 0.4 | 1.6 | 0.4 | 1.6 | ns |
| TCCJ | IOAPIC Cycle to Cycle Jitter[2,5] | - | 500 | - | 500 | - | 500 | ps |
| TPeriod | 3V66-(0:2) period[1,2] | 15.0 | 16.0 | 15.0 | 16.0 | 15.0 | 16.0 | ns |
| THIGH | 3V66-(0:2) high time[6] | 5.25 | - | 5.25 | - | 5.25 | - | ns |
| TLOW | 3V66-(0:2) low time[7] | 5.05 | - | 5.05 | - | 5.05 | - | ns |
| Tr / Tf | 3V66-(0:2) rise and fall times[3] | 0.5 | 2.0 | 0.5 | 2.0 | 0.5 | 2.0 | ns |
| TSKEW | (Any 3V66) to (any 3V66) Skew[2,5] | - | 175 | - | 175 | - | 175 | ps |
| TCCJ | 3V66-(0:2) Cycle to Cycle Jitter[2,5] | - | 500 | - | 500 | - | 500 | ps |
| Tperiod0 | PCI(0:4) period[1,2] | 30.0 | - | 30.0 | - | 30.0 | - | ns |
| THIGH | PCI(0:4) period[6] | 12.0 | - | 12.0 | - | 12.0 | - | ns |
| TLOW | PCI(0:4) low time[7] | 12.0 | - | 12.0 | - | 12.0 | - | ns |
| Tr / Tf | PCI(0:4) rise and fall times[3] | 0.5 | 2.0 | 0.5 | 2.0 | 0.5 | 2.0 | ns |
| TSKEW | (Any PCI) to (Any PCI) Skew[2,5] | - | 500 | - | 500 | - | 500 | ps |
| TCCJ | PCI(0:4) Cycle to Cycle Jitter[2,5] | - | 500 | - | 500 | - | 500 | ps |
| TPeriod | DOT & USB period (conforms to +167ppm max) [1,2] | 20.8299 | 20.8333 | 20.8299 | 20.8333 | 20.829 | 20.833 | ns |
| Tr / Tf | DOT & USB rise and fall times[3] | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | ns |
| TCCJ | DOT & USB Cycle to Cycle Jitter[2,5] | - | 500 | - | 500 | - | 500 | ps |

| Symbol | Parameter | 133MHz Host | | 100MHz Host | | 66MHz Host | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Tperiod | REF period[1,2] | 69.8413 | 71.0 | 69.8413 | 71.0 | 69.8413 | 71.0 | ns |
| Tr / Tf | REF rise and fall times[3] | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | ns |
| TCCJ | REF Cycle to Cycle Jitter[2] | - | 1000 | - | 1000 | - | 1000 | ps |
| TpZL, tpZH | Output enable delay (all outputs) [4] | 1.0 | 10.0 | 1.0 | 10.0 | 1.0 | 10.0 | ns |
| tstable | All clock Stabilization from power-up[8] | | 3 | | 3 | | 3 | ms |
| Tduty | Duty Cycle for All outputs[9] | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Note 1:** This parameter is measured as an average over 1us duration, with a crystal center frequency of 14.31818MHz
**Note 2:** All outputs loaded as per table 5, Probes are placed on the pins and taken at 1.5V levels for 3.3V signals and at 1.25V for 2.5V signals (figs. 10A and 10B).
**Note 3:** Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Fig.10A and Fig.10B)
**Note 4:** Measured from when TS#/PD# is switched to high (enable).
**Note 5:** This measurement is applicable with Spread ON or Spread OFF.
**Note 6:** Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals, (see Figs. 10A & 10B)
**Note 7:** Probes are placed on the pins, and measurements are acquired at 0.4V.
**Note 8:** The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications
**Note 9:** Device designed for Typical Duty Cycle of 50%.

## Output Buffer Characteristics

**CPU and IOAPIC**

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current | $IOH_1$ | -15 | -31 | -50 | mA | Vout =VDDC - 0.5V (or VDDI - 0.5V) |
| Pull-Up Current | $IOH_2$ | -26 | -58 | -101 | mA | Vout = 1.2V |
| Pull-Down Current | $IOL_1$ | 12 | 24 | 40 | mA | Vout = 0.4V |
| Pull-Down Current | $IOL_2$ | 27 | 56 | 93 | mA | Vout = 1.2V |

**PCI, 3V66 and DOT**

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current | $IOH_1$ | -20 | -25 | -33 | mA | Vout =VDD - 1.0V |
| Pull-Up Current | $IOH_2$ | -30 | -54 | -184 | mA | Vout = 1.5V |
| Pull-Down Current | $IOL_1$ | 9.4 | 18 | 38 | mA | Vout = 0.4V |
| Pull-Down Current | $IOL_2$ | 28 | 55 | 148 | mA | Vout = 1.5V |

**USB and REF**

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current | $IOH_1$ | -12 | -20 | -30 | mA | Vout =VDD - 1.0V |
| Pull-Up Current | $IOH_2$ | -27 | -43 | -92 | mA | Vout = 1.5V |
| Pull-Down Current | $IOL_1$ | 9 | 13 | 27 | mA | Vout = 0.4V |
| Pull-Down Current | $IOL_2$ | 26 | 39 | 79 | mA | Vout = 1.5V |

**SDRAM**

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current | $IOH_1$ | -30 | -40 | -60 | mA | Vout =VDDS - 1. 0V |
| Pull-Up Current | $IOH_2$ | -68 | -110 | -188 | mA | Vout = 1.4V |
| Pull-Down Current | $IOL_1$ | 23 | 34 | 53 | mA | Vout = 0.4V |
| Pull-Down Current | $IOL_1$ | 64 | 98 | 159 | mA | Vout = 1.5V |
| **VDD = VDDS = 3.3V ±5%, VDDC = VDDI = 2.5±5%, TA = 0 to 70ºC** | | | | | | |

## Suggested Crystal Oscillator Parameters

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Frequency | $F_o$ | 12.00 | 14.31818 | 16.00 | MHz | |
| Tolerance | TC | - | - | +/-100 | PPM | Note 1 |
| | TS | - | - | +/- 100 | PPM | Stability (Ta -10 to +60C) Note 1 |
| | TA | - | - | 5 | PPM | Aging (first year @ 25C) Note 1 |
| Mode | OM | - | - | - | | Parallel Resonant, Note 1 |
| Load Capacitance | CL | - | 20 | - | pF | The crystal's rated load. Note 1 |
| Effective Series resistance (ESR) | R1 | - | 40 | - | Ohms | Note 1 |
| Power Dissipation | DL | - | - | 0.10 | mW | Note 1 |

Note1: For best performance and accurate Center frequencies of this device, It is recommended but not mandatory that the chosen crystal meets these specifications

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Device pin capacitance: Cxtal = 36pF
In order to meet the specification for CL = 18pF following the formula:

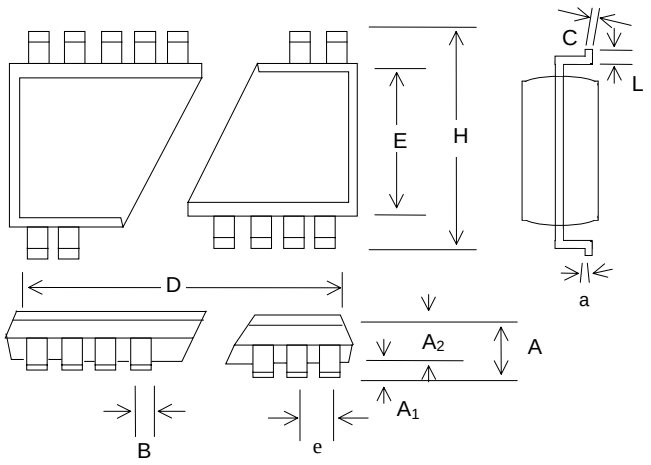
$$C_L = \frac{(C_{XINTRACE} + C_{XINDEVICE}) \times (C_{XOUTTRACE} + C_{XOUTDEVICE})}{(C_{XINTRACE} + C_{XINDEVICE}) + (C_{XOUTRACE} + C_{XOUTDEVICE})}$$

Then the board trace capacitance between Xin and the crystal should be no more than 4pF. (Same is applicable to the trace between Xout and the crystal)

In this case the total capacitance from the crystal to Xin will be 40pF. Similarly the total capacitance between the crystal and Xout will be 36pF. Hence using the above formula:

$$C_L = \frac{40 \times 40}{40 + 40} = 20pF$$

## Package Drawing and Dimensions




### 48 Pin SSOP Outline Dimensions

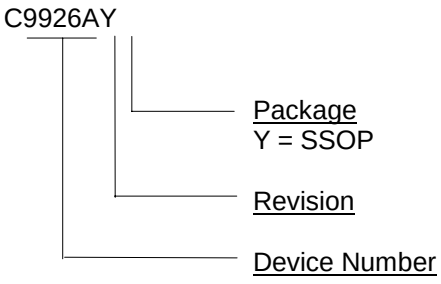
| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.095 | 0.102 | 0.110 | 2.41 | 2.59 | 2.79 |
| $A_1$ | 0.008 | 0.012 | 0.016 | 0.20 | 0.30 | 0.41 |
| A2 | 0.088 | - | 0.092 | 2.24 | - | 2.34 |
| b | 0.008 | 0.010 | 0.0135 | 0.203 | 0.254 | 0.343 |
| C | 0.005 | 0.008 | 0.010 | 0.127 | 0.20 | 0.254 |
| D | 0.620 | 0.625 | 0.630 | 15.75 | 15.88 | 16.00 |
| E | 0.291 | 0.295 | 0.299 | 7.39 | 7.49 | 7.60 |
| e | 0.025 BSC | | | 0.635 BSC | | |
| H | 0.395 | 0.408 | 0.420 | 10.03 | 10.36 | 10.67 |
| L | 0.020 | 0.030 | 0.040 | 0.508 | 0.76 | 1.016 |
| a | 0º | 4º | 8º | 0º | 4º | 8º |

## Ordering Information

| Part Number | Package Type | Production Flow |
|---|---|---|
| C9926AY | 48 PIN SSOP | Commercial, 0° to 85°C |

Document # : 38-07070

Marking: Example: Cypress
C9926AY
Date Code, Lot #

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**Document Title:** C9926 Low EMI Clock Generator for Intel® 133 MHz/ 2DIMM Chipset Systems
**Document Number:** 38-07070

| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
|---|---|---|---|---|
| ** | 107106 | 06/07/01 | IKA | Convert from IMI to Cypress |