C9950

3.3V, 180MHz, Multi-Output Clock Driver

Product Features

- 180MHz Clock Support
- Supports PowerPC™, Intel and RISC Processors
- 9 Clock Outputs: Frequency Configurable
- Oscillator or Crystal Reference Input
- Output Disable Control
- Spread Spectrum Compatible
- Pin Compatible with MPC950
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin TQFP Package

Block Diagram

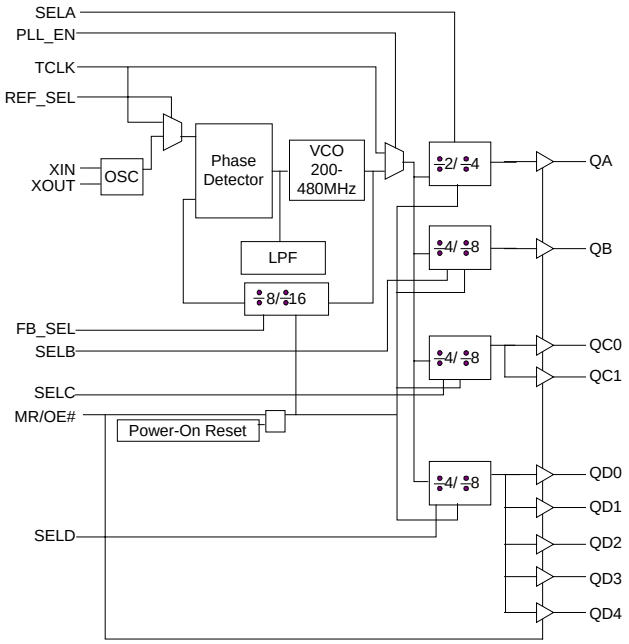


Figure 1

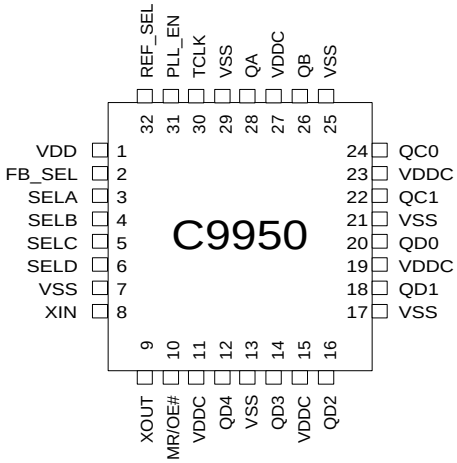
Frequency Table

SEL (A:D)	FB_SEL = 1				FB_SEL = 0			
	QA	QB	QC (0,1)	QD (0:4)	QA	QB	QC (0,1)	QD (0:4)
0000	4x	2x	2x	2x	8x	4x	4x	4x
0001	4x	2x	2x	x	8x	4x	4x	2x
0010	4x	2x	x	2x	8x	4x	2x	4x
0011	4x	2x	x	x	8x	4x	2x	2x
0100	4x	x	2x	2x	8x	2x	4x	4x
0101	4x	x	2x	x	8x	2x	4x	2x
0110	4x	x	x	2x	8x	2x	2x	4x
0111	4x	x	x	x	8x	2x	2x	2x
1000	2x	2x	2x	2x	4x	4x	4x	4x
1001	2x	2x	2x	x	4x	4x	4x	2x
1010	2x	2x	x	2x	4x	4x	2x	4x
1011	2x	2x	x	x	4x	4x	2x	2x
1100	2x	x	2x	2x	4x	2x	4x	4x
1101	2x	x	2x	x	4x	2x	4x	2x
1110	2x	x	x	2x	4x	2x	2x	4x
1111	2x	x	x	x	4x	2x	2x	2x

Table 1

* x = is the reference input frequency

Pin Configuration



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Pin Description

PIN	NAME	PWR	I/O	TYPE	Description
8	**XIN**		I		Oscillator Input. Connect to a crystal.
9	**XOUT**		0		Oscillator Output. Connect to a crystal.
30	**TCLK**		I		External Test Clock Input.
28	**QA**	VDDC	O		Clock Output. See Frequency Table.
26	**QB**	VDDC	O		Clock Output. See Frequency Table.
22, 24	**QC(1,0)**	VDDC	O		Clock Outputs. See Frequency Table.
12, 14, 16, 18, 20	**QD(4:0)**	VDDC	O		Clock Outputs. See Frequency Table.
2	**FB_SEL**		I	PD	Feedback Select Input. If FB_SEL = 1, then the (÷8) counter is selected in the PLL feedback loop. If FB_SEL = 0, then the (÷16) counter is selected in the PLL feedback loop.
10	**MR/OE#**		I		Master Reset/Output Enable Input. When asserted high, resets all of the internal flip-flops and also disables all of the outputs. When pulled low, releases the internal flip-flops from reset and enables all of the outputs.
31	**PLL_EN**		I		PLL Enable Input. When asserted high, PLL is enabled. And when set low, PLL is bypassed.
32	**REF_SEL**		I		Reference Select Input. When high, TCLK is the reference clock and when low, the crystal oscillator is selected.
3, 4, 5, 6	**SEL(A:D)**		I		Frequency Select Inputs. See Frequency Table. If SEL_ = 1, then QA divider = ÷4, QB:D divider = ÷8 If SEL_ = 0, then QA divider = ÷2, QB:D divider = ÷4
11, 15, 19, 23, 27	**VDDC**				3.3V Power Supply for Output Clock Buffers.
1	**VDD**				3.3V Power Supply for PLL
7, 13, 17, 21, 25, 29	**VSS**				Common Ground

PD = Internal Pull-Down, PU = Internal Pull-Up.

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Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: -40°C to +85°C
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V
Maximum Input Current: ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	V	
Input High Voltage	VIH	2.0	-	-	V	
Input Low Current (@VIL = VSS)	IIL			-120	µA	Note 1
Input High Current (@VIL =VDD)	IIH			120	µA	Note 1
Output Low Voltage	VOL			0.5	V	IOL = 40mA, Note 2
Output High Voltage	VOH	2.4			V	IOH = -40mA, Note 2
Quiescent Supply Current	IDDC	-	15	20	mA	All VDDC and VDD
PLL Supply Current	IDD	-	15	20	mA	VDD only
Input Capacitance	Cin	-	-	4	pF	
VDD = VDDC = 3.3V ±5%, TA = -40°C to +85°C						

Note 1: Inputs have internal pull-up/pull-down resistors that affect input current**.**
Note 2: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission. Output buffers are dual staged to control drive strength in order to reduce over / under shoot.

AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Tr / Tf	TCLK Input Rise / Fall			3.0	ns	
Fref	Reference Input Frequency	Note 2		Note 2	MHz	
Fxtal	Crystal Oscillator Frequency	10		25	MHz	See Table 3 for details
FrefDC	Reference Input Duty Cycle	25		75	%	
Fvco	PLL VCO Lock Range	200		480	MHz	
Tlock	Maximum PLL lock Time			10	ms	
Tr / Tf	Output Clocks Rise / Fall Time[3]	0.10		1.0	ns	0.8V to 2.0V
Fout	Maximum Output Frequency	-		180	MHz	QA = (÷2)
				120		QA/QB = (÷4)
				60		QB = (÷8)
FoutDC	Output Duty Cycle	TCYCLE/2 – 1		TCYCLE/2 + 1	ns	
tpZL, tpZH	Output enable time (all outputs)			6	ns	
tpLZ, tpHZ	Output disable time (all outputs)			7	ns	
TCCJ	Cycle to Cycle Jitter (peak to peak)[3]		+/- 100		ps	
TSKEW0	Any Output to Any Output Skew[3]	-	200	350	ps	
VDD = VDDC = 3.3V ± 5%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production.
Note 2: Maximum and minimum input reference is limited by the VCO lock range.
Note 3: Outputs loaded with 30pF each.

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Description

The C9950 has an integrated PLL that provides low skew and low jitter clock outputs for high performance microprocessors. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 480 MHz. This allows a wide range of output frequencies from 25MHz to 180MHz. The internal VCO frequency is divided by 8 or 16 and compared to the input reference clock. These selectable dividers allow for input reference clock flexibility. The internal VCO is running at 2x or 4x the high speed output (QA), and 4x or 8x the outputs Q(B:D) depending on the configuration (see table 2). The use of even dividers ensures that the output duty cycle remains at 50%.

Output Frequency

The C9950 generates outputs with programmable frequency relationships. As a result, the input reference frequency is a function of the desired output frequency (see Table 1). The following block diagram illustrates the corresponding parameters that are needed to calculate the output frequency.

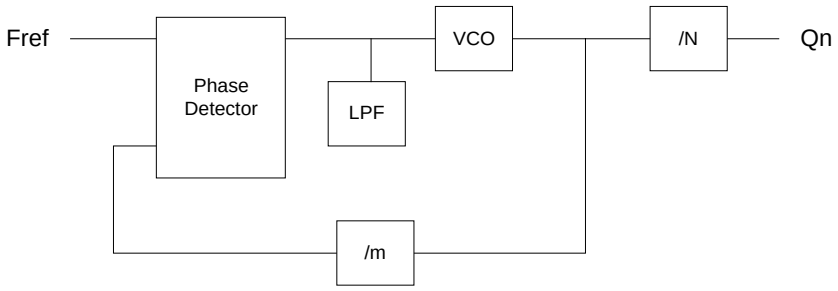


Figure 2

Fref = FVCO/m, FVCO = FQn x N
Fref = (FQn x N) / m

Where m = 8 (FB_SEL = 1) or m = 16 (FB_SEL = 0), and N = 2, 4, or 8 depending on SEL_ as shown in Table 1.

INPUTS				OUTPUTS			
SELA	SELB	SELC	SELD	QA	QB	QC	QD
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

Table 2

Suggested Oscillator Crystal Parameters

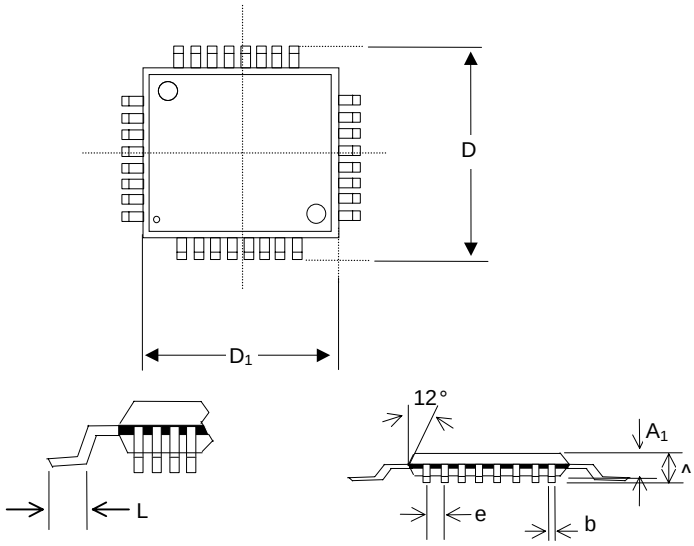
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency Tolerance	T_C	-	-	+/-100	PPM	Note 1
Frequency Temperature Stability	T_S	-	-	+/- 100	PPM	(T_A -10 to +60C) Note 1
Aging	T_A	-	-	5	PPM/Yr	(first 3 years @ 25C) Note 1
Load Capacitance	C_L	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	80	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

Table 3

Package Drawing and Dimensions



32 Pin TQFP Outline Dimensions

	MILLIMETERS			INCHES		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	1.000	1.100	1.200	0.039	0.043	0.047
A_1	0.950	1.000	1.050	0.037	0.039	0.041
D	8.950	9.000	9.050	0.352	0.354	0.356
D_1	6.95	7.000	7.050	0.274	0.276	0.278
b	0.30	0.37	0.45	0.012	0.015	0.018
e	0.80 BSC			0.031 BSC		
L	0.45	0.600	0.75	0.018	0.024	0.030

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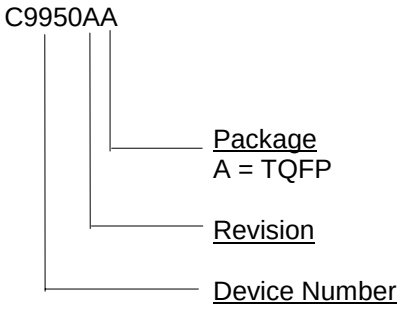
Ordering Information

Part Number	Package Type	Production Flow
C9950AA	32 PIN TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
C9950AA
Date Code, Lot #



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Document Title: C9950 3.3V, 180MHz, Multi-Output Clock Driver **Document Number:** 38-07072				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107108	06/11/01	IKA	Convert from IMI to Cypress
*A	108125	07/03/01	NDP	Delete Pull Down in Pin 10, 30, & 32 and Pull Up in Pin 3, 4, 4, 5, 6, & 31(See page 2)