



Clock Generator for the DVD Player

Product Features

- 2 PLLs
- Standard 16.9344 MHz Crystal Frequency
- 3 Clock outputs
 - 27 MHz
 - 16.9344 MHz
 - 36.864, 16.9344 MHz selectable
- Very low jitter
- On chip load capacitors for XIN/XOUT
- Integrated loop filter
- Single power supply 3.3V
- 8 pin SOIC package

Product Description

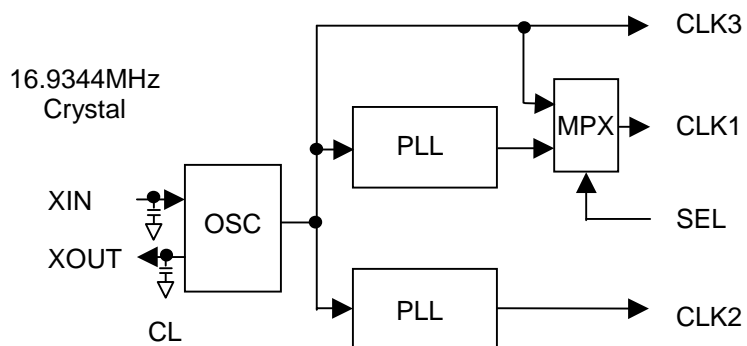
The Cypress CG804 is designed to support the clocking requirements for DVD / MPEG systems. It generates three clock outputs from a crystal oscillator. The center frequency of these outputs is designed to be highly accurate in order to maintain reliable system stability.

Frequency Selection Table

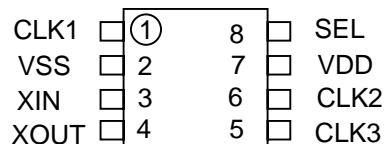
| SEL | CLK1 | CLK2 | CLK3 |
|-----|------------|------------|------------|
| 0 | 36.864MHz | 27.0000MHz | 16.9344MHz |
| 1 | 16.9344MHz | 27.0000MHz | 16.9344MHz |

PLL counter accuracy on all frequencies are 0ppm error.

Block Diagram



Pin Configuration



**Clock Generator for the DVD Player****Pin Description**

| Pin No. | Pin Name | I/O | Description |
|---------|----------|-----|---|
| 1 | CLK1 | O | 36.864 or 16.9344MHz selected by input pin SEL. |
| 2 | VSS | P | Circuit ground. |
| 3 | XIN | I | Input from Crystal or external input. |
| 4 | XOUT | O | Connect to crystal or open if external input is used. |
| 5 | CLK3 | O | 16.9344MHz fixed output. |
| 6 | CLK2 | O | 27.00MHz fixed output. |
| 7 | VDD | P | Positive power supply. |
| 8 | SEL | I | Input pin for frequency selection for CLK1 output. Pull-up to VDD |

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V

Maximum Input Voltage Relative to VDD: VDD + 0.3V

Storage Temperature: -65°C to + 150°C

Operating Temperature: -40°C to +85°C

Maximum Power Supply: 7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).



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Electrical Characteristics

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|--------------------------------------|-----------------|-----|------|-----|-------|--|
| Output High Voltage | VOH | 2.4 | - | - | V | IOH=-4.0mA |
| Output Low Voltage | VOL | - | - | 0.4 | V | IOL=4.0mA |
| Input High Voltage | VIH | 2.0 | - | - | V | Note-1 |
| Input Low Voltage | VIL | - | - | 0.8 | V | Note-1 |
| Input High Current | I _{IH} | - | - | 5 | μA | Note-1, V _{IH} =V _{DD} -0.5V |
| Input Low Current | I _{IL} | -50 | - | - | μA | Note-1, V _{IL} =0.5V |
| Load Capacitance | CL | - | 10.5 | - | PF | |
| Dynamic Supply Current | IDD | - | 20 | 40 | MA | Clockouts are loaded with a 15pf @VDD=3.3V |
| VDD = 3.3V ±10%, TA = -40°C to +85°C | | | | | | |

Note-1: Applicable to SEL pin.

AC Parameters

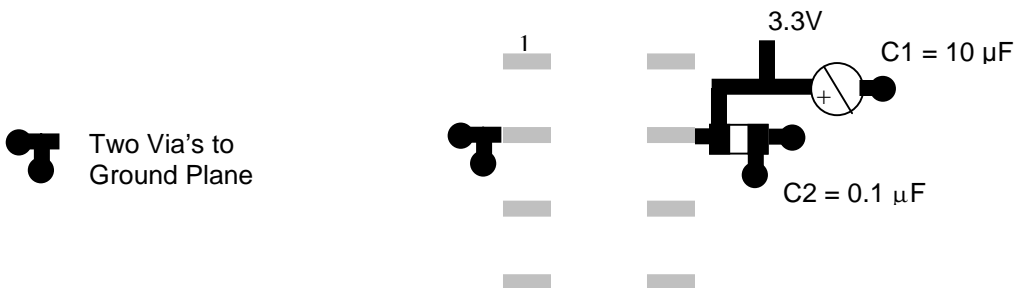
| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|--|-------------------|-----|-----|-----|-------|--|
| Frequency error, all output clock | Ferror | - | - | 0 | Ppm | PLL counter accuracy. Input Crystal Frequency = 16.9344MHz |
| Rise time | Tr | - | 3 | 5 | NS | 15pf Load, all outputs, Note 2 |
| Fall time | Tf | - | 2.5 | 4 | NS | 15pf Load, all outputs, Note 2 |
| Duty Cycle -1 | T _{dy-1} | 45 | 50 | 55 | % | 15pf Load, CLK-1&CLK-2, Note 3 |
| Duty Cycle -2 | T _{dy-2} | 40 | 50 | 60 | % | 15pf Load, CLK-3, Note 3 |
| Clock Jitter, peak to peak period jitter | T _{j1} | - | 400 | 500 | PS | 15pf Load, all outputs |
| Crystal Startup time | Txs | - | - | 40 | μS | From Stable 3.3V power supply. |
| Maximum PLL Lock Time ⁽¹⁾ | TLOCK | - | - | 10 | MS | Stable power supply, valid clocks presented on all outputs |
| VDD = 3.3V ±10%, TA = -40°C to +85°C | | | | | | |

Note 2: Measurements are done between 0.4V and 2.4V.

Note 3: Measurement done at 1.5V

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PCB Layout Suggestion

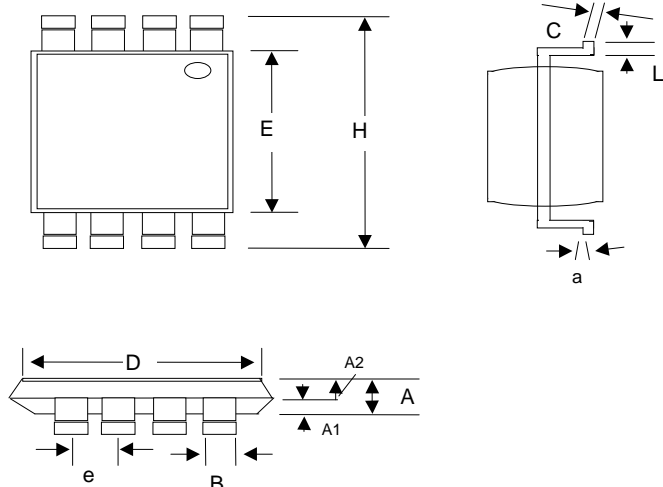


NOTE:

Power supply bypass capacitor C2 (0.1 uf.) must be positioned as close as possible (< 0.2inches) to the VDD pin. Otherwise, its filtering function will not be effective, which would result in higher jitter in the device. Capacitors must be low leakage such as multilayer ceramic Z5U or X7R material.

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Package Drawing and Dimensions



8-PIN SOIC OUTLINE DIMENSIONS

| SYMBOL | INCHES | | | MILLIMETERS | | |
|----------------|----------|------|-------|-------------|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .061 | .064 | .068 | 1.55 | 1.63 | 1.73 |
| A ₁ | .004 | .006 | .0098 | 0.127 | 0.15 | 0.25 |
| A ₂ | .055 | .058 | .061 | 1.40 | 1.47 | 1.55 |
| B | 0.138 | .016 | .0192 | 0.35 | 0.41 | 0.49 |
| C | .0075 | .008 | .0098 | 0.19 | 0.20 | 0.25 |
| D | .189 | .194 | .196 | 4.80 | 4.93 | 4.98 |
| E | .150 | .155 | .157 | 3.81 | 3.94 | 3.99 |
| e | .050 BSC | | | 1.27 BSC | | |
| H | .230 | .236 | .244 | 5.84 | 5.99 | 6.20 |
| L | .016 | .025 | .035 | 0.41 | 0.64 | 0.89 |
| a | 0° | 5° | 8° | 0° | 5° | 8° |

Ordering Information

| Part Number | Package Type | Production Flow |
|-------------|--------------|-----------------|
| CG804AZ | 8 Pin SOIC | -40°C to +85°C |

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
CG804AZ
Date Code, Lot #

CG804AZ

Package
Z = SOIC

Revision

Device Number

Notice

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APPROVED PRODUCT

CG804

Clock Generator for the DVD Player

Document Title: CG804 Clock Generator for the DVD Player

Document Number: 38-07032

| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
|------|---------|------------|-----------------|-----------------------------|
| ** | 106960 | 06/12/01 | IKA | Convert from IMI to Cypress |