*Preliminary*

# CY2CC1810

## *1:10 Signal Fanout Buffer w/ Output Enable*

## ComL™ SERIES

### Product Features

- Low Voltage Operation
  *VDD range from 3.6 to 1.65V*
- 1:10 Fanout
- Low input capacitance
- Low output skew
- Low propagation delay
  *High Speed (tpd<5.0ns)*
- High Speed Operation >200MHz
- LVTTL/LVCMOS compatible input
  *Output Disable to Tri-state*
- VOI ™ Output Drivers for low noise
  *Eliminates the need for series damping resistors*
- Industrial Operation at 0°C to +85°C
- Packages available include: SOIC/SSOP

### Product Description

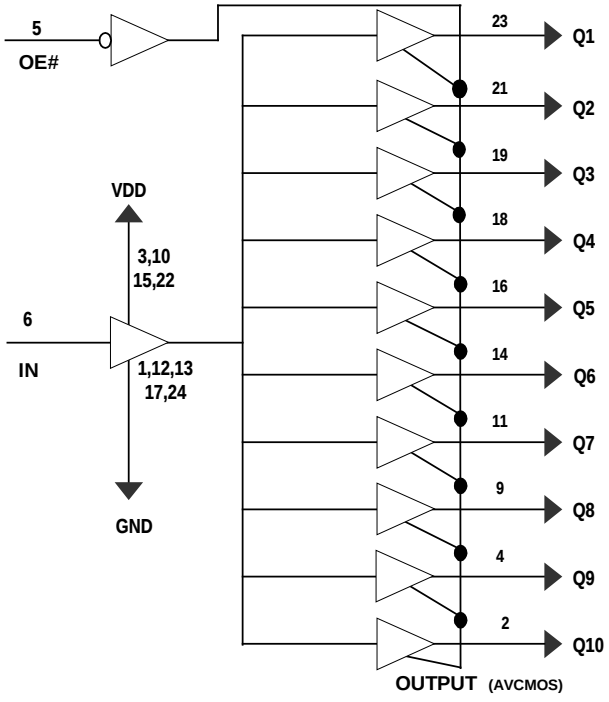
The CYPRESS ComL series of network circuits are produced using advanced 0.35 micron CMOS technology, achieving the industries fastest logic and buffers.

The CYPRESS CY2CC1810 fanout buffer features one input and ten outputs.

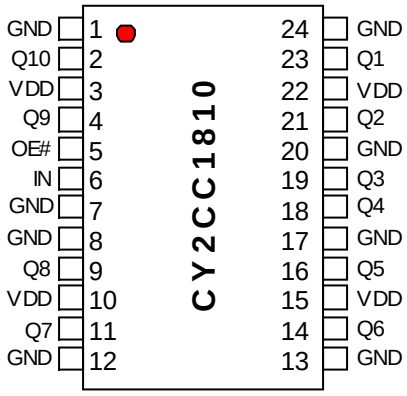
Designed for Data Communications clock management applications, the large fanout from a single input reduces loading on the input clock.

AVCMOS type outputs dynamically adjust for variable impedance matching and eliminate the need for series damping resistors and reduce noise overall.

### Block Diagram




### Pin Configuration




*24 pin SOIC/SSOP*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## ComL™ SERIES

## Pin Description

| Pin Number | Pin Name | Description | |
|---|---|---|---|
| 1,7,8,12,13,17,20,24 | GND | Ground | Power |
| 3,10,15,22 | $V_{DD}$ | Power Supply | Power |
| 5 | OE# | Output Enable | LVTTL / LVCMOS |
| 6 | IN | Input | LVTTL / LVCMOS |
| 2,4,9,11,14,16,18,19,21,23 | Q10,Q9,Q8,Q7,Q6,Q5,Q4,Q3,Q2,Q1 | Output | AVC CMOS |

All power pins must be connected. Input pins shall be connected or pulled by resistors to be a 1 or a zero.

## Absolute Maximum Ratings:

| | |
|---|---|
| Storage Temperature | -65°C to 150°C |
| Ambient Temperature | 0°C to +85°C |
| Supply Voltage to Ground Potential (Inputs and $V_{DD}$ only) | -0.5V to 4.6V |
| Supply Voltage to Ground Potential (outputs and D/O only) | -0.5V to $V_{DD}$+0.5V |
| DC Input Voltage | -0.5V to $V_{DD}$+0.5V |
| DC Output Voltage | -0.5V to $V_{DD}$+0.5V |
| Power Dissipation | 0.75W |

***Note**: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

## ComL™ SERIES

## D.C. Electrical Characteristics: @ 3.3V

*D.C. Electrical Characteristics (Over the Operating Range , TA = 0°C to +85°C, VDD=3.3V +/-5%*

| Parameter | Description | Test Conditions | | Min. | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{DD}$=Min., $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OH}$= -12mA | 2.3 | 3.3 | | V |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$=Min., $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OL}$= 12mA | | 0.2 | 0.5 | V |
| $V_{IH}$ | Input High Voltage | Guaranteed Logic High Level | | 2 | | | V |
| $V_{IL}$ | Input Low Voltage | Guaranteed Logic Low Level | | | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{DD}$=Max | $V_{IN}$=2.7V | | | 1 | uA |
| $I_{IL}$ | Input Low Current | $V_{DD}$=Max | $V_{IN}$=0.5V | | | -1 | uA |
| $I_I$ | Input High Current | $V_{DD}$=Max., $V_{IN}$=$V_{DD}$(Max) | | | | 20 | uA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$=Min., $I_{IN}$ = -18mA | | | -0.7 | -1.2 | V |
| $I_{OK}$ | Continuous Clamp Current | $V_{DD}$=Max, $V_{OUT}$ = GND | | | | -50 | mA |
| $O_{OFF}$ | Power Down Disable | $V_{DD}$ = GND, $V_{OUT}$ =<4.5V | | | | 100 | uA |
| $V_H$ | Input Hysteresis | | | | 80 | | mV |

## D.C. Electrical Characteristics: @ 2.5V

*D.C. Electrical Characteristics (Over the Operating Range , TA = 0°C to +85°C, VDD=2.5 +/-5%*

| Parameter | Description | Test Conditions | | Min. | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{DD}$=Min., $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OH}$= -7mA | 1.80 | | | V |
| | | | $I_{OH}$= -15.2mA | 1.60 | | | V |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$=Min., $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OL}$= 15.2mA | 0.65 | | | V |
| $V_{IH}$ | Input High Voltage | Guaranteed Logic High Level | | 1.60 | | | V |
| $V_{IL}$ | Input Low Voltage | Guaranteed Logic Low Level | | | | 0.9 | V |
| $I_{IH}$ | Input High Current | $V_{DD}$=Max | $V_{IN}$=2.4V | | | 1 | uA |
| $I_{IL}$ | Input Low Current | $V_{DD}$=Max | $V_{IN}$=0.5V | | | -1 | uA |
| $I_I$ | Input High Current | $V_{DD}$=Max, $V_{IN}$=$V_{DD}$(Max) | | | | 20 | uA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{DD}$=Min. $I_{IN}$ = -18mA | | | -0.7 | -1.2 | V |
| $I_{OK}$ | Continuous Clamp Current | $V_{DD}$=Max, $V_{OUT}$ = GND | | | | -50 | mA |
| $O_{OFF}$ | Power Down Disable | $V_{DD}$ = GND, $V_{OUT}$ =<4.5V | | | | 100 | uA |
| $V_H$ | Input Hysteresis | | | | 80 | | mV |

## ComL™ SERIES

### Capacitance:

| Parameter | Description | Test Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| Cin | Input Capacitance | Vin = 0V | 2.5 | 5 | pF |
| Cout | Output Capacitance | Vout = 0V | 6.5 | 8 | pF |

### Power Supply Characteristics:

| Symbol | Parameter | Test Conditions | | Min. | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ΔICC | Delta Quiescent Power Supply Current LVTTL/LVCMOS Inputs High | **\|value\| = ($V_{DD}$ = Max ) - ($V_{DD}$ = $V_{DD}$-0.6V)** | fL=0Hz | - | 3 | 50 | uA |
| ICCD | Dynamic Power Supply Current | $V_{DD}$ = Max Input toggling 50% Duty Cycle, Outputs Open | fL=fMAX OE# = VDD | - | 1 | 2.2 | mA / MHz |
| IC | Total Power Supply Current | $V_{DD}$ = Max Input toggling 50% Duty Cycle, Outputs Open | fL=100MHz OE# = GND | - | 310 | 350 | mA |

### High Frequency Parametrics :

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fmax | Maximum frequency VDD = 3.3V | 50% duty cycle tW(50-50) Standard Load Circuit | - | - | 160 | MHz |
| | | 50% duty cycle tW(50-50) The “point to point load circuit” | | | 200 | |
| Fmax(20) | Maximum frequency VDD = 3.3 V | 20% duty cycle tW(20-80) The “point to point load circuit” Vin = 3.0V / 0.0V Vout = 2.3V / 0.4V | - | - | 200 | MHz |
| | Maximum frequency VDD = 2.5 V | The “point to point load circuit” Vin = 2.4 / 0.0V Vout = 1.7V / 0.7V | | | 100 | |
| tW | Minimum pulse VDD = 3.3 V | The “point to point load circuit” Vin = 3.0V / 0.0V F = 100MHz Vout = 2.0V / 0.8V | 2 | - | - | nS |
| | Minimum pulse VDD = 2.5 V | The “point to point load circuit” Vin = 2.4 / 0.0V F = 100MHz Vout = 1.7V / 0.7V | 1 | | | |

## ComL™ SERIES

AC Switching Characteristics @ 3.3

*AC Switching Characteristics Over Operating Range VDD = 3.3V +/-5%, Temperature = 0°C to +85°C*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| tPLH | Propagation Delay – Low to High | | - | 3 | - | nS |
| tPHL | Propagation Delay – High to Low | | - | 3 | - | nS |
| tPHZ | Propagation Delay –High to High Z | | - | 4 | - | nS |
| tPLZ | Propagation Delay – Low to High Z | | - | 3 | - | nS |
| tR | Output Rise Time | | - | 0.8 | - | V/nS |
| tF | Output Fall Time | | - | 0.8 | - | V/nS |
| tSK(0) | Output Skew: Skew between outputs of the same package (in phase) | | - | - | 0.2 | nS |
| tSK(p) | Pulse Skew: Skew between opposite transitions of the same output (TPHL – TPLH) | | - | - | 0.2 | nS |
| tSK(t) | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | | - | - | 0.3 | nS |
| toff | Delay from OE to driver off | | | | 4.00 | nS |
| ton | Delay from OE to Driver on | | | | 4.00 | nS |

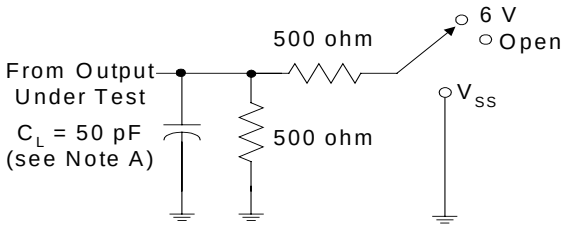
## AC Switching Characteristics @ 2.5

*AC Switching Characteristics Over Operating Range VDD = 2.5V +/-5%, Temperature = 0°C to +85°C*

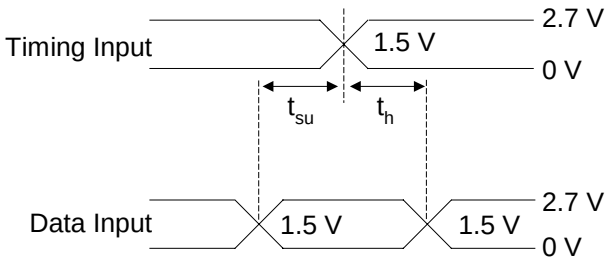
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| tPLH | Propagation Delay – Low to High | | - | 3.8 | - | nS |
| tPHL | Propagation Delay – High to Low | | - | 3.8 | - | nS |
| tPHZ | Propagation Delay –High to High Z | | - | 5 | - | nS |
| tPLZ | Propagation Delay – Low to High Z | | - | 4 | - | nS |
| tR | Output Rise Time | | - | 0.4 | - | V/nS |
| tF | Output Fall Time | | - | 0.6 | - | V/nS |
| tSK(0) | Output Skew: Skew between outputs of the same package (in phase) | | - | - | 0.2 | nS |
| tSK(p) | Pulse Skew: Skew between opposite transitions of the same output (TPHL – TPLH) | | - | - | 0.2 | nS |
| tSK(t) | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. | | - | - | 0.3 | nS |
| toff | Delay from OE to driver off | | | | 5.00 | nS |
| ton | Delay from OE to Driver on | | | | 5.00 | nS |

## ComL™ SERIES
## Parameter Measurement Information

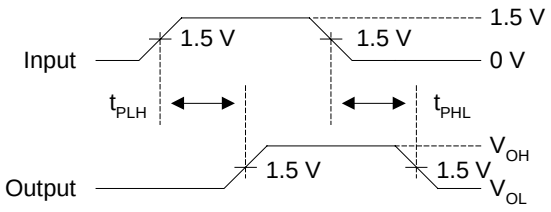
VDD @ 2.5




Load Circuit

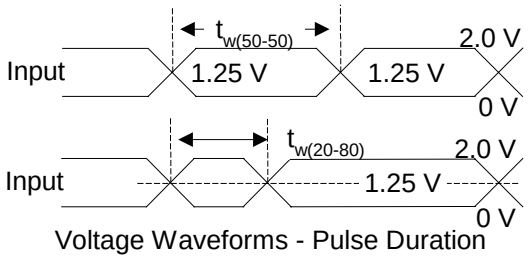



Voltage Waveforms
Setup and Hold Times

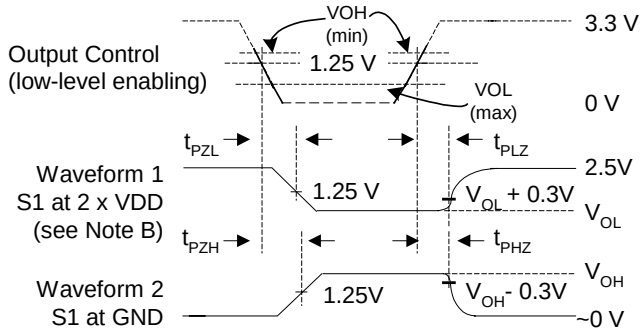



Voltage Waveforms
Propagation Delay Times

| Test | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 x $V_{DD}$ |
| $t_{PHZ}/t_{PZH}$ | $V_{SS}$ |




Voltage Waveforms - Pulse Duration



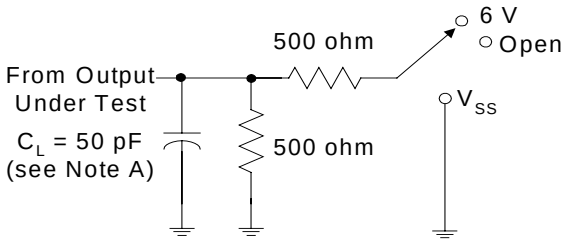

Voltage Waveforms
Enable and Disable Times

**Notes**:

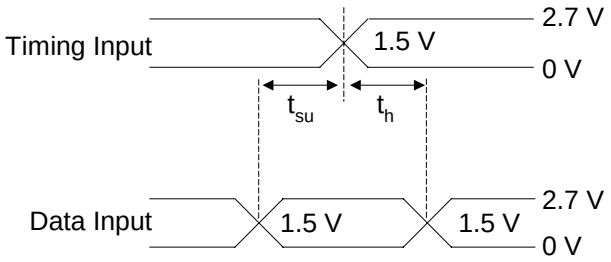
A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 2.5 nS, $t_f$ < 2.5nS.
D. The outputs are measured one at a time with on transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

## Parameter Measurement Information

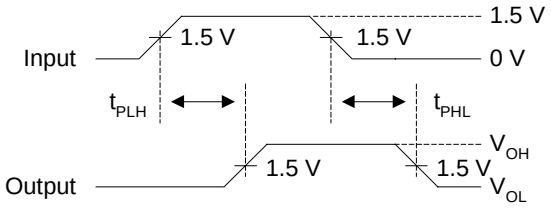
VDD @ 3.3




Load Circuit

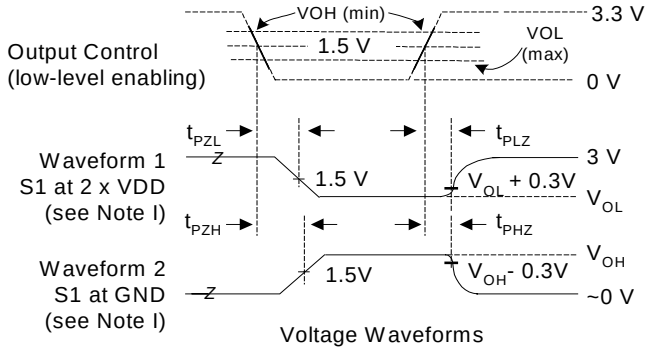



Voltage Waveforms
Setup and Hold Times

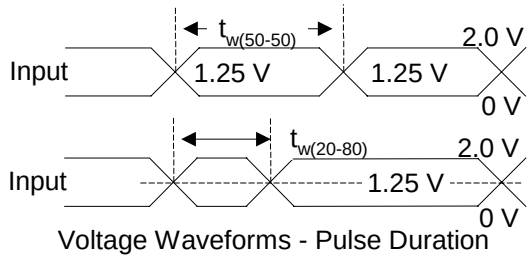



Voltage Waveforms
Propagation Delay Times

| Test | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 x $V_{DD}$ |
| $t_{PHZ}/t_{PZH}$ | $V_{SS}$ |




Voltage Waveforms
Enable and Disable Times




Voltage Waveforms - Pulse Duration

Notes:

H. CL includes probe and jig capacitance.

I. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

J. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, $Z_O$ = 50 Ω, $t_r$ < 2.5 nS, $t_f$ < 2.5nS.

K. The outputs are measured one at a time with on transition per measurement.

L. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

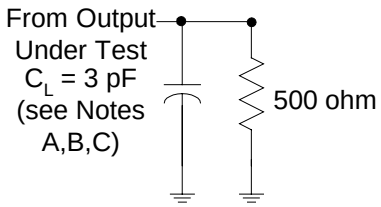
M. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

N. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

## ComL™ SERIES

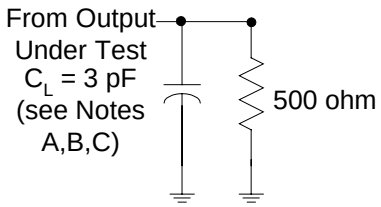
### Parameter Measurement Information

VDD @ 2.5



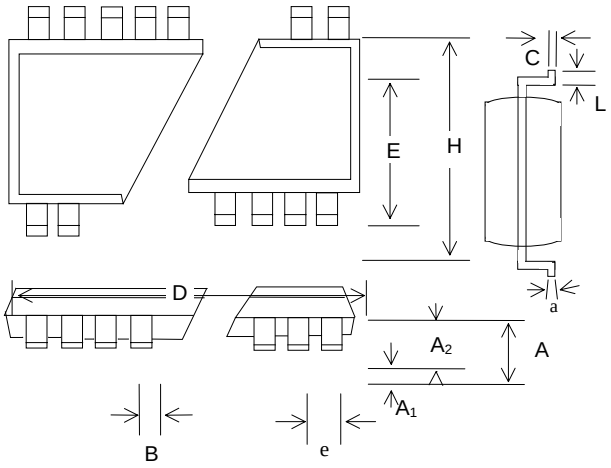

**Point to Point Load Circuit**

VDD @ 3.3




**Point to Point Load Circuit**

## Package Drawing and Dimensions




## 24 Pin SSOP Outline Dimensions

| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | MIN | NOM | MAX |
| A | - | - | .07874 | - | - | 2.0 |
| $A_1$ | .001969 | - | - | 0.05 | - | - |
| A2 | .06496 | .06890 | .07283 | 1.65 | 1.75 | 1.85 |
| B | .008661 | - | .01496 | 0.22 | - | 0.38 |
| C | .003543 | - | .009843 | 0.09 | - | 0.25 |
| D | .3110 | .3228 | .3346 | 7.90 | 8.20 | 8.50 |
| E | .1969 | .2087 | .2205 | 5.00 | 5.30 | 5.60 |
| e | 0.02559 BSC | | | 0.65 BSC | | |
| H | .2913 | .3071 | .3228 | 7.40 | 7.80 | 8.20 |
| L | .02165 | .02953 | 0.037 | 0.55 | 0.75 | 0.95 |
| a | 0º | - | 8º | 0º | - | 8º |
| | | | | | | |

## 24 Pin SOIC Outline Dimensions

| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .09252 | - | .1043 | 2.35 | - | 2.65 |
| $A_1$ | .003937 | - | .01181 | .10 | - | .30 |
| A2 | .08858 | - | .09252 | 2.250 | - | 2.350 |
| B | .01299 | - | .02008 | .33 | - | .51 |
| C | .009055 | - | .01260 | .23 | - | .32 |
| D | .5984 | - | .6142 | 15.20 | - | 15.60 |
| E | .2913 | - | .2992 | 7.40 | - | 7.60 |
| e | 0.050 BSC | | | 1.27 BSC | | |
| H | .3937 | - | .4193 | 10.00 | - | 10.65 |
| L | .01575 | - | .050 | .40 | - | 1.27 |
| a | 0º | - | 8º | 0º | - | 8º |

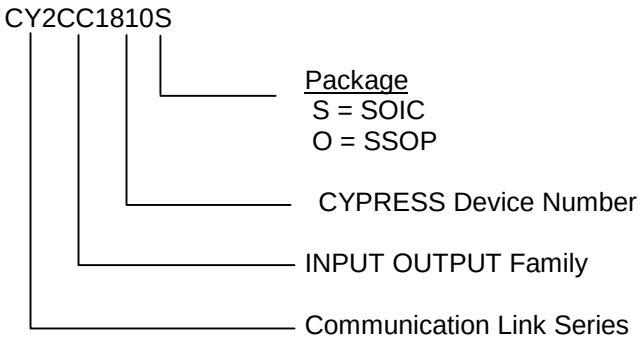
## ComL™ SERIES
## Ordering Information

| Part Number | Package Type |
|---|---|
| CY2CC1810S | 24 Pin SOIC |
| CY2CC1810O | 24 Pin SSOP |

Note: the ordering part number is formed by a combination of device number, package and screening as shown below.

Marking: Example:

CY2CC1810 S
Date Code, A
Lot #

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| **Document Title:** CY2CC2920 1:10 Signal Fanout Buffer w/ Output Enable<br>**Document Number:** 38-07055 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 107080 | 06/07/01 | IKA | Convert from IMI to Cypress |