CY2CC810

1:10 Clock Fanout Buffer

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Product Features

- Low Voltage Operation
  VDD range from 2.5 to 3.3V
- 1:10 Fanout
- Drives either a 50 ohm or 75 ohm load
- Low input capacitance
- Low output skew
- Low propagation delay
  Typical (tpd<4ns)
- High Speed Operation >500MHz
- Industrial Operation at 0°C to +85°C
- Packages available include: SOIC/SSOP

Product Description

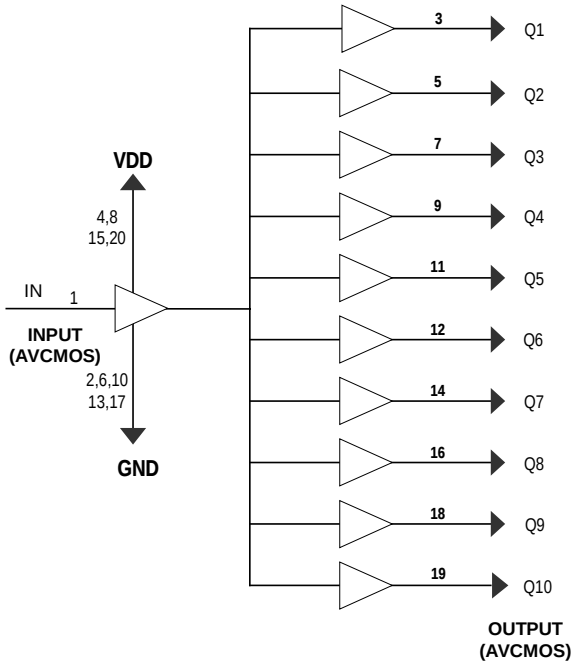
The CYPRESS series of network circuits are produced using advanced 0.35 micron CMOS technology, achieving the industries fastest logic and buffers.

The CYPRESS CY2CC810 fanout buffer features one input and ten outputs.

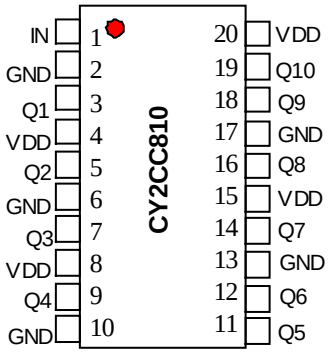
Designed for Data Communications clock management applications, the large fanout from a single input reduces loading on the input clock.

AVCMOS type outputs dynamically adjust for variable impedance matching and eliminate the need for series damping resistors and reduce noise overall.

Block Diagram



Pin Configuration



20 pin SOIC/SSOP

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Pin Description

Pin Number	Pin Name	Description
1	IN	Input
2,6,10,13,17	GND	Ground
4,8,15,20	V_{DD}	Power Supply
3,5,7,9,11,12,14,16,18,19	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8,Q9,Q10	Output

Absolute Maximum Ratings:

Storage Temperature	-65°C to 150°C
Ambient Temperature	0°C to +85°C
Supply Voltage to Ground Potential (Inputs and Vcc only)	-0.5V to 4.6V
Supply Voltage to Ground Potential (outputs only)	-0.5V to V_{DD}+0.5V
DC Input Voltage	-0.5V to V_{DD}+0.5V
DC Output Voltage	-0.5V to V_{DD}+0.5V
Power Dissipation	0.75W

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85, VDD=3.3V +/-10%							
Parameter	**Description**	**Test Conditions**		**Min**	**Typ**	**Max**	**Units**
V_{OH}	Output High Voltage	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}	IOH= -12mA	2.3	3.3		V
V_{OL}	Output Low Voltage	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}	IOL = 12mA		0.2	0.5	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD}=Max	V_{IN}=2.7V			1	uA
I_{IL}	Input Low Current	V_{DD}=Max	V_{IN}=0.5V			-1	uA
I_I	Input High Current	V_{DD}=Max., V_{IN}=V_{DD}(Max)				20	uA
V_{IK}	Clamp Diode Voltage	V_{DD}=Min., I_{IN} = -18mA			-0.7	-1.2	V
I_{OK}	Continuous Clamp Current	V_{DD}=Max, V_{OUT} = GND				-50	mA
O_{OFF}	Power Down Disable	V_{DD} = GND, V_{OUT} =<4.5V				100	uA
V_H	Input Hysteresis				80		mV

D.C. Electrical Characteristics: @ 2.5V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C VDD=2.5 +/-10%							
Parameter	**Description**	**Test Conditions**		**Min.**	**Typ**	**Max**	**Units**
V_{OH}	Output High Voltage	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}	I_{OH}= -7mA	1.80			V
			I_{OH}= -15.2mA	1.60			V
V_{OL}	Output Low Voltage	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}	I_{OL}= 15.2mA			0.65	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		1.60			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.9	V
I_{IH}	Input High Current	V_{DD}=Max	V_{IN}=2.4V			1	uA
I_{IL}	Input Low Current	V_{DD}=Max	V_{IN}=0.5V			-1	uA
I_I	Input High Current	V_{DD}=Max., V_{IN}=V_{DD}(Max)				20	uA
V_{IK}	Clamp Diode Voltage	V_{DD}=Min., I_{IN} = -18mA			-0.7	-1.2	V
I_{OK}	Continuous Clamp Current	V_{DD}=Max, V_{OUT} = GND				-50	mA
O_{OFF}	Power Down Disable	V_{DD} = GND, V_{OUT} =<4.5V				100	uA
V_H	Input Hysteresis				80		mV

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Capacitance:

Parameter	Description	Test Conditions	Typ	Max	Units
Cin	Input Capacitance	Vin = 0V	2.5	-	pF
Cout	Output Capacitance	Vout = 0V	6.5	-	pF

Power Supply Characteristics:

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔI_{CC}	Delta Quiescent Power Supply Current LVTTL/LVCMOS	| value | = (V_{DD} = Max) – (V_{DD} = V_{DD}- 0.6V) with Input High	-	3	50	uA
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open	-	2.2	2.5	mA/MHz
I_C	Total Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL=100MHZ	-	230	265	mA

High Frequency Parametrics :

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Fmax	Maximum frequency VDD = 3.3V	50% duty cycle tW(50-50) Standard Load Circuit.	-	-	160	MHz
		50% duty cycle tW(50-50) The “point to point load circuit”			650	
Fmax(20)	Maximum frequency VDD = 3.3 V	20% duty cycle tW(20-80) The “point to point load circuit” Vin = 3.0V / 0.0V Vout = 2.3V / 0.4V	-	-	250	MHz
	Maximum frequency VDD = 2.5 V	The “point to point load circuit” Vin = 2.4 / 0.0V Vout = 1.7V / 0.7V	-	-	200	MHz
tW	Minimum pulse VDD = 3.3 V	The “point to point load circuit” Vin = 3.0V / 0.0V F= 100MHz Vout = 2.0V / 0.8V	1	-	-	ns
	Minimum pulse VDD = 2.5 V	The “point to point load circuit” Vin = 2.4 / 0.0V F= 100MHz Vout = 1.7V / 0.7V	1			

AC Switching Characteristics @ 3.3

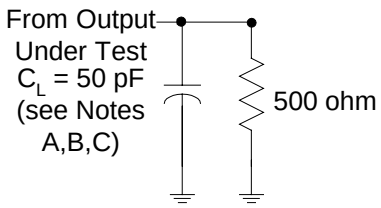
AC Switching Characteristics Over Operating Range VDD = 3.3V +/-5%, Temperature = 0°C to +85°C						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
tPLH	Propagation Delay – Low to High			3.8		nS
tPHL	Propagation Delay – High to Low			3.8		nS
tR	Output Rise Time			0.8		V/nS
tF	Output Fall Time			0.8		V/nS
tSK(0)	Output Skew: Skew between outputs of the same package (in phase)		-	-	0.2	nS
tSK(p)	Pulse Skew: Skew between opposite transitions of the same output (tPHL – tPLH)		-	-	0.2	nS
tSK(t)	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.		-	-	0.3	nS

AC Switching Characteristics @ 2.5

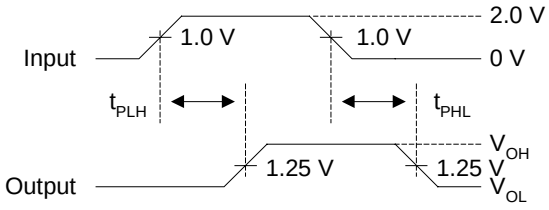
AC Switching Characteristics Over Operating Range VDD = 2.5V +/-5%, Temperature = 0°C to +85°C						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
tPLH	Propagation Delay – Low to High			3.8		nS
tPHL	Propagation Delay – High to Low			3.8		nS
tR	Output Rise Time			0.8		V/nS
tF	Output Fall Time			0.8		V/nS
tSK(0)	Output Skew: Skew between outputs of the same package (in phase)		-	-	0.2	nS
tSK(p)	Pulse Skew: Skew between opposite transitions of the same output (tPHL – tPLH)		-	-	0.2	nS
tSK(t)	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.		-	-	0.3	nS

Parameter Measurement Information

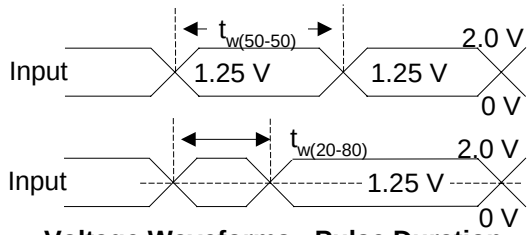
VDD @ 2.5



Load Circuit



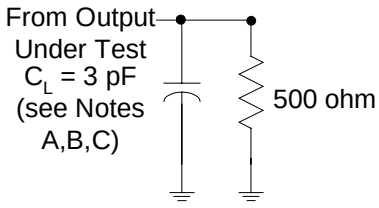
Voltage Waveforms
Propagation Delay Times



Voltage Waveforms - Pulse Duration

Notes:

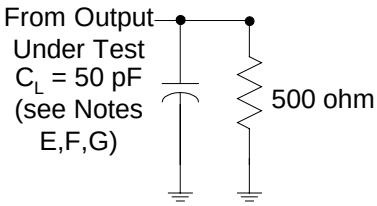
A. CL includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz, Z_O = 50 Ω, t_r < 2.5 nS, t_f < 2.5nS.
C. The outputs are measured one at a time with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.



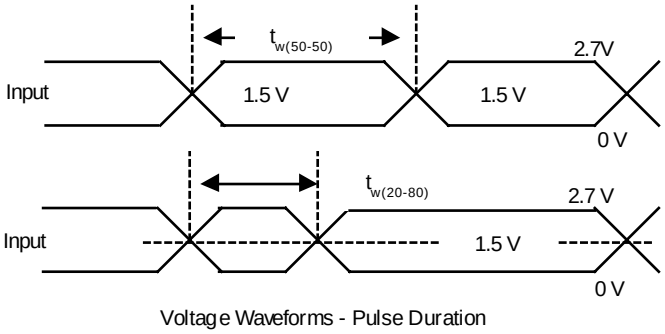
Point to Point Load Circuit

Parameter Measurement Information

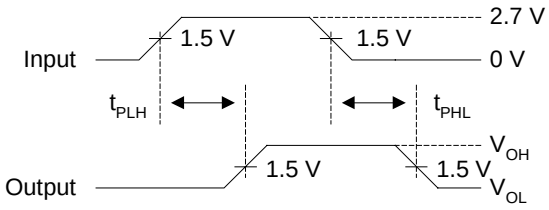
VDD @ 3.3



Load Circuit



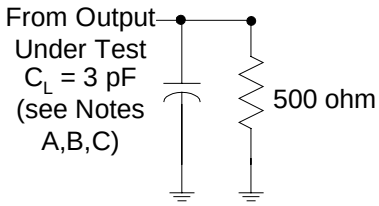
Voltage Waveforms - Pulse Duration



Voltage Waveforms
Propagation Delay Times

Notes:

E. CL includes probe and jig capacitance.
F. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, Z_O = 50 Ω, t_r < 2.5 nS, t_f < 2.5nS.
G. The outputs are measured one at a time with one transition per measurement.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.



Point to Point Load Circuit

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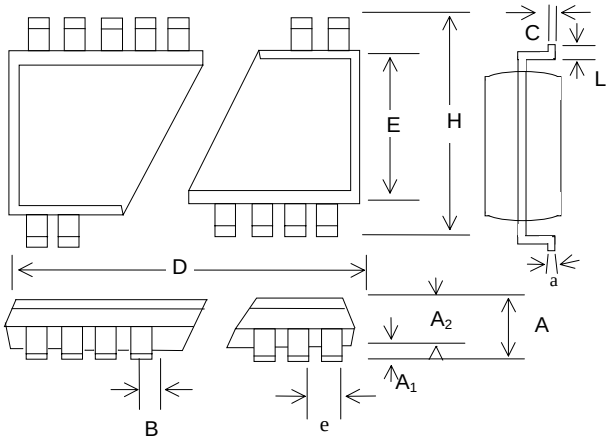
Package Drawing and Dimensions



20 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.079	-	-	2.0
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.065	0.069	0.073	1.65	1.75	1.85
B	0.009	-	0.015	0.22	-	0.38
C	0.004	-	0.010	0.09	-	0.25
D	0.272	0.283	0.295	6.90	7.20	7.50
E	0.197	0.209	0.220	5.00	5.30	5.60
e	0.026 BSC			0.65 BSC		
H	0.291	0.307	0.323	7.40	7.80	8.20
L	0.022	0.030	0.037	0.55	0.75	0.95
a	0º	-	8º	0º	-	8º

20 Pin SOIC Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	.09252	-	.1043	2.35	-	2.65
A_1	.003937	-	.01181	.10	-	.30
A2	.08858	-	.09252	2.250	-	2.350
B	.01299	-	.02008	.33	-	.51
C	.009055	-	.01260	.23	-	.32
D	.4961	-	.5118	12.60	-	13.00
E	.2913	-	.2992	7.40	-	7.60
e	0.050 BSC			1.27 BSC		
H	.3937	-	.4193	10.00	-	10.65
L	.01575	-	.050	.40	-	1.27
a	0º	-	8º	0º	-	8º

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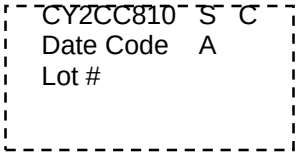
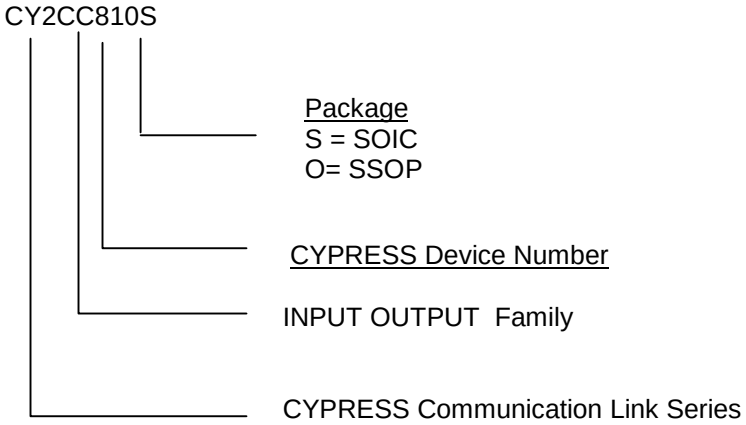
Ordering Information

Part Number	Package Type
CY2CC810S	20 Pin SOIC
CY2CC810O	20 Pin SSOP

Note: the ordering part number is formed by a combination of device number, package and screening as shown below.

Marking: Example:





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Document Title: CY2CC810 1:10 Clock Fanout Buffer **Document Number:** 38-07056				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107081	06/07/01	IKA	Convert from IMI to Cypress