ADVANCED

CY2DP818

1:8 Clock Fanout Buffer

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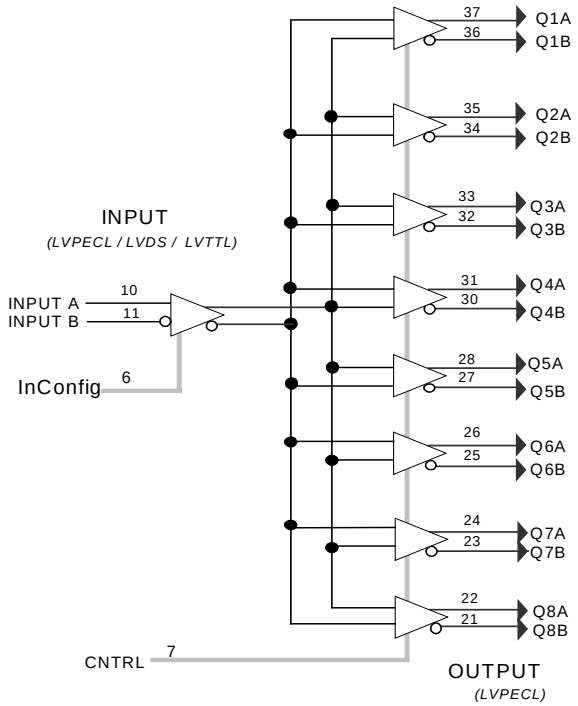
Product Features

- Low Voltage Operation
  V_{DD} = 3.3V
- 1:8 Fanout
- Single input configurable for LVDS, LVPECL or LVTTL
- 8 pair of LVPECL outputs
- Drives either a 50 ohm or 100 ohm load (Selectable)
- Low input capacitance
- Low output skew
- Low propagation delay
  Typical (tpd<4ns)
- Fmax=>400MHz
- Industrial Operation at 0°C to +85°C
- Packages available include: TSSOP

Block Diagram



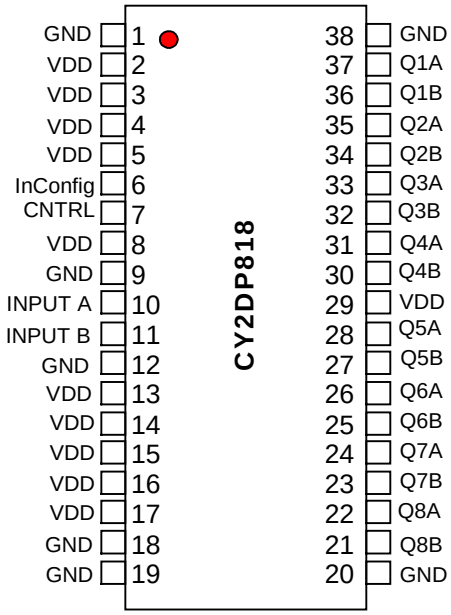
Product Description

This CYPRESS series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industries fastest logic.

The CYPRESS CY2DP818 fanout buffer features a single LVDS or a single ended LVTTL compatible input and 8 LVPECL output pairs.

Designed for Data Communications clock management applications, the large fanout from a single input reduces loading on the input clock.
The DP818 is ideal for both level translations from single ended to LVPECL and/or for the distribution of LVPECL-based clock signals.
The CYPRESS CY2DP818 has configurable input and output functions. The input can be selectable for LVCMOS/LVTTL, LVPECL or LVDS signal.

Pin Configuration



38 pin TSSOP

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Pin Description

Pin Number	Pin Name	Pin Interface Standard	Description
1, 6,9,12, 18,19,20,38	GND	POWER	Ground
2,3,4,5,8, 13 14,15,16,17,29	VDD	POWER	Power Supply
10,11	Input A, Input B(#)	Default LVPECL / InConfig : LDVS / Optional LVTTL single pin.	Differential input pair
37, 36,35,34, 33,32,31, 30, 28,27,26,25, 24,23,22,21	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B, Q5A, Q5B, Q6A, Q6B, Q7A, Q7B, Q8A, Q8B	LVPECL	Differential Outputs
6	InConfig	LVTTL / LVCMOS	Converts inputs from the default LVPECL (logic = 0) To LDVS (logic = 1) **See Fig.7 for additional Information**
7	CNTRL	LVTTL / LVCMOS	Converts into a High-speed driver. Logic = 0 = 100 ohm Logic = 1 = 50 ohm **See Fig. 7 for additional Information**

Absolute Maximum Ratings:

Storage Temperature	-65°C to 150°C
Ambient Temperature	0°C to +85°C
Supply Voltage to Ground Potential (Inputs and Vcc only)	-0.3V to 4.6V
Supply Voltage to Ground Potential (outputs and D/O only)	-0.3V to V_{DD}+0.3V
DC Input Voltage	-0.3V to V_{DD}+0.3V
DC Output Voltage	-0.3V to V_{DD}+3.9V
Power Dissipation	0.75W

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open	-	0.4	0.5	mA/MHz
I_C	Total Power Supply Current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL=100MHz	-	20	50	mA

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LVDS Input D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%

Parameter	Description	Test Conditions		Min.	Typ.	Max	Units
$\|V_{ID}\|$	Magnitude of Differential Input Voltage			100		600	mV
$\|V_{IC}\|$	Common-Mode of Differential Input Voltage$\|V_{ID}\|$ (min&max)			IVIDI /2		2.4-(IVIDI /2)	V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD}=Max	$V_{IN}=V_{DD}$		+/-10	+/-20	uA
I_{IL}	Input Low Current	V_{DD}=Max	$V_{IN}=V_{SS}$		+/-10	+/-20	uA
I_I	Input High Current	V_{DD}=Max, $V_{IN}=V_{DD}$(max)				+/-20	uA

LVPECL Input D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%

Parameter	Description	Test Conditions		Min.	Typ	Max	Units
$\|V_{ID}\|$	Differential input voltage p-p	Guaranteed Logic High Level		400		2600	mV
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2.15		2.4	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level		1.5		1.8	V
I_{IH}	Input High Current	V_{DD}=Max	$V_{IN}=V_{DD}$		+/-10	+/-20	uA
I_{IL}	Input Low Current	V_{DD}=Max	$V_{IN}=V_{SS}$		+/-10	+/-20	uA
I_I	Input High Current	V_{DD}=Max., $V_{IN}=V_{DD}$(Max)				+/-20	uA

LVPECL Output D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0°C to +85°C, VDD=3.3V +/-5%

Parameter	Description	Test Conditions		Min.	Typ	Max	Units
$\|V_{OD}\|$	Driver Differential Output voltage p-p	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}	RL=75 ohm	1100		2200	mV
			RL=50 ohm	1100		2200	mV
$\|V_{OC}\|$	Driver common-mode p-p	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}	RL=75 ohm		2100		mV
Risetime	Differential 20% to 80%	CL-10pF RL & CL to GND	RL=75 ohm	600		300	pS
Falltime				600		300	pS
V_{OH}	Output High Voltage	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}	I_{OH} = -12mA	1.8		2.4	V
V_{OL}	Output Low Voltage	V_{DD}=Min., $V_{IN}=V_{IH}$ or V_{IL}		1.2		1.7	V
I_{OS}	Short Circuit Current	V_{DD}=Max, V_{OUT} = GND				-50	mA

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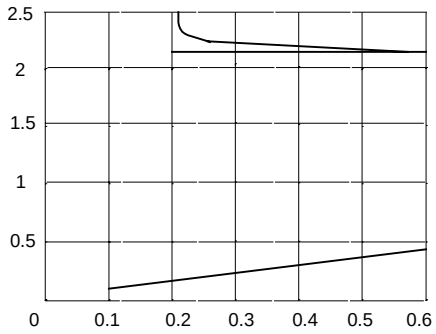
AC Switching Characteristics @ 3.3

AC Switching Characteristics Over Operating Range VDD = 3.3V +/-5%, Temperature = 0°C to +85°C						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ.**	**Max**	**Units**
TPLH	Propagation Delay – Low to High		1.0	2.5	3.5	nS
TPHL	Propagation Delay – High to Low		1.0	2.5	3.5	nS
TSK(0)	Output Skew: Skew between outputs of the same package (in phase)		-	-	0.2	nS
TSK(p)	Pulse Skew: Skew between opposite transitions of the same output (TPHL – TPLH)		-	-	0.3	nS
TSK(t)	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.		-	-	1.6	nS

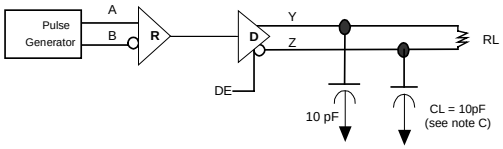
High Frequency Parametrics :

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Fmax	Maximum frequency VDD = 3.3V	50% duty cycle tW(50-50) Standard Load Circuit.	-	-	400	MHz
		50% duty cycle tW(50-50) The “point to point load circuit”	-	-	400	
Fmax(20)	Maximum frequency VDD = 3.3 V	20% duty cycle tW(20-80) The “point to point load circuit” Vin = 3.0V / 0.0V Vout = 2.3V / 0.4V	-	-	TBD	MHz
tW	Minimum pulse VDD = 3.3 V	The “point to point load circuit” Vin = 3.0V / 0.0V F= 100MHz Vout = 2.0V / 0.8V	TBD	-	-	nS

Common - Mode Input Voltage vs. DIfferential Voltage



Test Circuit & Voltage Definitions for the Differential Output Signal



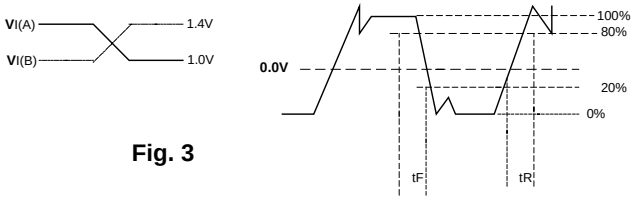


Fig. 3

Differential Receiver to Driver Propagation Delay and Driver Transition Time

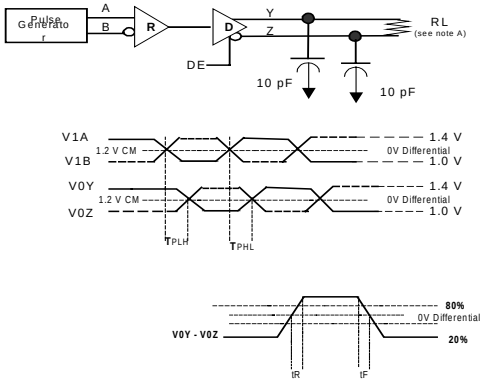


Fig.5

Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage

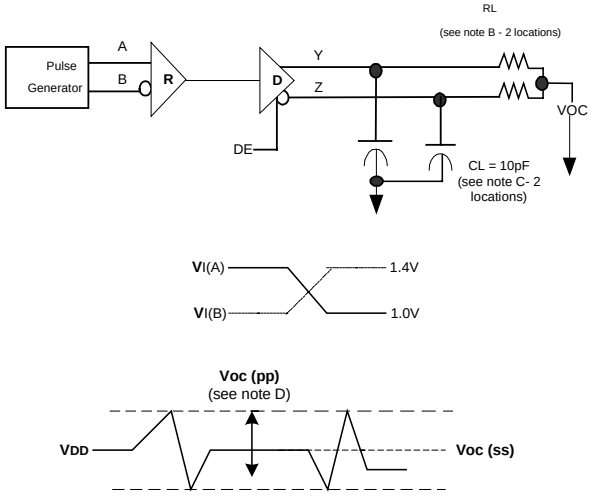


Fig. 4

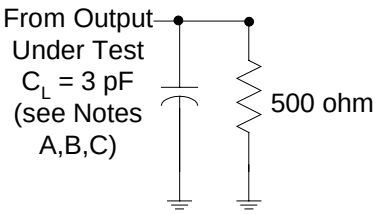
Notes:

A: All input pulses are supplied by a frequency Generator With the following characteristics:
- TR & tF ≤ 1nS
- Pulse re rate = 50 Mpps
- Pulse width = 10±0.2nS

B: RL-100 ohm / 50ohm±1%

C: CL includes instrumentation and fixture capacitance within 6mm of the DUT

D: VOC measurement requires equipment with a 3dB Bandwidth of at least 300MHz.



Point to Point Load Circuit
Fig 5A

Test Circuit & Voltage Definitions for the
Driver Common-Mode Output Voltage

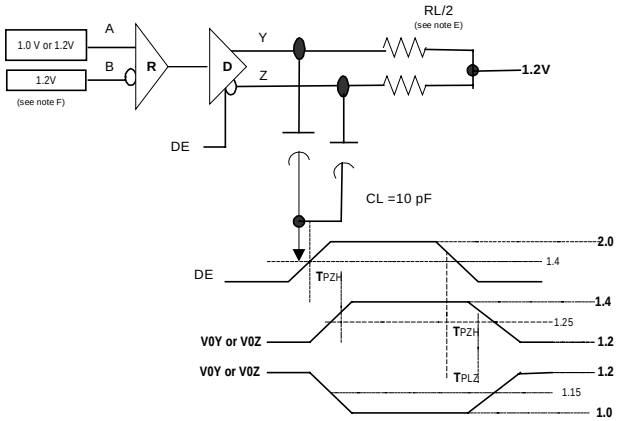
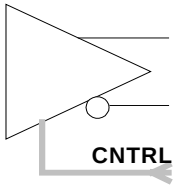


Fig. 6

Notes:

E: RL-100 ohm/50ohm±1%
F: All input pulses are supplied by a frequency Generator
With the following characteristics:
TR & tF ≤ 1nS
Pulse re rate = 50 Mpps
Pulse width = 10±0.2nS



(see Note I)

0	Standard	100 Ohms	'Vo = Vo
		50 Ohms	'Vo = 1/2 Vo
1	Hi Drive B	100 Ohms	'Vo = 2 Vo
		50 Ohms	'Vo = Vo

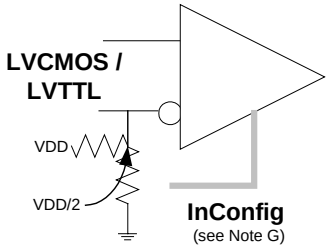
I/O Configuration Options

Input Configurations

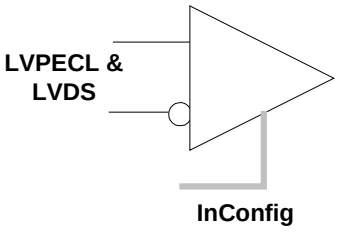
G. LVCMOS / LVTTL single ended input.
H. LVPECL or LVDS differential input.

Output Configuration:

I. Standard 100 ohm output impedance
High Drive 50 ohm output impedance



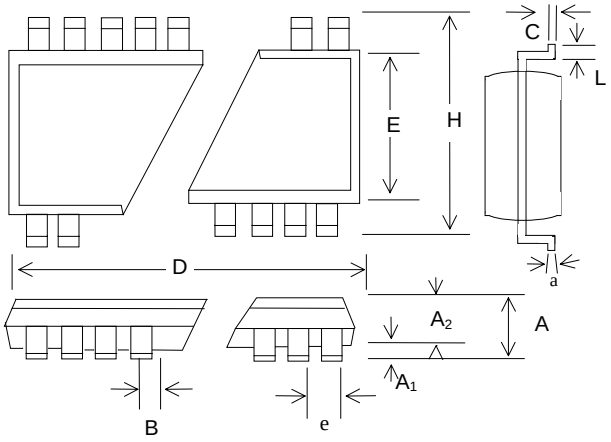
0	LVPECL



(see Note **H**)

0	LVPECL
1	LVDS

Package Drawing and Dimensions



38 Pin TSSOP Outline Dimensions

JEDEC MO-153e Variation: BD

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D				9.60	9.70	9.80
E				4.30	4.40	4.50
e	0.01969 BSC			0.50 BSC		
H	0.2510 BSC			6.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

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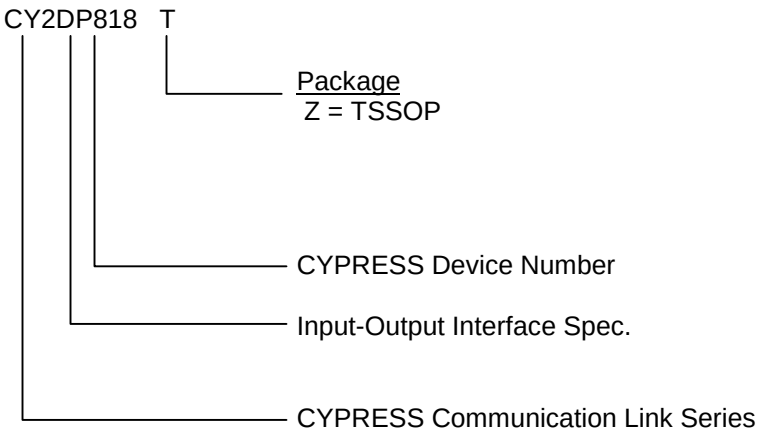
Ordering Information

Part Number	Package Type
CY2DP818Z	38 Pin TSSOP

Note: the ordering part number is formed by a combination of device number, package and screening as shown below.

Marking: Example:

CYPRESS
CY2DP818
Date Code, Lot #



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Document Title: CY2DP818 1:8 Clock Fanout Buffer **Document Number:** 38-07061				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107086	06/07/01	IKA	Convert from IMI to Cypress