ADVANCED

CY2DP8520

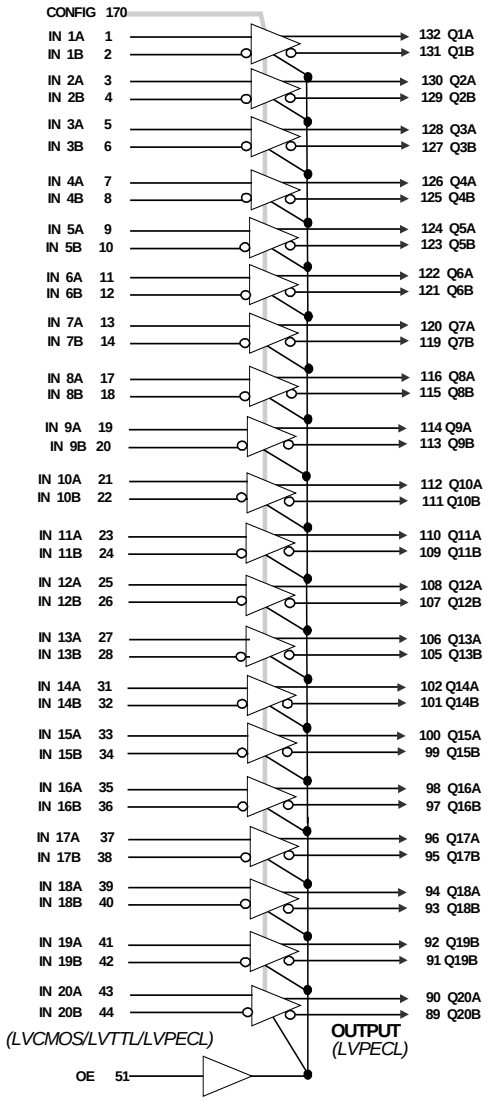
20 Bit Buffer/ Converter w/ Output Enable(s)

ComL™ SERIES

Product Features

- Low Voltage Operation
  V_{DD} range from 2.5 to 3.3V
- 20 input's configurable for LVPECL/ LVTTL/LVCMOS
- 20 pairs LVPECL output
- Drives 50/100 ohm load
- Low output skew

Block Diagram



Product Features (Cont.)

- Low input capacitance
- Low propagation delay
  Typical (tpd<4ns)
- Fmax =>400MHz
- Industrial Operation at 0°C to +85°C
- Packages available include: LPQFP

Product Description

The CYPRESS series of network circuits are produced using advanced 0.35 micron CMOS technology, achieving the industries fastest logic.

The CYPRESS CY2DP8520 buffer/converter features a 20 independent LVCMOS-LVPECL-LVDS compatible inputs and 20 LVPECL output pairs. The DP8520 is ideal for both level translations from single ended to LVPECL and/or for the distribution of LVDS-based signals. The CYPRESS CY2DP8520 has configurable input. The input can be selectable for LVPECL/LVTTL-LVCMOS or LVDS using the **CONFIG** signal.

Pin Configuration

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CY2DP8520

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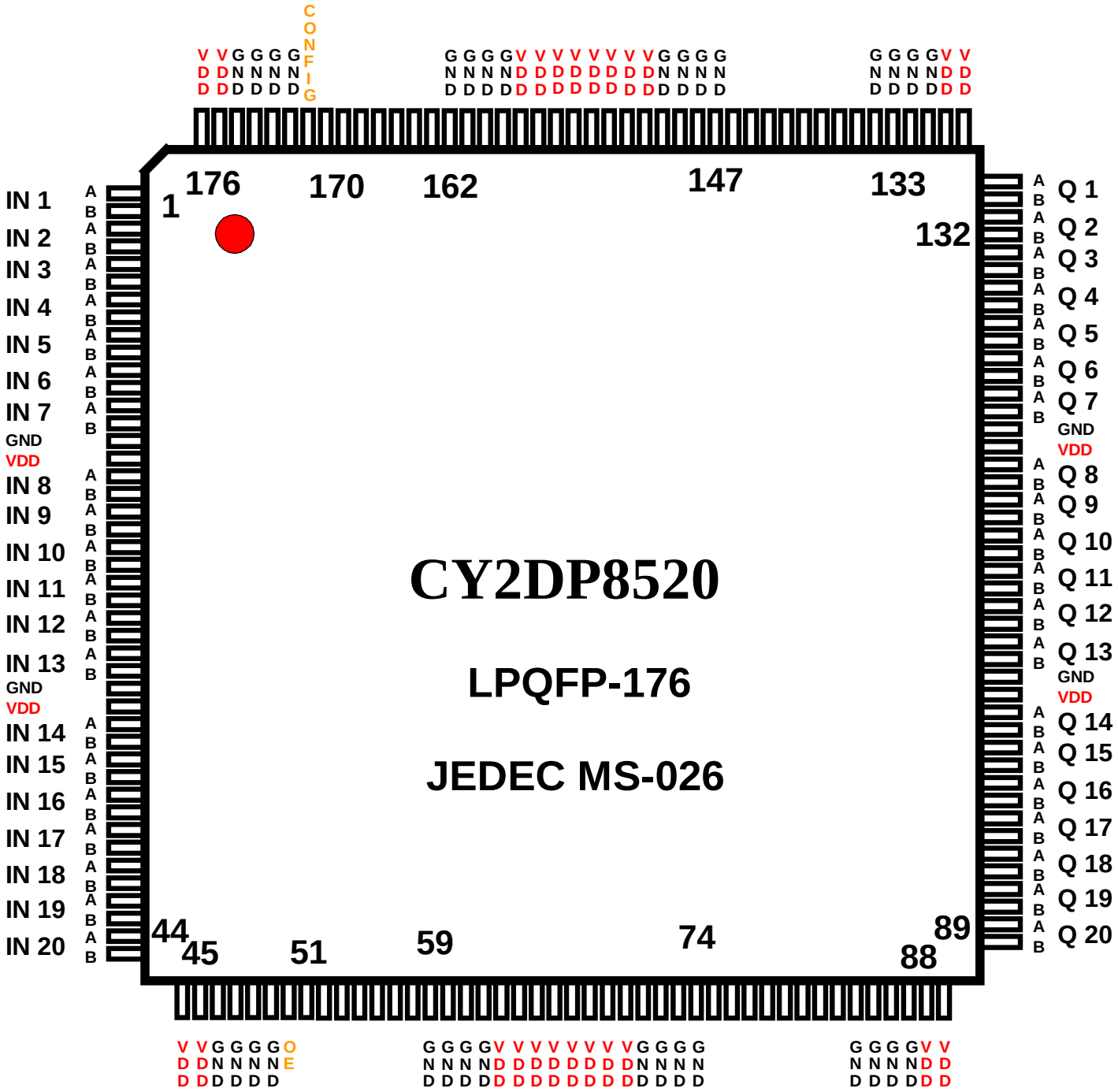
Detailed Pin Configuration



Pin Description

Pin Number [Pin #, Pin #]	Pin Name	Class of I/O	Description
1[1,2] 2[3,4] 3[5,6] 4[7,8] 5[9,10] 6[11,12] 7[13,14] **8[17,18]** 9[19,20] 10[21,22] 11[23,24] 12[25,26] 13[27,28] **14[31,32]** 15[33,34] 16[35,36] 17[37,38] 18[39,40] 19[41,42] 20[43,44]	**IN *x* [*A* , *B*]**	LVCMOS / LVTTL / LVPECL	Differential inputs IN (**1..20)[pinA,pinB]** **B is the inverted input** The **BOLD** **pin number[pinA,pinB]** Indicates a shift of sequence.
1[132,131] 2[130,129] 3[128,127] 4[126,125] 5[124,123] 6[122,121] 7[120,119] **8[116,115]** 9[114,113] 10[112,111] 11[110,109] 12[108,107] 13[106,105] **14[102,101]** 15[100,99] 16[98,97] 17[96,95] 18[94,93] 19[92,91] 20[90,89]	**Q *x* [*A,B*]**	LVPECL	Output pins in LVPECL **B is the inverted output** The **BOLD** **pin number[pinA,pinB]** Indicates a shift of sequence.
170	CONFIG	LVCMOS / LVTTL	
51	OE	LVCMOS / LVTTL	
16,30, 45,46,63,64,65,66,67,68,69,70,87,88, 103,117, 133,134,151,152,153,154,155,156,157,158,175,176	VDD	Power	Voltage : 2.5V to 3.3V range
15,29, 47,48,49,50,59,60,61,62,71,72,73,74,83,84,85,86, 104,118, 135,136,137,138,147,148,149,150,159,160,161,162, 171,172,173,174	GND	Ground	Ground

Absolute Maximum Ratings:

Storage Temperature	-65°C to 150°C
Ambient Temperature	0°C to +85°C
Supply Voltage to Ground Potential (Inputs and V_{DD} only)	-0.3V to 4.6V
Supply Voltage to Ground Potential (outputs only)	-0.3V to V_{DD}+0.3V
DC Input Voltage	-0.3V to V_{DD} +0.3V
DC Output Voltage	-0.3V to V_{DD} +3.9V
Power Dissipation	0.75W

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

High Frequency Parametrics :

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Fmax	Maximum frequency VDD = 3.3V	50% duty cycle tW(50-50) Standard Load Circuit	-	200	TBD	MHz
		50% duty cycle tW(50-50) The "point to point load circuit"		350	400	
Fmax(20)	Maximum frequency VDD = 3.3 V	20% duty cycle tW(20-80) The "point to point load circuit" Vin = 3.0V / 0.0V Vout = 2.3V / 0.4V	-	-	TBD	MHz
	Maximum frequency VDD = 2.5 V	The "point to point load circuit" Vin = 2.4 / 0.0V Vout = 1.7V / 0.7V			TBD	
tW	Minimum pulse VDD = 3.3 V	The "point to point load circuit" Vin = 3.0V / 0.0V F = 100MHz Vout = 2.0V / 0.8V	2	-	-	nS
	Minimum pulse VDD = 2.5 V	The "point to point load circuit" Vin = 2.4 / 0.0V F = 100MHz Vout = 1.7V / 0.7V	1			

LVDS Input D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0℃ to +85℃, VDD=3.3V +/-5%							
Parameter	**Description**	**Test Conditions**		**Min.**	**Typ.**	**Max**	**Units**
I V_{ID} I	Magnitude of Differential Input Voltage			100		600	mV
I V_{IC} I	Common-Mode of Differential Input VoltageIV_{ID}I (min&max)			IVIDI /2	2.4-(IVIDI /2)		V
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD}=Max	V_{IN}=V_{DD}		+/-1	+/-2.5	uA
I_{IL}	Input Low Current	V_{DD}=Max	V_{IN}=V_{SS}		+/-1	+/-2.5	uA
I_I	Input High Current	V_{DD}=Max, V_{IN}=V_{DD}(max)				+/-2.5	uA

LVPECL Input D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0℃ to +85℃, VDD=3.3V +/-5%							
Parameter	**Description**	**Test Conditions**		**Min.**	**Typ**	**Max**	**Units**
I V_{ID} I	Differential input voltage p-p	Guaranteed Logic High Level		400		2400	mV
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2.15		2.4	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level		1.5		1.8	V
I_{IH}	Input High Current	V_{DD}=Max	V_{IN}=V_{DD}		+/-1	+/-2.5	uA
I_{IL}	Input Low Current	V_{DD}=Max	V_{IN}=V_{SS}		+/-1	+/-2.5	uA
I_I	Input High Current	V_{DD}=Max., V_{IN}=V_{DD}(Max)				+/-2.5	uA

LVPECL Output D.C. Electrical Characteristics: @ 3.3V

D.C. Electrical Characteristics (Over the Operating Range , TA =0℃ to +85℃, VDD=3.3V +/-5%							
Parameter	**Description**	**Test Conditions**		**Min.**	**Typ**	**Max**	**Units**
I V_{OD} I	Driver Differential Output voltage p-p	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}	RL=75 ohm	1100		2200	mV
			RL=50 ohm	1100		2200	mV
I V_{OC} I	Driver common-mode p-p	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}	RL=75 ohm		2100		mV
Risetime	Differential 20% to 80%	CL-10pF RL & CL to GND	RL=75 ohm	600		300	pS
Falltime				600		300	pS
V_{OH}	Output High Voltage	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}	I_{OH} = -12mA	1.8		2.4	V
V_{OL}	Output Low Voltage	V_{DD}=Min., V_{IN}=V_{IH} or V_{IL}		1.2		1.7	V
I_{OS}	Short Circuit Current	V_{DD}=Max, V_{OUT} = GND				-50	mA

Power Supply Characteristics

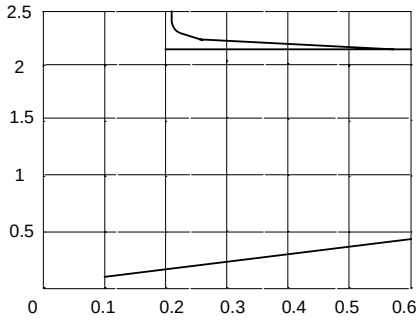
Symbol	Parameter	Test Conditions		Min.	Typ	Max	Unit
ΔICC	Quiescent Power Supply Current LVTTL/LVCMOS Inputs High	V_{DD} = Max V_{IN} = V_{DD}-0.6V		-	3	50	uA
ICCD	Dynamic Power Supply Current	V_{DD} = Max		-	0.4	0.5	mA/mHz
		Input toggling 50% Duty	V_{IN} = V_{DD}				
		Cycle, Outputs Open	V_{IN} = GND				
IC	Total Power Supply Current	V_{DD} = Max	V_{IN} = V_{DD}	-	20	50	mA
		Input toggling 50% Duty	V_{IN} = GND				
		Cycle, Outputs Open	V_{IN} = V_{DD}-0.6V				
		fL=100MHz	V_{IN} = GND				

AC Switching Characteristics @ 3.3

AC Switching Characteristics Over Operating Range TA =0°C to +85°C, V_{DD}=3.3V +/-5%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TPLH	Propagation Delay – Low to High	Figure 5	1.0	2.5	3.5	nS
TPHL	Propagation Delay – High to Low		1.0	2.5	3.5	nS
TSK(0)	Output Skew: Skew between outputs of the same package (in phase)		-	-	0.2	nS
TSK(p)	Pulse Skew: Skew between opposite transitions of the same output (TPHL – TPLH)		-	-	0.3	nS
TSK(t)	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.		-	-	1.6	nS
t_{PZH} t_{PZL}	Output Enable (OE) Time From Tristate	OE to output	1.0		3.0	nS
t_{PHZ} t_{PLZ}	Output Enable (OE) Time To Tristate	OE to output	1.0		3.0	ns

Common - Mode Input Voltage vs. DIfferential Voltage



Test Circuit & Voltage Definitions for the Differential Output Signal

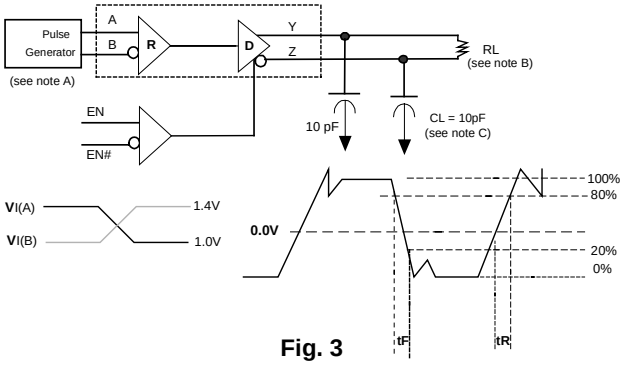
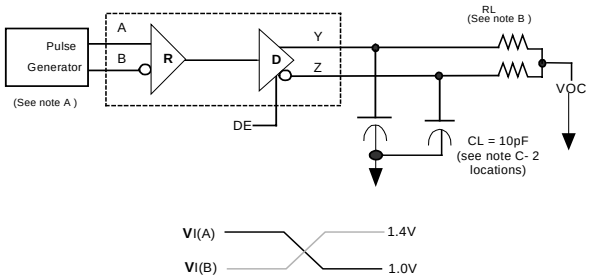


Fig. 3

Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage



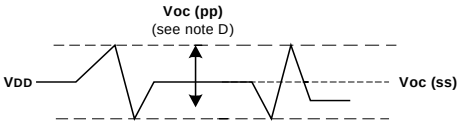


Fig. 4

Differential Receiver to Driver Propagation Delay and Driver Transition Time

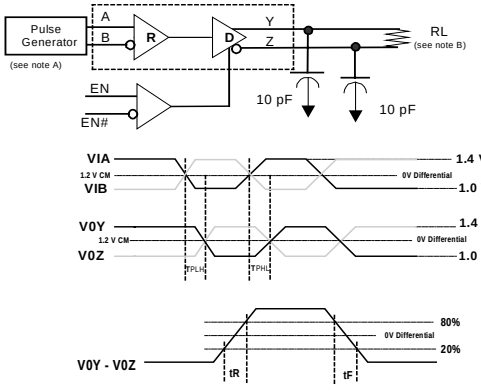


Fig.5

Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage

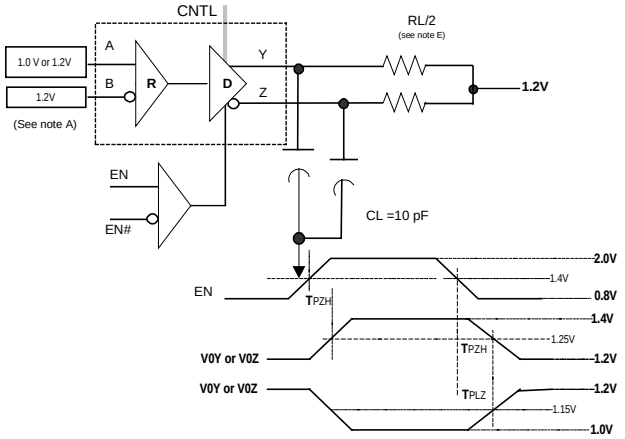
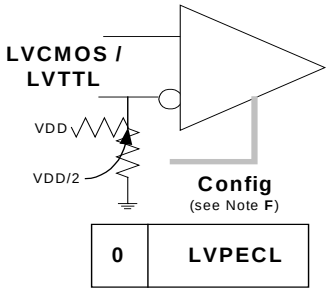
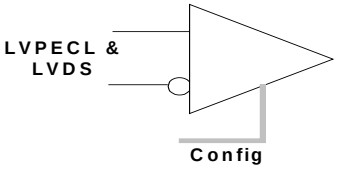


Fig. 6



0	LVPECL



0	LVPECL
1	LVDS

Notes:

A: All input pulses are supplied by a frequency Generator
With the following characteristics:
t_R & $t_F \leq$ 1nS
Pulse rep rate = 50 MppS
Pulse width = 10 ± 0.2nS

B: RL-100 ohm/50 ohm ±1%

C: CL includes instrumentation and fixture capacitance within 6mm of the DUT

D: VOC measurement requires equipment with a 3dB Bandwidth of at least 300MHz.

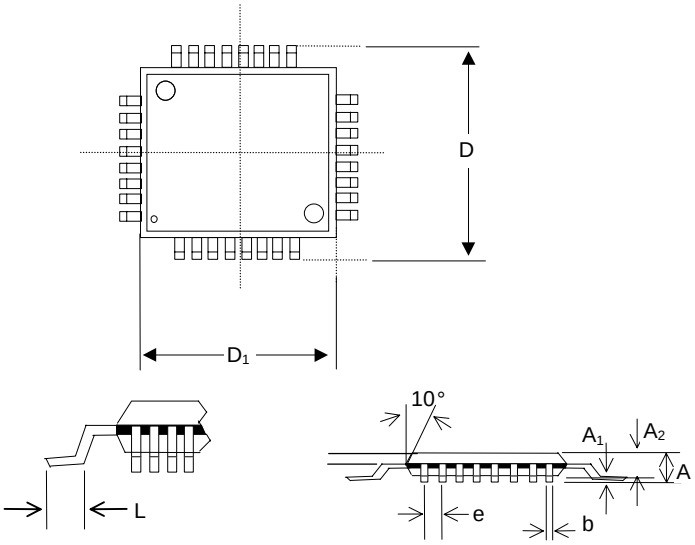
E: RL-100 ohm/50 ohm ±1% via CNTL

Input Configuration Options

Input Configurations:

F. LVCMOS / LVTTL single ended input.
G. LVPECL or LVDS differential input.

Package Drawing and Dimensions



176 Pin LPQFP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	**MIN**	**NOM**	**MAX**
A	-	-	.06299	**-**	**-**	**1.60**
A_1	.001969	-	.005906	**0.05**	**-**	**0.15**
A2	.05315	.05512	.05709	**1.35**	**1.40**	**1.45**
D	-	1.024	-	**-**	**26.00**	**-**
D_1	-	.9449	-	**-**	**24.00**	**-**
b	.006693	.008661	.01063	**0.17**	**0.22**	**0.27**
e	0.01969 BSC			**0.50 BSC**		
L	.01772	.02362	.02953	**0.45**	**0.60**	**0.75**

JEDEC MS-026 version: BGA, 176 PIN LPQFP

CY2DP8520

20 Bit Buffer/ Converter w/ Output Enable(s)

ComL™ SERIES

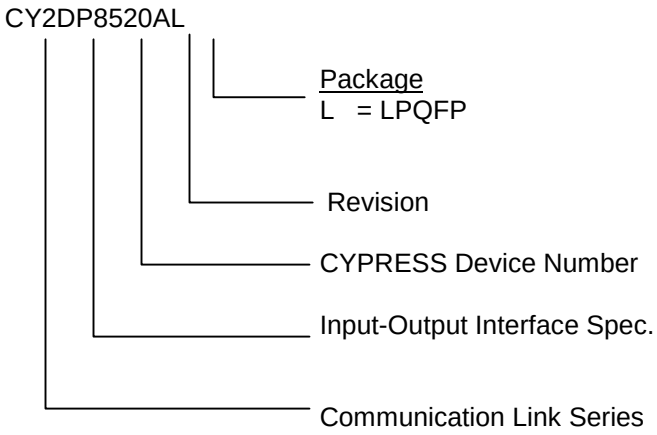
Ordering Information

Part Number	Package Type
CY2DP8520AL	176 Pin LPQFP

Note: the ordering part number is formed by a combination of device number, package and screening as shown below.

Marking: Example:

CYPRESS
CY2DP8520AL
Date Code, Lot #



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Document Title: CY2DP8520 20 Bit Buffer/ Converter w/ Output Enable(s) **Document Number:** 38-07062				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107087	06/07/01	IKA	Convert from IMI to Cypress