



SMBus System Clock Buffer

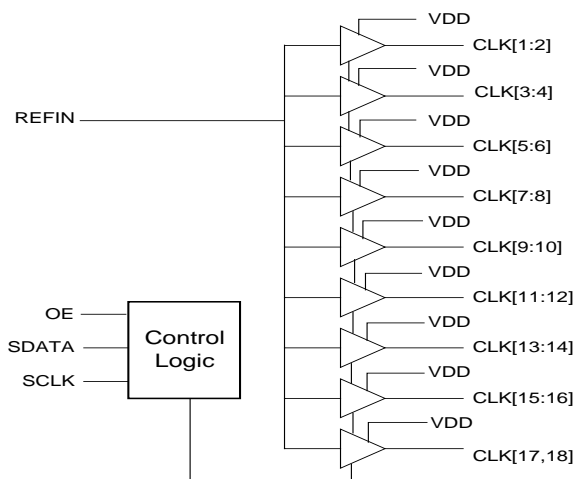
Product Features

- 18 output buffer for high clock fanout applications
- Each output can be internally disabled for EMI reduction
- VDD=3.3 volts for chip Vdd
- Output frequency range 10 Mhz to 100 Mhz
- < 250ps skew between output clocks
- 48-pin SSOP package
- Single Clock Enable pin for testability

Product Description

The SC680 is a high fanout system clock buffer. Its primary application is to create the large quantity of clocks needed to support a wide range of applications that requires those clock loads signal that are referenced to a single existing clock. Loads of up to 30 pF are supported. One of the chief applications of this component is where long traces are used to transport clocks from their generating devices to their loads. The creation of EMI and the degradation of waveform rise and fall times is greatly reduced by running a single reference clock trace to this device and then using it to regenerate the clock that drives shorter traces. Using these devices EMI is therefore minimized and board real estate is saved.

Block Diagram



Pin Configuration

IMISC680

| | | | |
|-------|----|----|--------|
| NC | 1 | 48 | NC |
| NC | 2 | 47 | NC |
| VDD | 3 | 46 | VDD |
| CLK1 | 4 | 45 | CLK18 |
| CLK2 | 5 | 44 | CLK17 |
| VSS | 6 | 43 | VSS |
| VDD | 7 | 42 | VDD |
| CLK3 | 8 | 41 | CLK16 |
| CLK4 | 9 | 40 | CLK15 |
| VSS | 10 | 39 | VSS |
| REFIN | 11 | 38 | OE |
| VDD | 12 | 37 | VDD |
| CLK5 | 13 | 36 | CLK14 |
| CLK6 | 14 | 35 | CLK13 |
| VSS | 15 | 34 | VSS |
| VDD | 16 | 33 | VDD |
| CLK7 | 17 | 32 | CLK12 |
| CLK8 | 18 | 31 | CLK11 |
| VSS | 19 | 30 | VSS |
| VDD | 20 | 29 | VDD |
| CLK9 | 21 | 28 | CLK10 |
| VSS | 22 | 27 | VSS |
| VDD | 23 | 26 | VSS |
| SDATA | 24 | 25 | SCLOCK |



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Pin Description

| PIN No. | Pin Name | PWR | I/O | TYPE | Description |
|-----------------------------------|------------|-----|-----|------|---|
| 11 | REFIN | VDD | I | PAD | This pin is connected to the input reference clock. This clock must be in the range of 10.0 to 100.0 Mhz. |
| 4,5 | CLK(1:2) | VDD | O | BUF1 | Low skew output clock |
| 8,9 | CLK(3:4) | VDD | O | BUF1 | Low skew output clock |
| 13, 14 | CLK(5:6) | VDD | O | BUF1 | Low skew output clock |
| 17, 18 | CLK(7:8) | VDD | O | BUF1 | Low skew output clock |
| 21, 28 | CLK(9:10) | VDD | O | BUF1 | Low skew output clock |
| 31, 32 | CLK(11:12) | VDD | O | BUF1 | Low skew output clock |
| 35, 36 | CLK(13:14) | VDD | O | BUF1 | Low skew output clock |
| 40, 41 | CLK(15:16) | VDD | O | BUF1 | Low skew output clock |
| 44, 45 | CLK(17:18) | VDD | O | BUF1 | Low skew output clock |
| 38 | OE | - | I | PAD | Buffer Output Enable pin. When driven to a logic low level this pin is used to place all output clocks (CLK1:18) in a tri state condition. This feature facilitates in production board level testing to be easily implemented for the clocks that this device produces. Has internal pull-up resistor. |
| 24 | SDATA | - | I/O | PAD | serial data of SMBus 2-wire control interface. Has internal pull-up resistor. |
| 25 | SDCLK | - | I | PAD | Serial clock of SMBus 2-wire control interface. Has internal pull-up resistor. |
| 6, 10, 15, 19, 22, 30, 34, 39, 43 | Vss | | PWR | - | Ground pins for clock output buffers. These pins must be returned to the same potential to reduce output clock skew. |
| 3, 7, 12, 16, 20, 33, 37, 42, 46 | Vdd | - | PWR | - | Power for output clock buffers. |
| 29, 23 | Vdd | - | PWR | - | Power for core logic. |
| 26, 27 | Vss | - | PWR | - | Ground supply pins for internal lcore logic pins. |



SMBus System Clock Buffer

2-Wire SMBus Control Interface

The 2-wire control interface implements a write only slave interface. The device cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledgement is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. Previously set control registers are retained.

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:

- 1) "**Command Code**" byte, and
- 2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte 2,) will be valid and acknowledged.



SMBus System Clock Buffer**Serial Control Registers (Cont.)****Byte 0: Function Select Register** (1 = enable, 0 = Stopped)

| Bit | @Pup | Pin# | Description |
|-----|------|------|-----------------------------------|
| 7 | 1 | 18 | CLK8 (Active = 1, Forced low = 0) |
| 6 | 1 | 17 | CLK7 (Active = 1, Forced low = 0) |
| 5 | 1 | 14 | CLK6 (Active = 1, Forced low = 0) |
| 4 | 1 | 13 | CLK5 (Active = 1, Forced low = 0) |
| 3 | 1 | 9 | CLK4 (Active = 1, Forced low = 0) |
| 2 | 1 | 8 | CLK3 (Active = 1, Forced low = 0) |
| 1 | 1 | 5 | CLK2 (Active = 1, Forced low = 0) |
| 0 | 1 | 4 | CLK1 (Active = 1, Forced low = 0) |

Byte 1: Clock Register (1 = enable, 0 = Stopped)

| Bit | @Pup | Pin# | Description |
|-----|------|------|------------------------------------|
| 7 | 1 | 45 | CLK18 (Active = 1, Forced low = 0) |
| 6 | 1 | 44 | CLK17 (Active = 1, Forced low = 0) |
| 5 | 1 | 41 | CLK16 (Active = 1, Forced low = 0) |
| 4 | 1 | 40 | CLK15 (Active = 1, Forced low = 0) |
| 3 | 1 | 36 | CLK14 (Active = 1, Forced low = 0) |
| 2 | 1 | 35 | CLK13 (Active = 1, Forced low = 0) |
| 1 | 1 | 32 | CLK12 (Active = 1, Forced low = 0) |
| 0 | 1 | 31 | CLK11 (Active = 1, Forced low = 0) |

Byte 2: Clock Register (1 = enable, 0 = Stopped)

| Bit | @Pup | Pin# | Description |
|-----|------|------|------------------------------------|
| 7 | 1 | 28 | CLK10 (Active = 1, Forced low = 0) |
| 6 | 1 | 21 | CLK9 (Active = 1, Forced low = 0) |
| 5 | 0 | - | Not Used |
| 4 | 0 | - | Not Used |
| 3 | 0 | - | Not Used |
| 2 | 0 | - | Not Used |
| 1 | 1 | - | Not Used |
| 0 | 1 | - | Not Used |

**SMBus System Clock Buffer****Maximum Ratings**

| | |
|--------------------------|-----------------|
| Voltage Relative to VSS: | -0.3V |
| Voltage Relative to VDD: | 0.3V |
| Storage Temperature: | -65°C to +150°C |
| Operating Temperature: | 0°C to +70°C |
| Maximum Power Supply: | 7V |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

Electrical Characteristics

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|--|--------------------|-----|-----|-----|-------|--|
| Input Low Voltage | VIL | - | - | 0.8 | Vdc | - |
| Input High Voltage | VIH | 2.0 | - | - | Vdc | - |
| Input Low Current | IIL | -66 | | | μA | |
| Input High Current | IIH | | | 66 | μA | |
| Output Low Voltage IOL = 40mA | VOL | - | - | 0.4 | Vdc | All Outputs (see buffer spec) |
| Output High Voltage IOH = 30mA | VOH | 2.4 | - | - | Vdc | All Outputs Using 3.3V Power (see buffer spec) |
| Tri-State leakage Current | Ioz | - | - | 10 | μA | |
| Dynamic Supply Current | Idd ₆₆ | 9 | - | 160 | mA | Input frequency = 66 Mhz - All outputs on and at 30 pF load |
| | Idd ₁₀₀ | 12 | - | 220 | mA | Input frequency 100 Mhz - All outputs on and at 30 pF load |
| Static Supply Current | Isdd | - | - | 4 | mA | All outputs disabled no input clock |
| Short Circuit Current | ISC | 25 | - | - | mA | 1 output at a time - 30 seconds |
| Input Rise Time | VIR | 2.4 | - | - | nS | .8 to 2.4 volts |
| VDD = VDD1 thru VDD9 = 3.3V ±5%, , TA = 0°C to +70°C | | | | | | |

**SMBus System Clock Buffer****Switching Characteristics**

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|--------|-----|-----|-----|-------|-----------------------------|
| Output Duty Cycle | - | 45 | 50 | 55 | % | Measured at 1.5V (50/50 in) |
| Buffer out/out Skew All Buffer Outputs | tSKEW | - | - | 250 | pS | 35 pF Load Measured at 1.5V |
| Buffer input to output Skew | tSKEW | 2.0 | 0 | 5.0 | nS | |
| Jitter Cycle to Cycle* | TJCC | | | 100 | pS | @ 30 pF loading |
| Jitter Absolute (Peak to Peak)* | TJabs | | | 150 | pS | @ 30 pF loading |
| VDD = VDD1 thru VDD9 = 3.3V \pm 5%, , TA = 0°C to +70°C | | | | | | |

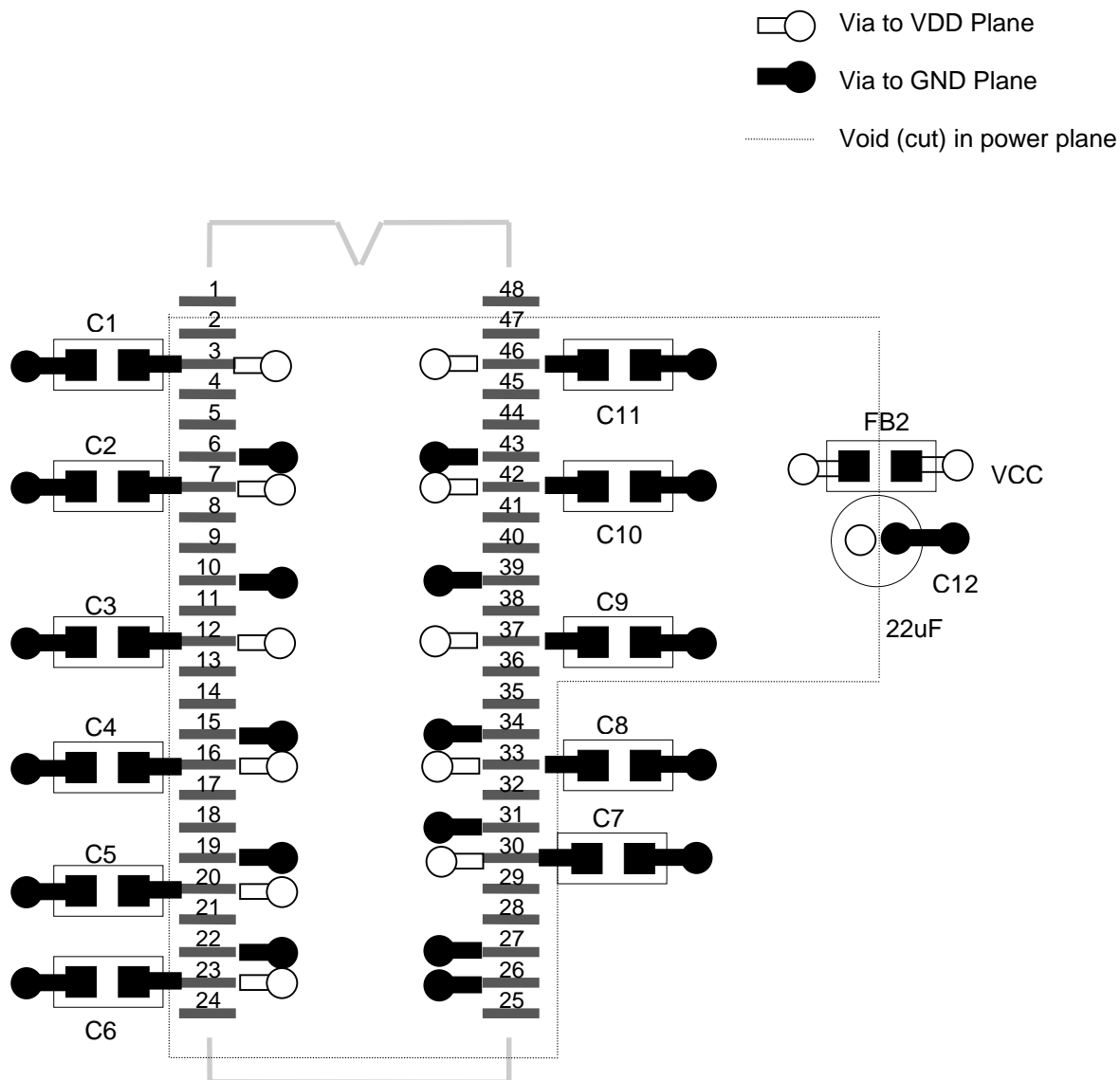
*This jitter is additive to the input clock's jitter.

TB40_ Type Buffer Characteristics (All Clock Outputs)

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|--------------------|-----|-----|------|-------|------------------|
| Pull-Up Current Min | IOH _{min} | 30 | - | 39 | mA | Vout = VDD - .5V |
| Pull-Up Current Max | IOH _{max} | 75 | - | 109 | mA | Vout = 1.5 V |
| Pull-Down Current Min | IOL _{min} | 30 | - | 40 | mA | Vout = 0.4 V |
| Pull-Down Current Max | IOL _{max} | 75 | - | 103 | mA | Vout = 1.2 V |
| Dynamic Output Impedance | Z _O | 8 | - | 15 | Ohms | 66-100 MHz |
| Rise/Fall Time Min Between 0.4 V and 2.4 V | TRF _{min} | 0.5 | - | 1.33 | nS | 30 pF Load |
| Rise/Fall Time Max Between 0.4 V and 2.4 V | TRF _{max} | 0.5 | - | 1.33 | nS | 30 pF Load |
| VDD = VDD1 thru VDD9 = 3.3V \pm 5%, , TA = 0°C to +70°C | | | | | | |

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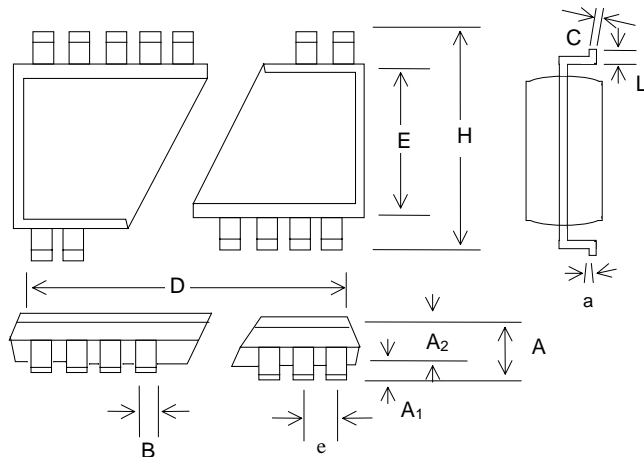
PCB layout Suggestion



This is only a layout recommendation for best performance and lower EMI. the designer may choose a different approach but C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, and C11 (all are 0.1 uf) should always be used and placed as close to their VDD pins as is physically possible.

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Packing Drawing and Dimensions



48 Pin SSOP Outline Dimensions

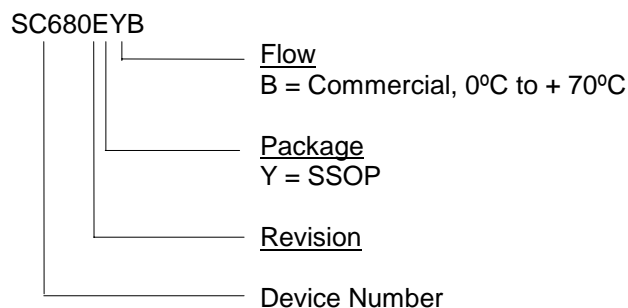
| SYMBOL | INCHES | | | MILLIMETERS | | |
|----------------|------------|-------|--------|-------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.095 | 0.102 | 0.110 | 2.41 | 2.59 | 2.79 |
| A ₁ | 0.008 | 0.012 | 0.016 | 0.20 | 0.31 | 0.41 |
| A ₂ | 0.085 | 0.090 | 0.095 | 2.16 | 2.29 | 2.41 |
| B | 0.008 | 0.010 | 0.0135 | 0.203 | 0.254 | 0.343 |
| c | 0.005 | .008 | 0.010 | 0.127 | 0.20 | 0.254 |
| D | 0.620 | 0.625 | 0.637 | 15.75 | 15.88 | 16.18 |
| E | 0.291 | 0.295 | 0.299 | 7.39 | 7.49 | 7.59 |
| e | 0.0256 BSC | | | 0.640 BSC | | |
| H | 0.395 | 0.408 | 0.420 | 10.03 | 10.36 | 10.67 |
| L | 0.024 | 0.030 | 0.040 | 0.61 | 0.76 | 1.02 |
| a | 0° | 4° | 8° | 0° | 4° | 8° |

Ordering Information

| Part Number | Package Type | Production Flow |
|-------------|--------------|--------------------------|
| SC680EYB | 48 PIN SSOP | Commercial, 0°C to +70°C |

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
SC680EYB
Date Code, Lot #





APPROVED PRODUCT

SC680E

SMBus System Clock Buffer

Notice

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APPROVED PRODUCT

SC680E

SMBus System Clock Buffer

| Document Title: SC680E SMBus System Clock Buffer | | | | |
|---|----------------|-------------------|------------------------|------------------------------|
| Document Number: 38-07026 | | | | |
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 106954 | 06/29/01 | IKA | Convert from IMI to Cypress |