



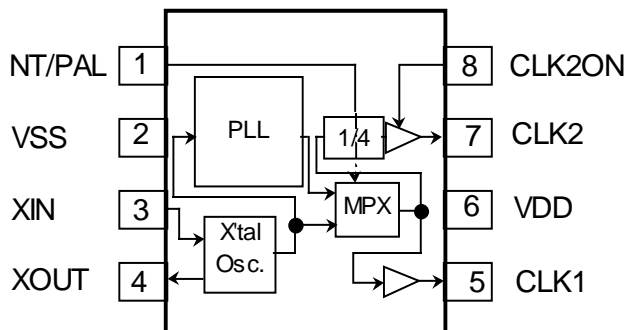
## Programmable NTSC/PAL Clock Generator

### Product Features

The IMISG587 is a clock generator that generates 17.734MHz using Phase Locked Loops (PLLs). The IMISG587 uses a 14.318MHz crystal to produce NTSC or PAL frequencies. The device is packaged in an 8pin TSSOP package for minimum occupation of board space.

- Convert/buffered Fsc frequency using 14.318MHz crystal.
- Internal Loop Filter that requires no external components or adjustments.
- 30 mA buffer switching current
- 8 pin TSSOP package.

### Pin Configuration



### Pin Description

**XIN, XOUT** - Forms an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal, 14.318MHz. XIN may also serve as input for an externally generated reference signal.

**CLK1** – CLK1 is derived from the reference crystal oscillator by using Phase-Locked Loop (PLL) or buffered reference output selected via NT/PAL input pin.

**CLK2** – CLK2 provides the required NTSC or PAL clock frequencies. This is obtained by dividing the CLK1 frequency by four (4).

**NT/PAL** – This pin is used to select NTSC or PAL frequency. When High (default), CLK1 to be selected crystal frequency, 14.318MHz. When Low, CLK1 to be selected PAL frequencies, 17.734MHz, through PLL circuit. See table-1. This pin has an internal pull-up resistor.

**CLK2ON** – This pin is used to enable/disable CLK2 output. When Low, CLK2 to be disabled. When High (default), CLK2 to be enabled. This pin has an internal pull-up resistor.

**VDD** – Circuit positive power supply.

**VSS** – Circuit ground.



## Block Diagram

Table-1



## Programmable NTSC/PAL Clock Generator

### Maximum Ratings

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-30°C to + 125°C
Operating Temperature:	0°C to + 70°C
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

### Electrical Characteristics

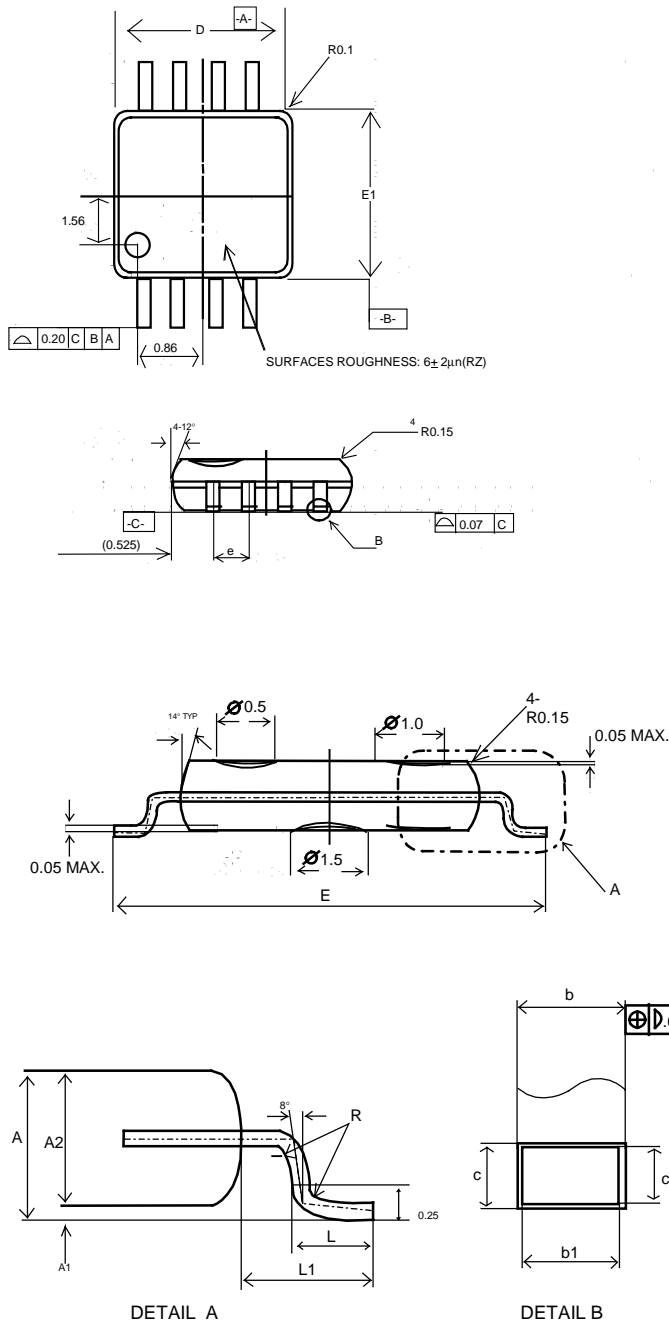
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	V	
Input High Voltage	VIH	2.0	-	-	V	
Input Low Current	IIL	-	-	100	μA	
Input High Current	IIH	-	-	100	μA	
Output Low Voltage	VOL	-	-	0.4	V	IOL=4mA
Output High Voltage	VOH	2.4	-	-	V	IOH=-4mA
Xtal Input / Output Capacitors	CL1,2	-	23	-	PF	X'Tal's CL=11.5pF
Supply Current	IDD	-	9.3	11.0	mA	
Short Circuit Current	ISC	-	-	30	mA	
Supply Voltage Range	VDDR	3.0	3.3	3.6	V	
<b>VDD = 3.3V, TA = 0 to 70°C and CL = 15pF</b>						

### Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise Time	Tr	-	3.7	4.2	ns	0.2*VDD to 0.8*VDD
Output Fall Time	Tf	-	2.1	2.5	ns	0.2*VDD to 0.8*VDD
Output Duty Cycle	Tduty	45	50	55	%	Vth=1.5V
Absolute Jitter	Tj	-	160	250	ps	Vth=1.5V
Power-up Frequency Stabilization	Tpw-on		-	50	ms	From 0.9*VDD to frequency lock
<b>Conditions: VDD = 3.3V +/-10%, TA = 0 to 70°C and CL = 15pF</b>						

## Programmable NTSC/PAL Clock Generator

### Package Drawing and Dimensions



### 8 Pin TSSOP Dimensions

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A1	0.0020	0.0039	0.0059	0.05	0.10	0.15
A2	0.037	0.039	0.041	0.95	1.0	1.05
L	0.020	0.024	0.028	0.50	0.60	0.70
L1	0.035	0.039	0.043	0.90	1.00	1.10
b	0.007	-	0.0011	0.19	-	0.275
b1	0.0076	0.0087	0.0096	0.195	0.22	0.245
c	0.0041	-	0.0069	0.105	-	0.175
c1	0.0041	0.0049	0.0057	0.105	0.125	0.145
θ	0°	-	8°	0°	-	8°
e	0.025 BSC			0.635 BSC		
D	0.114	0.118	0.122	2.9	3.0	3.1
E	0.248	0.252	0.256	6.3	6.4	6.5
E1	0.171	0.173	0.175	4.35	4.40	4.45



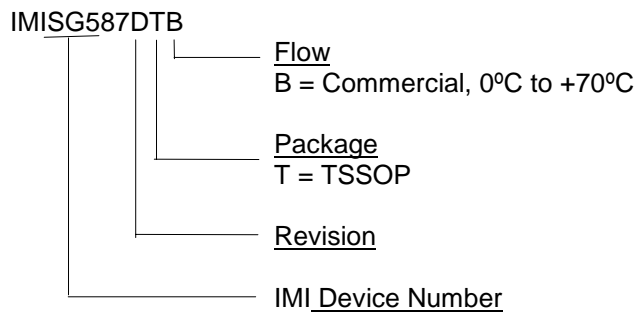
## Programmable NTSC/PAL Clock Generator

### Ordering Information

Part Number	Package Type	Production Flow
IMISG587DTB	8 PIN TSSOP	Commercial, 0°C to +70°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI Date Code  
587DTB



### NOTES:

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# SG587

## Programmable NTSC/PAL Clock Generator

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Rev.	ECN No.	Date of Issue	Orig. of Change	Description of Change
**	107393	05/22/01	IKA	New Data Sheet