Z9102

Variable Delay Motherboard Clock Buffer

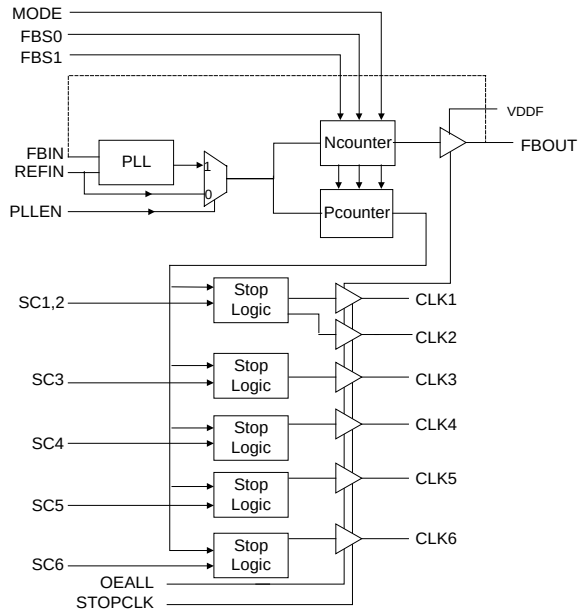
Product Features

- Output phase relationship is precisely controllable with respect to input clock via a dedicated external feedback path.
- 6 Low Skew Clocks Generated
- Outputs are individually enabled.
- Output frequencies from 30 to 100 MHz.
- 3.3 Volt Vdd operation
- Synchronous output enable and disable control
- 45 - 55% output duty cycle
- +/- 100 pSec Cycle to Cycle Jitter
- 32-Lead TQFP (in LQFP Profile) package

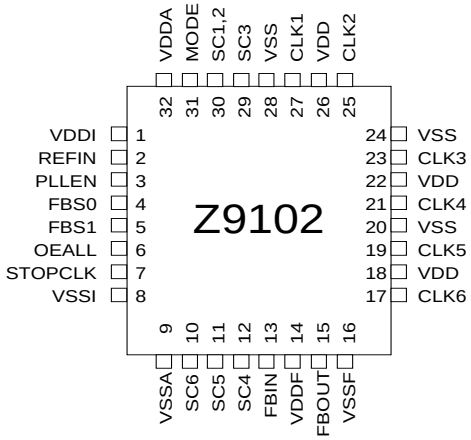
Feedback Scale Select Codes

Mode	FBS1	FBS0	Pcounter	Ncounter
0	0	0	÷ 4	÷ 8
0	0	1	÷ 4	÷ 10
0	1	0	÷ 4	÷ 12
0	1	1	÷ 8	÷ 12
1	0	0	÷ 4	÷ 4
1	0	1	÷ 4	÷ 5
1	1	0	÷ 4	÷ 6
1	1	1	÷ 8	÷ 8

Block Diagram



Pin Configuration



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Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
2	**REFIN**	VDDI	I	LINP	External reference clock input pin.
3	**PLLEN**	VDD	I	LINP PU	This pin routes the REFIN clock to the normal PLL output circuitry when at a logic low level. It is intended to be used for static testing of the parts internal logic.
4, 5	**FBS(0:1)**	VDD	I	LINP PD	Feedback selection pins. These input pins control the internal routing of the feedback output clock that produce the multiplier values listed in the “Feedback Scale Select Code” table on page 1.
31	**MODE**	VDD	I	LINP PD	Combined with the FBS pins, this pin determines the output clocks frequency with respect to the REFIN pin. See table on page 1 for functionality.
6	**OEALL**	VDD	I	LINP PU	Output Enable for all CLK output clocks. When at a logic low level, all outputs are driven to a Tri State.
7	**STOPCLK**	VDD	I	LINP PU	Stop Clock for all CLK output clocks. When at a logic low level CLK(1:6) are driven to a logic low level synchronously with their next occurring high to low transition. This signal does NOT effect the FBOUT clock.
15	**FBOUT**	VDDF	O	S133	Clock source that is used in the device’s external feedback loop. This pin is connected to the device’s FBIN pin either directly or through an external delay circuit.
27, 25, 23, 21, 19, 17	**CLK(1:6)**	VDD	O	S133	These output clocks are the synthesized product of the REFIN clock and the selections programmed on the FB0, FB1 and MODE pins.
20, 24, 28	**VSS**	---	P	PWR	Ground pins for the device.
18, 22, 26	**VDD**	---	P	PWR	3.3 Volt Power supply pins for clock buffer circuit
14	**VDDF**	---	P	PWR	3.3 volt power supply pins for the FBOUT clock output buffers.
30	**SC1,2**	VDD	I	LINP PU	Synchronous output enable control pin for CLK1 and CLK2.
29	**SC3**	VDD	I	LINP PU	Synchronous output enable control pin for CLK3 pins.
12	**SC4**	VDD	I	LINP PU	Synchronous output enable control pin for CLK4 pins.
11	**SC5**	VDD	I	LINP PU	Synchronous output enable control pin for CLK5 pins.
10	**SC6**	VDD	I	LINP PU	Synchronous output enable control pin for CLK6 pins.
32	**VDDA**		P	PWR	Analog power. See recommended circuitry later in this datasheet.
16	**VSSF**	---	P	PWR	Ground supply for pin 15 (FBOUT) buffer.
9	**VSSA**	---	P	PWR	Ground power connection for analog circuitry.
8	**VSSI**	---	P	PWR	Ground power connection for input clock circuitry.
1	**VDDI**	---	P	PWR	3.3V power connection for input clock circuitry.

NOTES:

1. ***Pins with “PU” or “PD” listed in the Type column indicate that these pins have internal pull-up or pull down resistors. These resistors ensure that the device will sense a logic 1 (high) or logic 0 (low) condition respectively when the device is powered up and no electrical connection is made to these pins.***
2. ***All synchronous output enables, when driven to a logic low level, will cause their associated output clocks to transition to a logic low level and remain there. Likewise, they will cause their associated output clocks to begin running when driven to a logic high level. This enabling and disabling action will produce no runt (short or long) clock output cycles.***

Maximum Ratings

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0ºC to + 125ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to up to 2,000 volts of static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	
Input High Voltage	VIH	2.0	-	3.6	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			±100	µA	
Tri-State leakage Current	Ioz	-	-	5	µA	
Dynamic Supply Current	Idd	-	-	125	mA	CLK(1:6) = 100 MHz all at rated load
Maximum Core Supply Current	I_{CC}			20	mA	Current drawn by VDDA (pin 32)
VDD = VDDF =3.3V ±5%, TA = 0ºC to +70ºC						

Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	TO_{dc}	45	50	55	%	Measured @ 1.5V, CLK25 measured at 1.25V
REFIN Rise and Fall Time	$TR_{r,f}$		-	3.0	nSec	0.4 to 2.4 Volts
Input Frequency	REFIN	Controlled by VCO lock range			MHz	See "VCO operating range" section of this data sheet
Reference Input Duty Cycle	F_{refDC}	25		75	%	Measured @ 1.5V
Output Frequency	F_{OUT4}	-	-	100	MHz	Ncounter = ÷4
	F_{OUT5}	-	-	96	MHz	Ncounter = ÷5
	F_{OUT6}	-	-	80	MHz	Ncounter = ÷6
VCO operating frequency.	F_{VCO}	200	-	400	MHz	
Output to Output clock skew (CLK(2:6])	T_{SKWO}	-	-	300	pSec	Measured at 1.5 Volts, 30 pF load on all clocks
Output to Output clock skew (CLK25 to Q(2:6))	T_{SKWO25}	-	-	600	pSec	Measured at 1.5 Volts, 30 pF load on CLK(2:6) and @ 1.25V on CLK25
REFIN TO FBIN	Toffset	-	150	-	PSec	Notes 1, 2, 3
ΔPeriod Adjacent Cycles	ΔPs			+/- 100	pS	Short term jitter (adjacent cycle) Select Code 100 50 MHz in/out
Maximum PLL Lock Time	tLOK			10	ms	
Power Up Ramp	tpr	250	-	20,000	nS	Measured between 0.3 and 3.0 volts
VDD = VDDF =3.3V ±5%, TA = 0ºC to +70ºC						

Notes:
1. Using the averaging feature of the scope to filter out the jitter component.
2. REFIN rise time = FBIN rise time.
3. Frequency >66 MHz.

Buffer Characteristics for CLK (1:6) and FBOUT

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-17	-	-	mA	Vout = VD – 0.5
Pull-Up Current Max	IOH_{max}	-36	-	-	mA	Vout = VDD/2
Pull-Down Current Min	IOL_{min}	16	-	-	mA	Vout = 0.4 V
Pull-Down Current Max	IOL_{max}	43	-	-	mA	Vout = VDD/2
Rise & Fall Time Between 0.8 V and 2.0 V	TRF	0.1	-	1.0	nS	30 pF Load
Output buffer Dynamic Impedance	Z_O	7	-	10	Ohms	
VDD = VDDF =3.3V ±5%, TA = 0ºC to +70ºC						

Output Clock Disable and Enable Timing

When each clock enable pin (SC1,2 through SC6) is brought to a logic low level, its related output clock (CKL(1,2) through CLK6) will de forced to a logic low level. All clocks maintain a valid high period on transitions from running to stopped. The clocks transition between running and stopped by waiting for one normally occurring positive edge followed by a negative edge of their own clock. At that point they remain low until their respective SC signal goes high. At that point the internal logic waits 1 internally occurring cycle and the clock then begins normal output at the next naturally occurring low to high transitioning time.

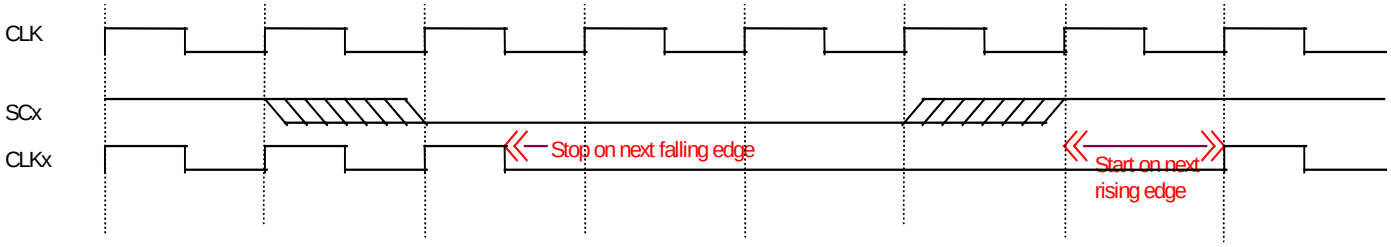


Fig. 2

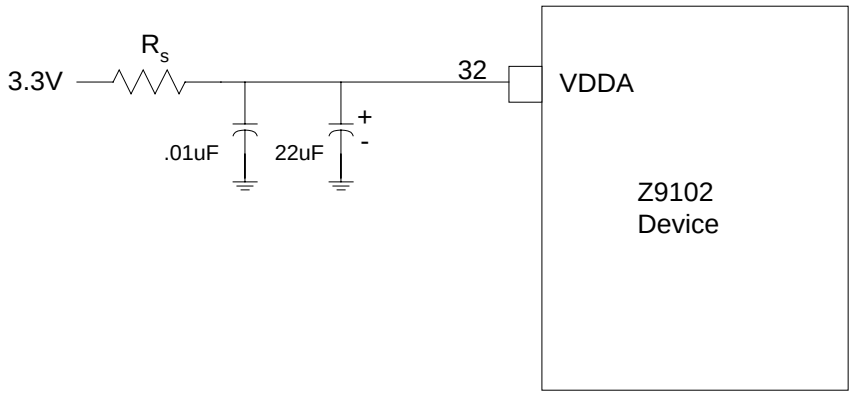


Fig. 3

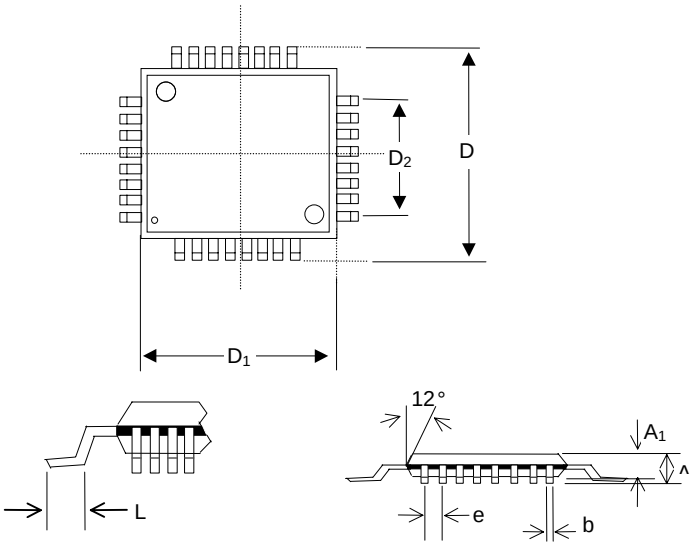
Figure 3 shows the recommended power supply decoupling circuitry to obtain minimum device clock noise (jitter). Designs shown implement this decoupling scheme in noisy VDD environments to protect the device's internal analog circuitry from digital noise born on the main 3.3 volt supply. A range of 2.2 to 15 ohms is recommended for R_s. R_s should be adjusted to the minimum value required to produce acceptable performances from the device. The ultimate limitation on the R_s maximum value is the device's minimum VDDA spec.

Frequency Applications Examples

Table 1. Z9102 Example Min/Max Frequency Table

Mode	FBS1	FBS0	REFIN Frequency Min. (MHz)	REFIN Frequency Max (MHz)	CLK(1:6), Output Frequency (MHz)	Example:
1	0	0	50	100	1 x REFIN	REFIN = 66.7 MHz CLK* = 66.7 MHz
1	0	1	40	80	1.25 x REFIN	REFIN = 66.7 MHz CLK* = 83.3 MHz
1	1	0	33.3	66.7	1.5 x REFIN	REFIN = 66.7 MHz CLK* = 100 MHz
1	1	1	25	50	1 x REFIN	REFIN = 33.3 MHz CLK* = 33.3 MHz
0	0	0	25	50	2 x REFIN	REFIN = 33.3 MHz CLK* = 66.7 MHz
0	0	1	20	40	2.5 x REFIN	REFIN = 33.3 MHz CLK* = 83.3 MHz
0	1	0	16.7	33.3	3 X REFIN	REFIN = 33.3 MHz CLK* = 100 MHz
0	1	1	16.7	33.3	1.5 X REFIN	REFIN = 33.3 MHz CLK* = 50 MHz

Package Drawing and Dimensions



32 Pin TQFP (LQFP) Outline Dimensions

	MILLIMETERS			INCHES		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	.055	.059	0.063
A_1	1.35	1.40	1.45	0.053	0.055	0.057
D	8.95	9.00	9.05	0.352	0.354	0.356
D_1	6.95	7.00	7.05	0.274	0.276	0.278
b	0.30	0.37	0.45	0.012	0.015	0.018
e	0.80 BSC			0.0315 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.029

Ordering Information

Part Number	Package Type	Production Flow
Z9102BAB	32 PIN TQFP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: CYPRESS
Z9102BAB, Date Code, Lot #

Z9102BAB

- Flow
  B = Commercial, 0ºC to + 70ºC
- Package
  A = TQFP
- Revision
- Device Number

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**	107118	06/05/01	IKA	Convert from IMI to Cypress