



APPROVED PRODUCT

**Z9104**

*Variable Delay Motherboard Clock Buffer*

## Product Features

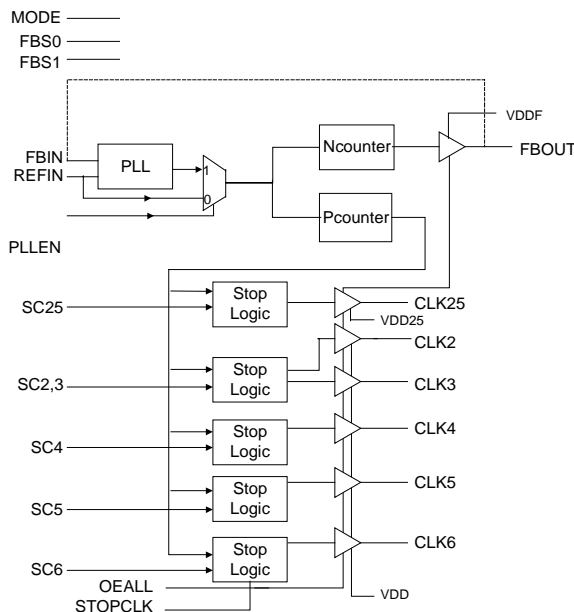
- Output phase relationship is precisely controllable with respect to input clock via a dedicated external feedback path.
- 2K volts ESD protected
- 6 Low Skew Clocks Generated
- One 2.5 Volt output clock
- Outputs are individually enabled.
- Output frequencies from 30 to 100 MHz.
- 3.3 Volt Vdd operation
- Synchronous output enable and disable control
- 45 - 55% output duty cycle
- +/- 100 pSec Cycle to Cycle Jitter
- 32-Lead TQFP package

## Feedback Scale Select Codes

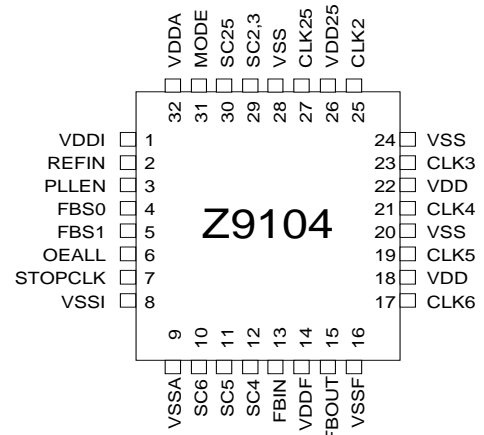
Mode	FBS1	FBS0	Pcounter	Ncounter	MF*
0	0	0	÷ 4	÷ 8	2.0
0	0	1	÷ 4	÷ 10	2.5
0	1	0	÷ 4	÷ 12	3.0
0	1	1	÷ 8	÷ 12	1.5
1	0	0	÷ 4	÷ 4	1.0
1	0	1	÷ 4	÷ 5	1.25
1	1	0	÷ 4	÷ 6	1.5
1	1	1	÷ 8	÷ 8	1.0

\*Multiplication Factor – The multiplication factor for these configurations is the output frequency with respect to REFIN (FOUT=FIN X multiplication factor)

## Block Diagram



## Pin Configuration



**Pin Description**

PIN No.	Pin Name	PWR	I/O	Description
2	REFIN	VDDI	I	External reference clock input pin.
3	PLEN	VDD	I	This pin routes the REFIN clock to the normal PLL output circuitry when at a logic low level. It is intended to be used for static testing of the parts internal logic.
4, 5	FBS(0:1)	VDD	I	Feedback selection pins. These input pins control the internal routing of the feedback output clock that produce the multiplier values listed in the "Feedback Scale Select Code" table on page 1.
31	MODE	VDD	I	Combined with the FBS pins, this pin determines the output clocks frequency with respect to the REFIN pin. See table on page 1 for functionality.
6	OEALL	VDD	I	Output Enable for all CLK output clocks. When at a logic low level, all outputs are driven to a Tri State.
7	STOPCLK	VDD	I	Stop Clock for all CLK output clocks. When at a logic low level CLK (1:6) are driven to a logic low level synchronously with their next occurring high to low transition. This signal does NOT effect the FBOUT clock.
15	FBOUT	VDDF	O	Clock source that is used in the device's external feedback loop. This pin is connected to the device's FBIN pin either directly or through an external delay circuit.
27	CLK25	VDD25	O	2.5 Volt output clock copy of CLK2:6
25, 23, 21, 19, 17	CLK(2:6)	VDD	O	These output clocks are the synthesized product of the REFIN clock and the selections programmed on the FB0, FB1 and MODE pins.
20, 24, 28	VSS	---	P	Ground pins for the device.
18, 22	VDD	---	P	3.3 Volt Power supply pins for clock buffer circuit
14	VDDF	---	P	3.3 volt power supply pins for the FBOUT clock output buffers.
30	SC25	VDD	I	Synchronous output enable control pin for CLK25.
29	SC2:3	VDD	I	Synchronous output enable control pin for CLK2 and CLK3 pins.
12	SC4	VDD	I	Synchronous output enable control pin for CLK4 pins.
11	SC5	VDD	I	Synchronous output enable control pin for CLK5 pins.
10	SC6	VDD	I	Synchronous output enable control pin for CLK6 pins.
26	VDD25	---	P	2.5 volt power supply pin for the CLK25 clock output buffers.
32	VDDA	---	P	Analog power. See recommended circuitry later in this datasheet.
16	VSSF	---	P	Ground supply for pin 15 (FBOUT) buffer.
9	VSSA	---	P	Ground power connection for analog circuitry.
8	VSSI	---	P	Ground power connection for input clock circuitry.
1	VDDI	---	P	3.3V power connection for input clock circuitry.

**NOTES:**

1. Pins with "PU" or "PD" listed in the Type column indicate that these pins have internal pull-up or pull down resistors. These resistors ensure that the device will sense a logic 1 (high) or logic 0 (low) condition respectively when the device is powered up and no electrical connection is made to these pins.
2. All synchronous output enables, when driven to a logic low level, will cause their associated output clocks to transition to a logic low level and remain there. Likewise, they will cause their associated output clocks to begin running when driven to a logic high level. This enabling and disabling action will produce no runt (short or long) clock output cycles.

**Variable Delay Motherboard Clock Buffer****Maximum Ratings**

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	0°C to + 125°C
Operating Temperature:	0°C to +70°C
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to up to 2,000 volt static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS < (V_{in} \text{ or } V_{out}) < VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

**Electrical Characteristics**

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	
Input High Voltage	VIH	2.0	-	3.6	Vdc	-
Input Low Current	IIL			-66	μA	
Input High Current	IIH			±100	μA	
Output Voltage High for CLK(2:6)	VOH	2.4			Vdc	@IOH = -20ma
Output Voltage for High CLK25	VOH <sub>C25</sub>	2.0		0.5	Vdc	@IOH = -20ma
Output Voltage Low for CLK25	VIL	1.0			Vdc	@IOL = 20ma
Tri-State leakage Current	Ioz	-	-	10	μA	
Dynamic Supply Current	Idd	-	-	150	mA	CLK(1:6) = 100 MHz all at rated load
Maximum Core Supply Current	I <sub>CC</sub>			130	mA	
Maximum PLL Supply Current	I <sub>CCPLL</sub>			20	mA	
<b>VDD = VDDF = 3.3V ±5%, TA = 0°C to +70°C</b>						



## Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	$TO_{dc}$	45	50	55	%	Measured @ 1.5V, CLK25 measured at 1.25V
REFIN Rise and Fall Time	$TR_{r,f}$		-	3.0	nSec	0.4 to 2.4 Volts
Input Frequency	REFIN	Controlled by VCO lock range			MHz	See "VCO operating range" section of this data sheet
Reference Input Duty Cycle	$F_{refDC}$	25		75	%	Measured @ 1.5V
Output Frequency	$F_{OUT4}$	-	-	100	MHz	Ncounter = +4
	$F_{OUT5}$	-	-	96	MHz	Ncounter = +5
	$F_{OUT6}$	-	-	80	MHz	Ncounter = +6
VCO operating frequency.	$F_{VCO}$	200	-	400	MHz	
Output to Output clock skew (CLK(2:6))	$T_{SKWO}$	-	-	300	pSec	Measured at 1.5 Volts, 30 pF load on all clocks
Output to Output clock skew (CLK25 to Q(2:6))	$T_{SKWO25}$	-	-	600	pSec	Measured at 1.5 Volts, 30 pF load on CLK(2:6) and @ 1.25V on CLK25
REFIN TO FBIN	$T_{offset}$	-	150	-	PSec	Notes 1, 2, 3
$\Delta$ Period Adjacent Cycles	$\Delta Ps$			+/- 100	pS	Short term jitter (adjacent cycle) Select Code 100 50 MHz in/out
Maximum PLL Lock Time	$t_{LOK}$			10	ms	
Power Up Ramp	$t_{pr}$	250	-	20,000	nS	Measured between 0.3 and 3.0 volts
<b><math>VDD = VDDF = 3.3V \pm 5\%</math>, <math>TA = 0^{\circ}C</math> to <math>+70^{\circ}C</math></b>						

### Notes:

1. Using the averaging feature of the scope to filter out the jitter component.
2. REFIN rise time = FBIN rise time.
3. Frequency >66 MHz.

## Buffer Characteristics for CLK (2:6) and FBOUT

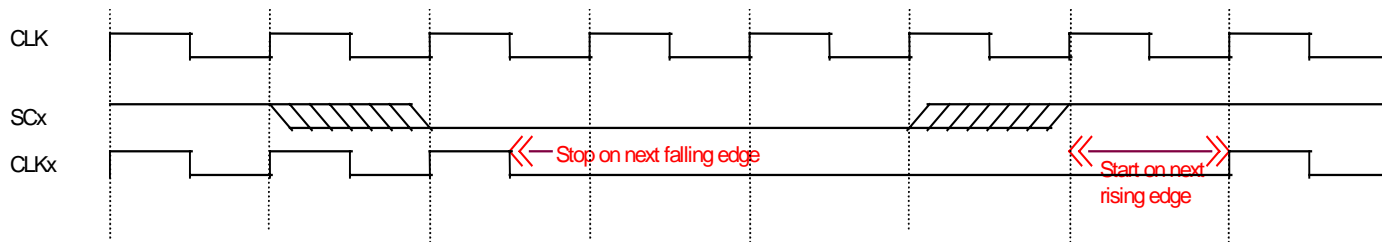
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	$IOH_{min}$	-17	-	-	mA	$V_{out} = VDD - .5V$
Pull-Up Current Max	$IOH_{max}$	-36	-	-	mA	$V_{out} = VDD/2$
Pull-Down Current Min	$IOL_{min}$	16	-	-	mA	$V_{out} = 0.4 V$
Pull-Down Current Max	$IOL_{max}$	43	-		mA	$V_{out} = VDD/2$
Rise & Fall Time Between 0.8 V and 2.0 V	TRF	0.6	-	1.0	nS	30 pF Load
Output buffer Dynamic Impedance	$Z_o$	7	-	10	Ohms	
<b><math>VDD = VDDF = 3.3V \pm 5\%</math>, <math>TA = 0^{\circ}C</math> to <math>+70^{\circ}C</math></b>						

**Buffer Characteristics for CLK25**

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	$IOH_{min}$	-13	-	-	mA	$V_{out} = V_{DD25} - .5V$
Pull-Up Current Max	$IOH_{max}$	-25	-	-	mA	$V_{out} = V_{DD25}/2$
Pull-Down Current Min	$IOL_{min}$	11	-	-	mA	$V_{out} = 0.4V$
Pull-Down Current Max	$IOL_{max}$	25	-	-	mA	$V_{out} = V_{DD25}/2$
Rise & Fall Time Between 0.8 V and 2.0 V	TRF	0.1	-	1.0	nS	30 pF Load
Output buffer Dynamic Impedance	$Z_o$	7		10	Ohms	
<b><math>V_{DD} = V_{DDF} = 3.3V \pm 5\%</math>, <math>V_{DD25} = 2.5 \pm 5\%</math>, <math>T_A = 0^{\circ}C</math> to <math>+70^{\circ}C</math></b>						

**Output Clock Disable and Enable Timing**

When each clock enable pin (SC25 through SC6) is brought to a logic low level, its related output clock (CLK25 through CLK6) will be forced to a logic low level. All clocks maintain a valid high period on transitions from running to stopped. The clocks transition between running and stopped by waiting for one normally occurring positive edge followed by a negative edge of their own clock. At that point they remain low until their respective SC signal goes high. At that point the internal logic waits 1 internally occurring cycle and the clock then begins normal output at the next naturally occurring low to high transitioning time.


**Fig. 2**

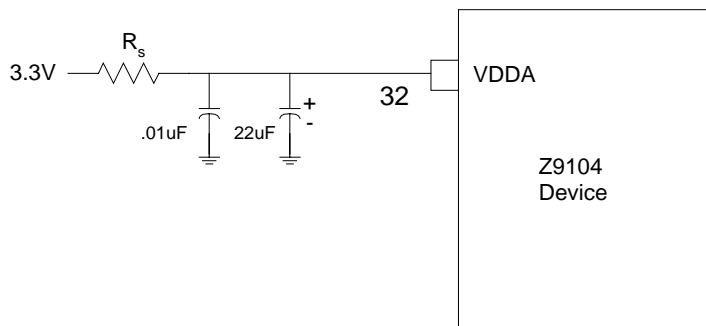
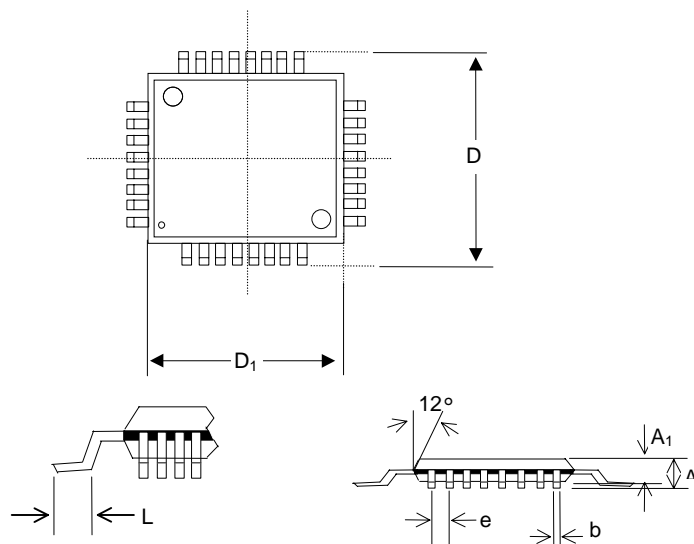

**Fig. 3**

Figure 3 shows the recommended power supply decoupling circuitry to obtain minimum device clock noise (jitter). Designs shown implement this decoupling scheme in noisy VDD environments to protect the device's internal analog circuitry from digital noise born on the main 3.3 volt supply. A range of 2.2 to 15 ohms is recommended for  $R_s$ .  $R_s$  should be adjusted to the minimum value required to produce acceptable performances from the device. The ultimate limitation on the  $R_s$  maximum value is the device's minimum VDDA spec.

## Frequency Applications Examples

**Table 1. Z9104 Example Min/Max Frequency Table**

Mode	FBS1	FBS0	REFIN Frequency Min. (MHz)	REFIN Frequency Max (MHz)	CLK(25:6), Output Frequency (MHz)	Example:
1	0	0	50	100	1 x REFIN	REFIN = 66.7 MHz CLK* = 66.7 MHz
1	0	1	40	80	1.25 x REFIN	REFIN = 66.7 MHz CLK* = 83.3 MHz
1	1	0	33.3	66.7	1.5 x REFIN	REFIN = 66.7 MHz CLK* = 100 MHz
1	1	1	25	50	1 x REFIN	REFIN = 33.3 MHz CLK* = 33.3 MHz
0	0	0	25	50	2 x REFIN	REFIN = 33.3 MHz CLK* = 66.7 MHz
0	0	1	20	40	2.5 x REFIN	REFIN = 33.3 MHz CLK* = 83.3 MHz
0	1	0	16.7	33.3	3 X REFIN	REFIN = 33.3 MHz CLK* = 100 MHz
0	1	1	16.7	33.3	1.5 X REFIN	REFIN = 33.3 MHz CLK* = 50 MHz

**Package Drawing and Dimensions**

**32 Pin TQFP Outline Dimensions**

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.000	1.100	1.200	0.039	0.043	0.047
A <sub>1</sub>	0.950	1.000	1.050	0.037	0.039	0.041
D	8.950	9.000	9.050	0.352	0.354	0.356
D <sub>1</sub>	6.95	7.000	7.050	0.274	0.276	0.278
b	0.30	0.37	0.45	0.012	0.015	0.018
e	0.80 BSC			0.0315 BSC		
L	0.500	0.600	0.700	0.020	0.024	0.028

**Ordering Information**

Part Number	Package Type	Production Flow
Z9104CAB	32 PIN TQFP	Commercial, 0°C to +70°C

**Note:** The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

**Marking:** Example: Cypress  
Z9104CAB,  
Date Code, Lot #

Z9104CAB

- Flow  
B = Commercial, 0°C to + 70°C
- Package  
A = TQFP
- Revision
- Device Number

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<b>Document Title:</b> Z9104 Variable Delay Motherboard Clock Buffer				
<b>Document Number:</b> 38-07083				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107119	06/05/01	IKA	Convert from IMI to Cypress
*A	108351	07/30/01	NDP	Change Production flow from "Commercial" to "Industrial". Change Part Number Revision from "C" to "D".