Z9960

2.5V/3.3V, 200MHz Multi-Output Zero Delay Buffer

Product Features

- 2.5V or 3.3V Operation
- Output Frequency up to 200MHz
- Supports PowerPC™, and Pentium™ Processors
- 21 Clock Outputs: Drive up to 42 Clock Lines
- LVPECL or LVCMOS/LVTTL Clock Input
- Output-to-Output Skew < 150ps
- Split 2.5V/3.3V Outputs
- Spread Spectrum Compatible
- Glitch-free Output Clocks Transitioning
- Output Disable Control
- Pin Compatible with MPC9600
- Industrial Temp. Range: -40°C to +85°C
- 48-Pin LQFP Package

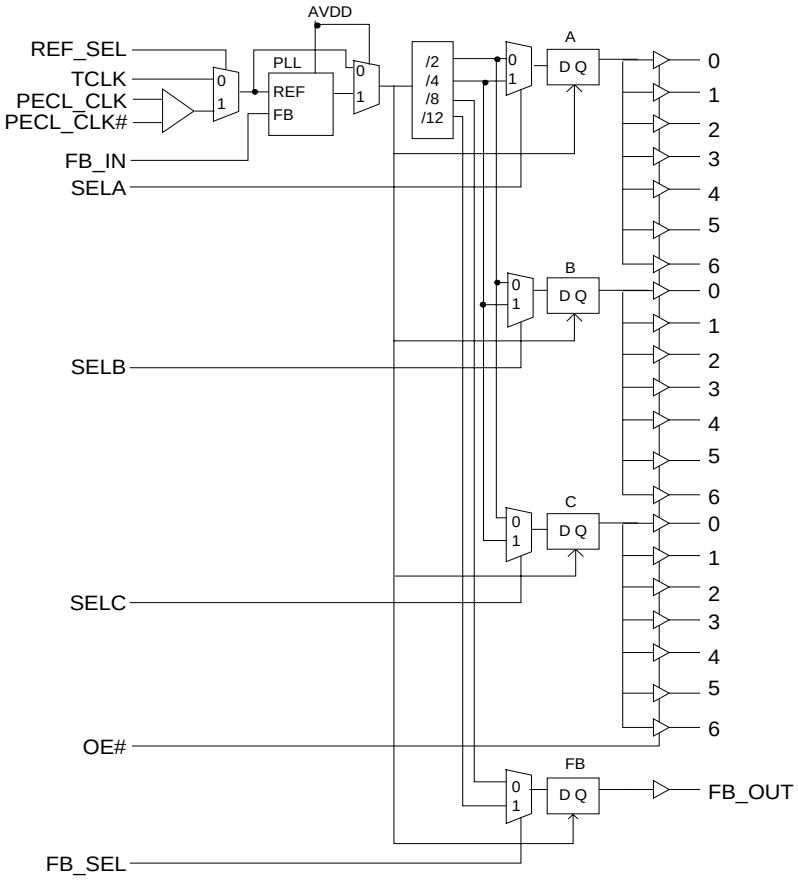
Frequency Table *

SELA	QA	SELB	QB	SELC	QC	FB_SEL	FB_OUT
0	VCO/2	0	VCO/2	0	VCO/2	0	VCO/8
1	VCO/4	1	VCO/4	1	VCO/4	1	VCO/12

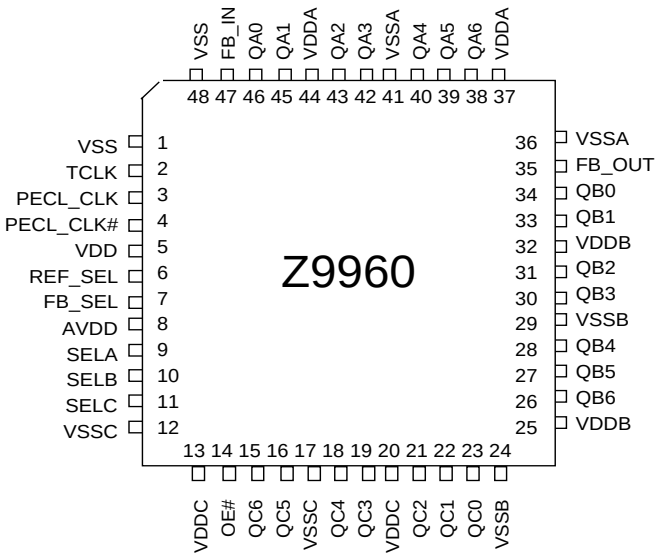
* Input frequency range: 16MHz to 33MHz (FB_SEL=1), or 25MHz to 50MHz (FB_SEL=0)

Table 1

Block Diagram



Pin Configuration



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Pin Description

PIN	NAME	PWR	I/O	Description
3	**PECL_CLK**		I, PD	PECL Clock Input.
4	**PECL_CLK#**		I, PU	PECL Clock Input.
2	**TCLK**		I, PD	External Reference/Test Clock Input.
38, 39, 40, 42, 43, 45, 46	**QA(6:0)**	VDDA	O	Clock Outputs. See Table 1 for frequency selections.
26, 27, 28, 30, 31, 33, 34	**QB(6:0)**	VDDB	O	Clock Outputs. See Table 1 for frequency selections.
15, 16, 18, 19, 21, 22, 23	**QC(6:0)**	VDDC	O	Clock Outputs. See Table 1 for frequency selections.
35	**FB_OUT**	VDD	O	Feedback Clock Output. Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL; see Table 1. A bypass delay capacitor at this output will control Input Reference/ Output Banks phase relationships.
9	**SELA**		I, PU	Frequency Select Inputs. These inputs select the divider ratio at QA(0:6) outputs. See Table 1
10	**SELB**		I, PU	Frequency Select Inputs. These inputs select the divider ratio at QB(0:6) outputs. See Table 1
11	**SELC**		I, PU	Frequency Select Inputs. These inputs select the divider ratio at QC(0:6) outputs. See Table 1
7	**FB_SEL**		I, PU	Feedback Select Inputs. These inputs select the divide ratio at FB_OUT output. See Table 1
47	**FB_IN**		I, PD	Feedback Clock Input. Connect to FB_OUT for accessing the PLL.
6	**REF_SEL**		I, PU	Reference Select Input. When high, the PECL clock is selected. And when low, TCLK is the reference clock.
14	**OE#**		I, PD	Output Enable Input. When asserted low, enables all of the outputs. When pulled high, disables to high impedance all of the outputs except FB_OUT.
37, 44	**VDDA**			Power Supply for Bank A Clock Buffers
25, 32	**VDDB**			Power Supply for Bank B Clock Buffers
13, 20	**VDDC**			Power Supply for Bank C Clock Buffers
5	**VDD**			Power Supply for Core.
8	**AVDD**			Power Supply for PLL. When AVDD is set low, PLL is bypassed and all the outputs except FB_OUT are disabled to high impedance.
36, 41	**VSSA**			Common Ground for Bank A
24, 29	**VSSB**			Common Ground for Bank B
12, 17	**VSSC**			Common Ground for Bank C
1, 48	**VSS**			Common Ground

A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Function Table

Control Pin	0	1
REF_SEL	TCLK	PECL_CLK
AVDD	PLL Bypass, Outputs Disabled (except FB_OUT)	PLL Power
OE#	Outputs Enabled	Outputs Disabled (except FB_OUT)
SELA	Output Bank A at VCO/2	Output Bank A at VCO/4
SELB	Output Bank B at VCO/2	Output Bank B at VCO/4
SELC	Output Bank C at VCO/2	Output Bank C at VCO/4
FB_SEL	Feedback Output at VCO/8	Feedback Output at VCO/12

Maximum Ratings

Input Voltage Relative to VSS:	VSS-0.3V
Input Voltage Relative to VDD:	VDD+0.3V
Storage Temperature:	-65°C to + 150°C
Operating Temperature:	-40°C to +85°C
Maximum ESD Protection	2kV
Maximum Power Supply:	5.5V
Maximum Input Current:	±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL[1]	VSS	-	0.7	V	
Input High Voltage	VIH[1]	1.7	-	VDD	V	
Peak-to-Peak Input Voltage PECL_CLK	VPP	500	-	1000	mV	
Common Mode Range PECL_CLK	VCMR[2]	VDD-1.4	-	VDD-0.6	V	
Input Low Current (@ VIL = VSS)	IIL[3]			-120	µA	
Input High Current (@ VIH = VDD)	IIH[3]			120	µA	
Output Low Voltage	VOL[4]			0.6	V	IOL = 15mA
Output High Voltage	VOH[4]	1.8			V	IOH = -15mA
Quiescent Supply Current	IDD	-	10	13	mA	VDD and AVDD
Input Pin Capacitance	Cin	-	4	-	pF	
VDD = 2.5V ± 5%, TA = -40°C to +85°C						

Note 1: The LVCMOS inputs threshold is at 30% of VDD

Note 2: The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification.

Note 3: Inputs have pull-up/pull-down resistors that affect input current

Note 4: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL[1]	VSS	-	0.8	V	
Input High Voltage	VIH[1]	2.0	-	VDD	V	
Peak-to-Peak Input Voltage PECL_CLK	VPP	500	-	1000	mV	
Common Mode Range PECL_CLK	VCMR[2]	VDD-1.4	-	VDD-0.6	V	
Input Low Current (@ VIL = VSS)	IIL[3]			-120	µA	
Input High Current (@ VIH = VDD)	IIH[3]			120	µA	
Output Low Voltage	VOL[4]			0.55	V	IOL = 24mA
Output High Voltage	VOH[4]	2.4			V	IOH = -24mA
Quiescent Supply Current	IDD	-	15	20	mA	VDD and AVDD
Input Pin Capacitance	Cin	-	4	-	pF	
VDD = 3.3V ± 5%, TA = -40°C to +85°C						

Note 1: The LVCMOS inputs threshold is at 30% of VDD
Note 2: The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification.
Note 3: Inputs have pull-up/pull-down resistors that affect input current
Note 4: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Fref	Reference Input Frequency	16		33	MHz	FB_SEL = 1
		25		50		FB_SEL = 0
FrefDC	Reference Input Duty Cycle	25		75	%	
Fvco	PLL VCO Lock Range	200		400	MHz	
Tlock	Maximum PLL lock Time			10	ms	
Tr / Tf	Output Clocks Rise / Fall Time[2,3]	0.1		1.0	ns	0.55V to 2.0V, VDD = 3.3V
						0.5V to 1.8V, VDD=2.5V
Fout	Maximum Output Frequency	100		200	MHz	Q (÷2)
		50		100		Q (÷4)
FoutDC	Output Duty Cycle[2,3]	45	50	55	%	
tpZL, tpZH	Output Enable Time[2] (all outputs)	2		10	ns	
tpLZ, tpHZ	Output Disable Time[2] (all outputs)	2		8	ns	
TCCJ	Cycle to Cycle Jitter[2,3]		+/- 100		ps	
Tskew	Any Output to Any Output Skew[2,3]			150	ps	Same Frequency
				300		Different Frequency
Tskew	Bank to Bank Skew			400	ps	Banks at different voltages
Tskew(pp)	Part to Part Skew[4]			450	ps	
Tpd	Phase Error[2,3] TCLK or PECL_CLK to FB_IN	0	100	200	ps	VDD = 3.3V
		25	125	225		VDD = 2.5V
VDD = 2.5V ± 5% or 3.3V ± 5%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production.
Note 2: Outputs loaded with 30pF each.
Note 3: 50Ω transmission line terminated into VDD/2.
Note 4: Part to Part skew at a given temperature and voltage

Description

The Z9960 has an integrated PLL that provides low skew and low jitter clock outputs for high performance microprocessors. Three independent banks of seven outputs as well as an independent PLL feedback output, FB_OUT, provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 400 MHz. This allows a wide range of output frequencies up to 200MHz.

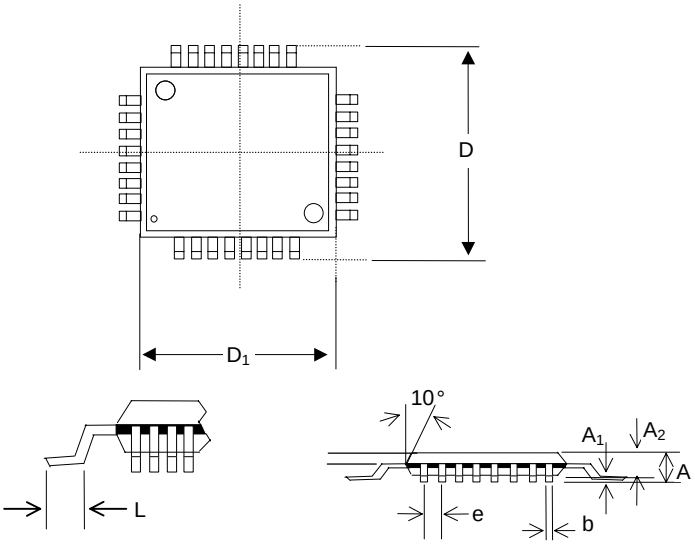
The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by FB_SEL select inputs; refer to Frequency Table. The VCO frequency is then divided down to provide the required output frequencies.

Zero Delay Buffer

When used as a zero delay buffer the Z9960 will likely be in a nested clock tree application. For these applications the Z9960 offers a low voltage PECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The Z9960 then can lock onto the LVPECL reference and translate with near zero delay to low skew outputs.

By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the Z9960 is a function of the configuration used.

Package Drawing and Dimensions (48 LQFP)



48 Pin LQFP Outline Dimensions

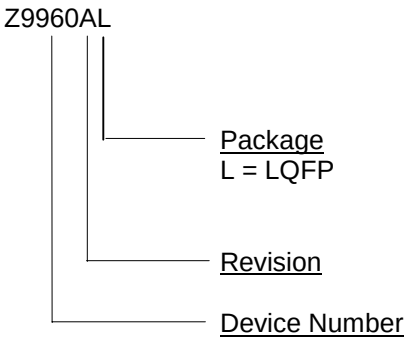
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.063	-	-	1.60
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.053	-	0.057	1.35	-	1.45
D	-	0.354	-	-	9.00	-
D_1	-	0.276	-	-	7.00	-
b	0.007	-	0.011	0.17	-	0.27
e	0.02 BSC			0.50 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
Z9960AL	48 LQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: CYPRESS
Z9960AL
Date Code, Lot #



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**	107123	06/06/01	IKA	Convert from IMI to Cypress