Z9975

3.3V, 150MHz, Multi-Output Zero Delay Buffer

Product Features

- Output Frequency up to 150MHz
- Supports Power PC ™, and Pentium ™ Processors
- 15 Clock Output: Frequency Configurable
- Two Reference Clock Inputs for Dynamic Toggling
- Output Tri-State Control
- Spread Spectrum Compatible
- 3.3V Power Supply
- Industrial Temp. Range: -40°C to +85°C
- 52 Pin TQFP Package

Product Description

The Z9975 is a low cost 3.3V zero delay clock driver for high speed signal buffering and redistribution.

It provides the designer with the flexibility of selecting various Output/Input Frequency ratios selected by fsela, fselb, fselc, fselFB(0:1), and VCO_sel input settings.

The Z9975 integrates PLL technology for Zero delay propagation from Input to Output. The PLL feedback is externally available for propagation delay tuning and divide ratio alternatives as per table 1.

The Z9975 has three banks of outputs with independent divider stages. These dividers allow the banks to have different frequencies as per table 2.

TCLK0 and TCLK1 one are selectable input reference clocks and may be toggled dynamically during operation to provide modulation and phase shifting designs.

This device includes a Master Reset signal that disables the outputs into Tristate (Hi-Z) mode, and reset all internal digital circuitry (excluding the PLL).

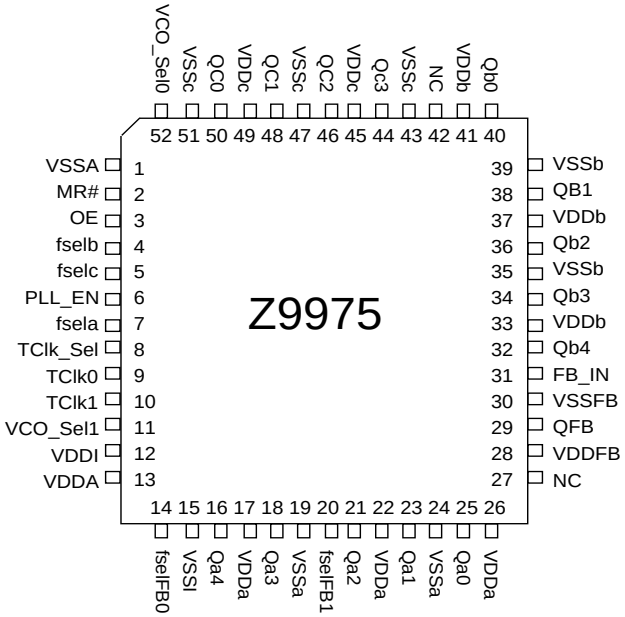
An Output Enable, OE, input pin is available for shutting Qa(0:4), Qb(0:4), and Qc(0:3) outputs in a low state. All outputs are held low with input clock turned off.

Feedback Ratio Selection Table

Inputs				Outputs
VCO_Sel1	VCO_Sel0	fselFB0	fselFB1	QFB
0	0	0	0	VCO/8
0	0	0	1	VCO/12
0	0	1	0	VCO/16
0	0	1	1	VCO/24
0	1	0	0	VCO/16
0	1	0	1	VCO/24
0	1	1	0	VCO/32
0	1	1	1	VCO/48
1	0	0	0	VCO/4
1	0	0	1	VCO/6
1	0	1	0	VCO/8
1	0	1	1	VCO/12
1	1	0	0	VCO/8
1	1	0	1	VCO/12
1	1	1	0	VCO/16
1	1	1	1	VCO/24

Table 1

Pin Configuration



Block Diagram

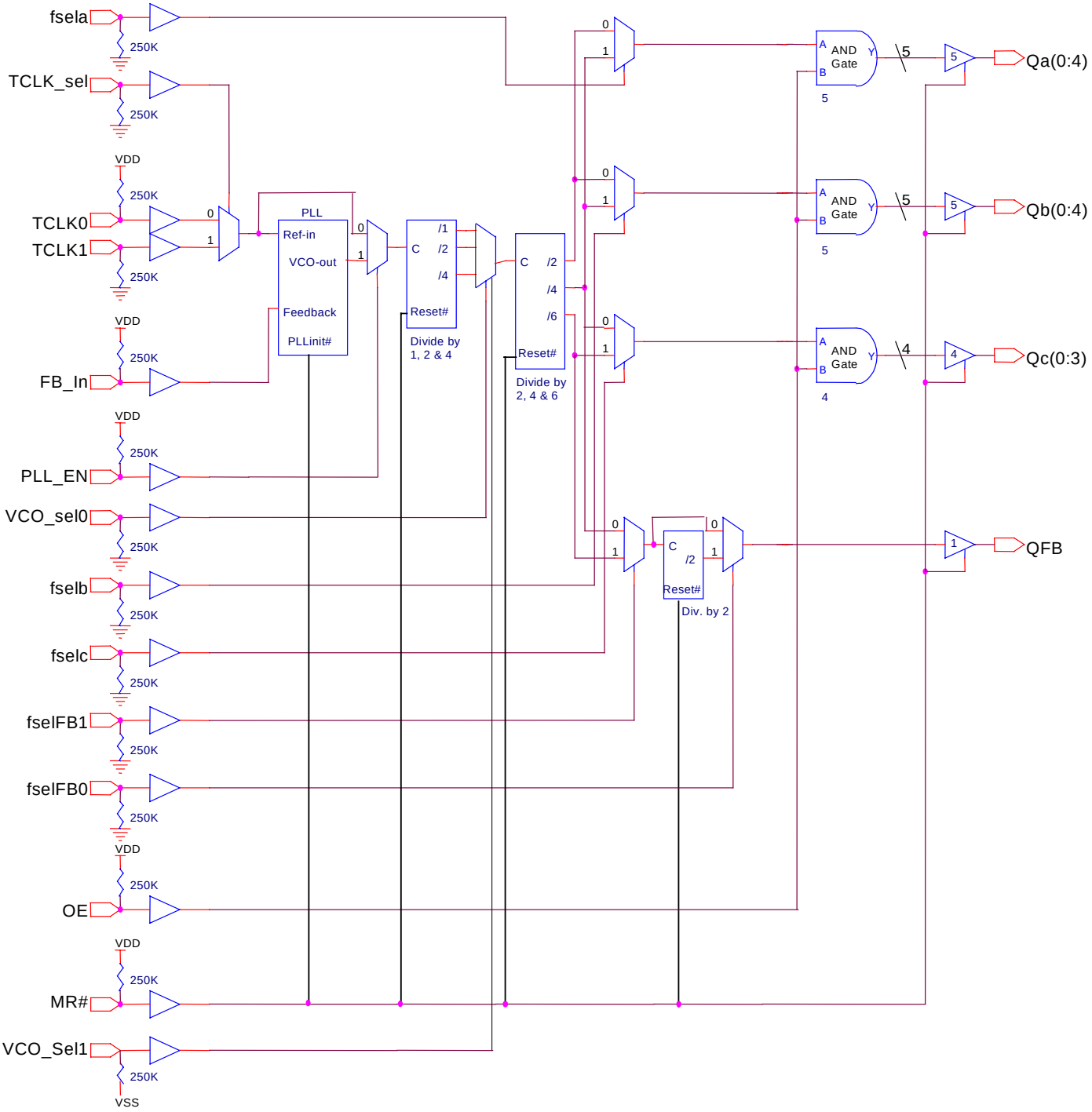


Fig.1

Output Frequency Selection Table (VCO_Sel1 = 0)

Inputs				Outputs		
VCO_sel0	fsela	fselb	fselc	Qa(0:4)	Qb(0:4)	Qc(0:3)
0	0	0	0	VCO/4	VCO/4	VCO/8
0	0	0	1	VCO/4	VCO/4	VCO/12
0	0	1	0	VCO/4	VCO/8	VCO/8
0	0	1	1	VCO/4	VCO/8	VCO/12
0	1	0	0	VCO/8	VCO/4	VCO/8
0	1	0	1	VCO/8	VCO/4	VCO/12
0	1	1	0	VCO/8	VCO/8	VCO/8
0	1	1	1	VCO/8	VCO/8	VCO/12
1	0	0	0	VCO/8	VCO/8	VCO/16
1	0	0	1	VCO/8	VCO/8	VCO/24
1	0	1	0	VCO/8	VCO/16	VCO/16
1	0	1	1	VCO/8	VCO/16	VCO/24
1	1	0	0	VCO/16	VCO/8	VCO/16
1	1	0	1	VCO/16	VCO/8	VCO/24
1	1	1	0	VCO/16	VCO/16	VCO/16
1	1	1	1	VCO/16	VCO/16	VCO/24

Table 2

Output Frequency Selection Table (VCO_Sel1 = 1)

Inputs				Outputs		
VCO_sel0	fsela	fselb	fselc	Qa(0:4)	Qb(0:4)	Qc(0:3)
0	0	0	0	VCO/2	VCO/2	VCO/4
0	0	0	1	VCO/2	VCO/2	VCO/6
0	0	1	0	VCO/2	VCO/4	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/6
0	1	0	0	VCO/4	VCO/2	VCO/4
0	1	0	1	VCO/4	VCO/2	VCO/6
0	1	1	0	VCO/4	VCO/4	VCO/4
0	1	1	1	VCO/4	VCO/4	VCO/6
1	0	0	0	VCO/4	VCO/4	VCO/8
1	0	0	1	VCO/4	VCO/4	VCO/12
1	0	1	0	VCO/4	VCO/8	VCO/8
1	0	1	1	VCO/4	VCO/8	VCO/12
1	1	0	0	VCO/8	VCO/4	VCO/8
1	1	0	1	VCO/8	VCO/4	VCO/12
1	1	1	0	VCO/8	VCO/8	VCO/8
1	1	1	1	VCO/8	VCO/8	VCO/12

Table 3

Pin Description

PIN No.	Pin Name	I/O	Description
2	**MR#**	I	Active low Master Reset pin. It has a 250KΩ internal pull-up. When forced low, all outputs are Tri-stated (high impedance) and internal ratio dividers are reset.
3	**OE**	I	Active high Output Enable pin. It has a 250KΩ internal pull-up. When forced low, Qa(0:4), Qb(0:4), and Qc(0:3) outputs are stopped in a low state. QFB is not effected by this signal.
7,4, 5	**Fsel(a,b,c)**	I	Input select pins for setting the output dividers at Qa(0:4), Qb(0:4), and Qc(0:3) respectively. Each pin has an internal 250KΩ pull-down. See table 2, page 3.
6	**PLL_EN**	I	Input pin for bypassing the PLL. It has an internal 250KΩ pull-up. When forced low, the input reference clock (applied at TCLK0, or TCLK1) bypasses the PLL and drives the dividers, typically for device testing. In this case, the PLL is disabled.
8	**TCLK_sel**	I	Input pin for selecting TCLK0 or TCLK1 as input reference. When TCLK_sel = 0, TCLK0 is selected, when TCLK_sel = 1, TCLK1 is selected. This pin has a 250KΩ internal pull-down.
9,10	**TCLK(0:1)**	I	Input pins for applying a reference clock to the PLL. The active input is selected by TCLK_sel, pin# 8. TCLK0 has a 250KΩ internal pull-down. TCLK1 has a 250KΩ internal pull-up.
14, 20	**FselFB(0:1)**	I	Input select pins for setting the Feedback divide ratio at QFB output, pin#29. See table 1, page1. Each of these pins has a 250KΩ internal pull-down.
25,23,21, 18,16	**Qa(0:4)**	O	High drive, Low Voltage CMOS, Output clock buffers, Bank Qa. Their divide ratio is programmed by fsela, pin#7.
29	**QFB**	O	Low Voltage CMOS output feedback clock to the internal PLL. The divide ratio for this output is set by fsleFB(0:1). A delay capacitor, or trace may be applied to this pin in order to control the Input Reference/Output Banks phase relationship.
31	**FB_In**	I	Feedback input pin. Typically connects to the QFB output for accessing the Feedback to the PLL. It has a 250KΩ internal pull-up.

Pin Description (Cont.)

PIN No.	Pin Name	I/O	Description
11	**VCO_Sel1**	I	Output Division Selection contains an internal pulldown resistor. When left floating or pulled to VSS (Logic 0) output frequencies are described by Output Frequency Table 2, when driven to VDD (Logic 1), output frequencies are described by Table 3.
40,38,36, 34,32	**Qb(0:4)**	O	High drive, Low Voltage CMOS, Output clock buffers, Bank Qb. Their divide ratio is programmed by fselb, pin#4.
50,48,46, 44	**Qc(0:3)**	O	High drive, Low Voltage CMOS, Output clock buffers, Bank Qc. Their divide ratio is programmed by fselc, pin#5.
52	**VCO_Sel0**	I	Input select pin for setting the divider of the VCO output. It has a 250KΩ internal pull-down. If VCO_sel = 0, then the PLL VCO output is divided by 2. If VCO_sel = 1, then the PLL VCO output is divided by 4. See fig.1, page2; table 1, page1, table 2, page 3.
27,42	**n/c**	-	These pins are not connected internally. They may be attached to a ground plane.
12	**VDDI**	P	Power for input logic circuitry.
15	**VSSI**	P	Ground for input logic circuitry.
13,	**VDDA**	P	Power and Ground supply pins for internal Analog circuitry.
17,22,26	**VDDa**	P	3.3V supply for Qa(0:4) output bank, and fselFB1 input.
19,24	**VSSa**	P	Common ground for Qa(0:4) output bank, and fselFB1 input.
28, 30	**VDDFB / VSSFB**	P	Power and ground supply pins for QFB output and FB_In input pins and digital circuitry.
33,37,41	**VDDb**	P	3.3V supply for Qb(0:4) output bank.
35,39	**VSSb**	P	Common ground for Qb(0:4) output bank.
45,49	**VDDc**	P	3.3V supply for Qc(0:3) output bank and VCO_sel pin.
43,47,51	**VSSc**	P	Common ground for Qc(0:3) output bank and VCO_sel pin.
1	**VSSA**	P	Analog Ground

A bypass capacitor (0.1µF) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductances of the traces.

Glitch-Free Output Frequency Transitions

Customarily when zero delay buffers have their internal counter's changed "on the fly' their output clock periods will:

A. Contain short or "runt" clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequency that is being transitioned to.
B. Contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequency that is being transitioned to.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed "on the fly" while it is operating: Fsela, Fselb, Fselc, VCO_Sel, FselFB1, and FselFB2.

Maximum Ratings

Input Voltage Relative to VSS:	VSS-0.3V
Input Voltage Relative to VDD:	VDD+0.3V
Storage Temperature:	-65°C to + 150°C
Operating Temperature:	-40°C to +85°C
Maximum Power Supply:	5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	VSS	-	0.8	Vdc	Applicable to all input signals.
Input High Voltage	VIH	2.0	-	VDD	Vdc	
Input Low Current	IIL			-100	µA	
Input High Current	IIH			100	µA	
Output Low Voltage	VOL			0.5	V	IOL = 20 mA
Output High Voltage	VOH	2.4			V	IOH = - 20mA
Quiescent Supply Current	Idd	-	-	20	mA	
Input Pin Capacitance	Cin	-	-	8	pF	Per input
VDD* =3.3V ± 5%, TA = -40°C to +85°C						

PLL AC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Maximum PLL Lock Time	tLOCK			10	mS	Stable power supply & valid clocks presented on TCLK(0:1) pins.
VCO Lock Range	fVCO	200		500	MHz	FselFB(0:1) = /4 to /12
TCLK(0:1) input rise / fall time	Tinr, Tinf			3	nS	
Input Reference frequency	fREF	Note 1		Note 1	MHz	
Input Reference duty cycle	fREFpw	25		75	%	
VDD* = 3.3V ± 5%, TA = -40°C to +85°C						

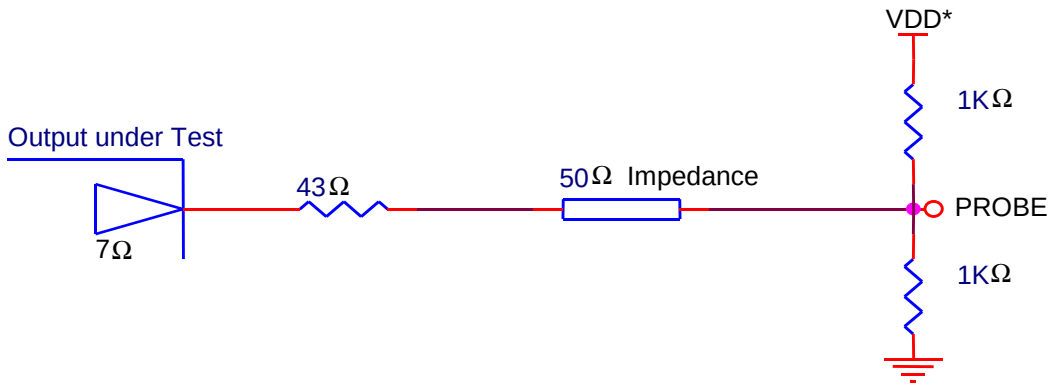
Note 1: Input Reference Frequency is limited by the divider selection and the VCO lock range.

AC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	Tpw	Tcycle/2 - 800	Tcycle/2 ± 500	Tcycle/2 + 800	ps	Measured @ VDD/2
Rise Time / Fall Time	T_r, T_f	0.15	-	1.5	ns	Measured between 0.8V and 2.0V
Output Impedance	Z_o		7	10	Ω	
Output to Output Skew	T_s	-	-	250	ps	All output equally loaded
Propagation Delay, TCLK(0:1) to FBIN	T_{pd}	-250	-	100	ps	Measured for 50MHz at VDD/2
Cycle to Cycle Jitter	tj	-	±100	-	ps	Measured for 50 MHz at VDD/2
Output Disable Time	tPLZ, tPHZ	2	-	10	ns	After MR# goes low
Output Enable Time	tPZL	2	-	10	ns	After MR# goes High
Maximum Output Frequency	Fout	-	-	150	MHz	Q (÷2)
		-	-	125		Q (÷4)
		-	-	83		Q (÷6)
VDD* = 3.3V ± 5%, TA = -40°C to +85°C						

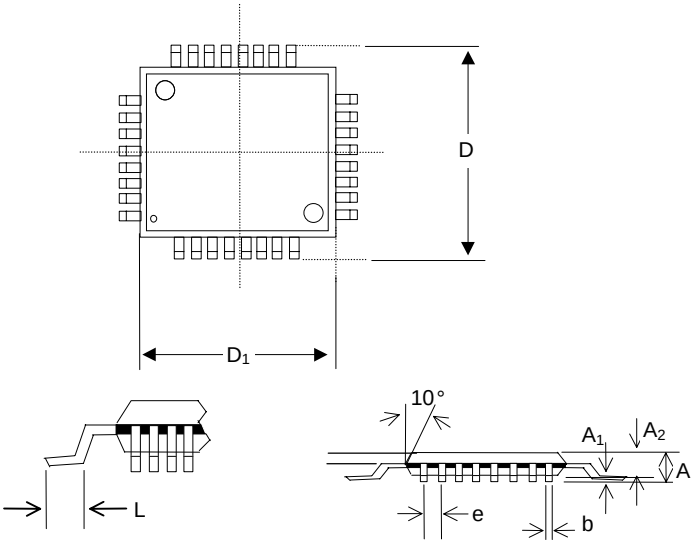
Note: Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs. Z9975 outputs can drive series or parallel terminator 50 Ω (or 50 Ω to VDD/2).

Test Circuit Diagram



NOTE: All buffer outputs are tied to a common 3.3 Volt VDD (VDD*) for testing purposes

Package Drawing and Dimensions (52 TQFP)



52 Pin TQFP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.472	-	-	12.00	-
D_1	-	0.394	-	-	10.00	-
b	0.009	-	0.015	0.22	-	0.38
e	0.026 BSC			0.65 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
Z9975CA	52 TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
Z9975CA
Date Code, Lot #

Z9975CA

- Package: A = TQFP
- Revision
- IMI Device Number

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Document Title: Z9975 3.3V, 150 MHz Multi-Output Zero Delay Buffer
Document Number: 38-07091

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107127	06/05/01	IKA	Converted from IMI to Cypress
*A	108069	07/03/01	NDP	Changed Commercial to Industrial