Frequently Asked Questions about the RoboClockII™ Family

The following questions are frequently asked by customers who are using devices in the RoboClock® family. The RoboClockII family consists of the CY7B993V and CY7B994V. The following are brief answers to sometimes complicated questions. More detailed application notes will be compiled on the more important topics and posted to the 'web when completed.

1. How do I use RoboClockII to multiply a frequency?

RoboClock is a Phase-Locked Loop (PLL) based clock buffer with the added flexibility of programmable output skew and divide. The PLL is a circuit that synchronizes an output (generated by an internal oscillator) with the reference (REF) input. If a divided output is applied to the feedback (FB) input, it will cause the internal VCO (voltage controlled oscillator) to operate at the divided factor times the reference frequency. For example, if one is a 20-MHz reference input and an output that has been configured for divide-by-two (/2) is connected to the feedback input, the internal VCO has to operate at twice the reference frequency in order to align the REF and FB inputs. Thus, applying a divided feedback configures RoboClock as a frequency multiplier.

2. Can I use an external divider in my feedback loop?

The RoboClockII (CY7B993/4V) has internal divide capability of up to divide-by-twelve. If a higher divide ratio is needed, it is possible to use external dividers in the feedback path. However, large dividers or dividers that have an inherently long delay should be used cautiously. There are some constraints that should be followed. A large divider ratio can cause the phase detector update gaps to become excessively large. As a "rule of thumb" the maximum divider ratio in the feedback path should be less than 16. Larger values are not recommended. The maximum time delay permitted in the external feedback loop is 10 ns.

3. The data sheet shows the maximum of the CY7B994V FS HIGH range as 200 MHz but the f_{OUT} specification has a 185 MHz maximum. Is there a contradiction here?

No. The maximum output frequency allowed with RoboClockII is 185 MHz. However, the internal VCO is allowed to run up to 200 MHz. For example, you could have a reference input of 20 MHz with a /10 FB. The internal VCO would be operating at 200 MHz. In this scenario a /1 output is illegal since that would require the output buffer to operate at 200 MHz. The minimum divide ratio on the output banks in this instance would be /2.

4. Are there any board layout recommendations for RoboClockII?

A separate application note is planned that will cover this topic in more detail at a later date. However, the following guidelines were employed by Cypress Semiconductor when creating their evaluation boards for RoboClockII:

1. Connect the V_{CCQ} and V_{CCN} pins to the same uncut power plane.
2. A top layer ground pour is recommended underneath the package. Connect this ground pour to the internal ground plane through several vias. Connect all ground pins to the center ground pour.
3. For each V_{CC} pin, place a capacitor as close as possible on the same side as the chip with a short thick trace connecting the pin and one end of the capacitor. This is then connected to the V_{CC} plane through a via (see *Figure 1*).
4. Try to assign a capacitor for each V_{CCQ}.
5. Decouple the center ground plane with 0.01uf capacitors on the bottom side of the ground pour (see *Figure 2*).
6. The above discussion assumes that generally accepted layout principles such as using controlled impedance traces for all the outputs signals, transmission line termination, etc. have been employed.

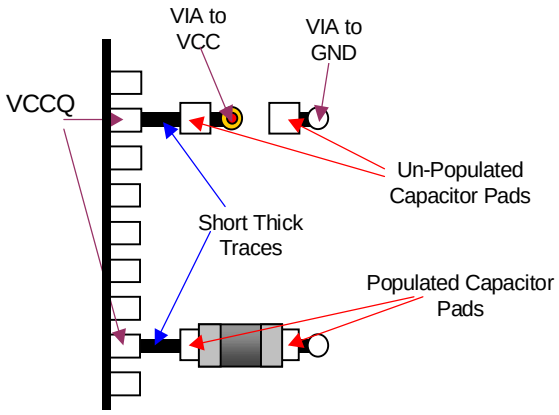

Figure 1. V_{cc} Pin Bypassing Scheme.

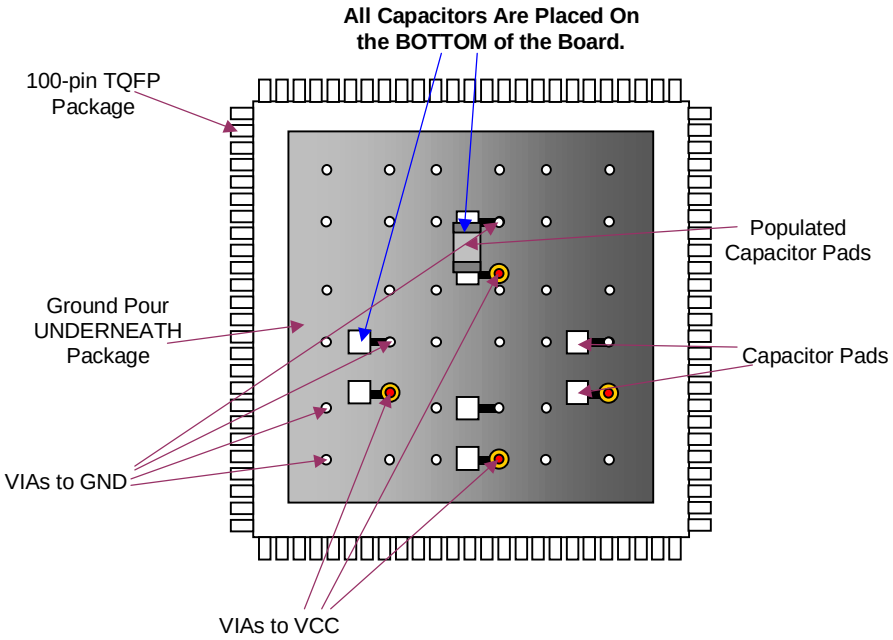

Figure 2. Ground Pour Decoupling.

5. How do I achieve a 90-degree offset? How can I use an external divider to achieve a 90-degree offset independent of frequency?

The simplest way to achieve a 90-degree phase shift is to use the programmable skew functionality of RoboClockII. An exact offset of 90 degrees is available when the FS pin is in any one of the three speed ranges for the CY7B994V. For the CY7B993V exact offset of 90 degrees is available when FS pin is in the MID and HIGH state. The period of the output is

divided into different amounts of time units (t_U) for each setting of the FS pin. *Table 1* shows that the number of time units per output period per each FS state is different for the CY7B993V and CY7B994V.

Table 1. Total time unit (tu) per $OUTPUT_{period}$

FS	CY7B993V	CY7B994V
LOW	$64t_U$	$32t_U$
MID	$32t_U$	$16t_U$
HIGH	$16t_U$	$8t_U$

A 90 degree offset is the $OUTPUT_{period}$ / 4. *Table 2* shows the required skew offset to implement 90 degree offset.

Table 2. Time unit for 90 Degree Offset

FS	CY7B993V	CY7B994V
LOW	$\pm16t_U$	$\pm8t_U$
MID	$\pm8t_U$	$\pm4t_U$
HIGH	$\pm4t_U$	$\pm2t_U$

The offset of $\pm2t_U$, $\pm4t_U$, and $\pm8t_U$ is achievable by simply programming the output to have the respective skew with specific FS settings (refer to the RoboClockII data sheet for programmable skew settings). The offset of $16t_U$ between two outputs when FS is LOW when using the CY7B993V can be achieved in two ways:

1. If the 90 degree phase relationship is only required between two banks of outputs and neither bank have to be 0 degree phase relative to the reference clock, then $16t_U$ of phase offset can be achieved by programming a bank of output to $-8t_U$ and the other bank of outputs to $+8t_U$. Then the phase relationship between these two banks of outputs will be $16t_U$.
2. If the reference clock must coincide with one of either 90 degree offset outputs, then a skewed feedback must be used. For example, bank3 is configured to $+8t_U$ and fed back to the FBA+ input. So all output banks with +8tu setting will be in phase with the input reference. All phase relationships and programmability are still preserved between banks; so bank4 can be configured to $-8t_U$ to obtain –90-degree offset with respect to bank3 and the reference input. For +90 degree offset, a $-8t_U$ output is required for feedback. Consequently, a bank not used for feedback can be programmed to $+8t_U$ skew to obtain +90-degree offset.

The second case described above also shows that NOT ONLY the feedback bank outputs can be used to drive the feedback inputs; ANY outputs on the RoboClockII can be used for feedback. This greatly expands the combination of configurations of the RoboClockII.

6. What do I do with unused outputs?

The outputs of RoboClockII are designed such that there is little or no interference between banks of outputs. Thus, you can either leave unused outputs floating or terminate them as per the data sheet load. Outputs that are not terminated can inflict up to 30 ps skew on adjacent outputs. Terminated outputs will use more power due to the recommended thevenin termination network. However, terminated outputs are likely to be less noisy. Alternatively, a bank of unused outputs can be disabled for aggressive power management.

7. Can RoboClockII outputs be divided and skewed at the same time?

Yes, the RoboClockII outputs can be programmed to divide from 1-12 (except 7, 9, and 11) and at the same time skewed to the desired time unit. The divide function and skew function of an output bank are independent of each other.

8. Is RoboClockII 3.3V-compatible? How about 2.5V compatibility?

The RoboClockII (CY7B993/4V) is completely 3.3V-compatible.

The RoboClockII requires a 3.3V V_{CC} supply. However, it is possible to make the output swing 2.5V compatible. *Figure 3* below shows a termination network that makes RoboClockII compatible with 2.5V systems.

The termination shown in *Figure 3* is a totem pole termination network. The reader must note that this termination network acts as a voltage divider, thus all AC measurements that are originally referenced to 1.5V will be scaled down to reference at 1.07V (1.5V * 0.71) for the 2.5V-compatible output.

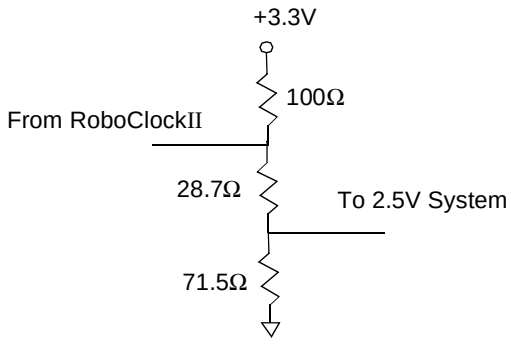

Figure 3. Typical 50Ω Termination to 3.3V for 2.5V-Compatible RoboClockII Outputs

9. What is the phase relationship between divided outputs?

All banks of the RoboClockII are capable of divide-by-one to twelve with the exception of divide-by-seven, nine and eleven. The relationship between divided outputs are rising (positive) edge aligned. This is a major difference between the first generation RoboClock and RoboClockII.

First generation RoboClock Family parts were capable of divide-by-two and divide-by-four only, and divided outputs are negative (falling) edge aligned. By having the falling edges of the /2 and /4 clocks aligned, the rising edges are spaced farther in time. If it is assumed that most logic is rising edge triggered, this makes the design more robust to jitter, skew problems, and loading effects. This trade-off is important because the divided outputs of first-generation RoboClock are not skewable.

On the other hand, RoboClockII divided outputs are rising edge aligned. It was designed with the same base assumption in mind. The trade-off between skew and divide functions no longer exists in RoboClockII. Each bank of outputs of the RoboClockII can be divided AND skewed at the same time. This extra degree of control can greatly improve system performance and allow more innovative system design.

10. The data sheet states that RoboClockII has "selectable reference input ... which allows smooth change over to a secondary clock source." What does this mean? Will the part automatically switch to the second reference input if the primary reference input goes dead?

The selectable reference scheme offered by RoboClockII provides the designer with the ability to select between two possible reference sources. This is useful for systems that route a secondary clock source to the system for testing or redundancy purposes. The reference source applied to RoboClockII is dictated by the REF_SEL pin. If the primary clock goes dead the part will NOT automatically select the secondary source.

RoboClockII was specifically designed to provide 'smooth' changeover when swapping between the two reference sources. If the REF_SEL pin is toggled, the part detects this and continues to provide output frequencies identical to the previously locked frequency for a short time. The part will then lock onto the new reference source and smoothly change from the previously locked frequency to the new reference source.

11. Why do we have two reference and two feedback inputs?

RoboClockII provides two reference inputs for redundancy purposes. The second feedback input is included to provide more flexibility. This enables the user to supply two feedback signals, that can have different divide and skew characteristics, to the part. The user can then select between the feedback inputs based on the operating requirements of the design.

12. How should the differential reference and feedback input be connected?

RoboClockII has two mux-able reference and feedback inputs (REFA and REFB; FBKA and FBKB). Each reference or feedback input is capable of receiving a differential mode signal or a single-ended mode signal. The required input is selected by (REFSEL) FBSEL. When LOW, (REFA) FBKA is selected. These inputs have an internal pull-down resistor, therefore, when it is left open, the (REFA) FBKA input is automatically selected.

Each input consists of two input pins; a "+" input and a "–" input, e.g., FBKA+ and FBKA–. When connecting to the input in single-ended mode, the output signal can be connected to either the "+" pin or the "–" pin; then the other input pin must be left open. In this case, the input becomes a normal LVTTL input with a threshold voltage of 1.5V. When the signal is connected to the "+" pin, then it is the same as connecting to any single-ended input and the polarity of the signal is preserved. When the signal is connected to the "–" pin, then the polarity of the input signal is inverted.

When the inputs are differential, the negative input (e.g., FBKA–) becomes the reference for the positive input (e.g., FBKA+) and this enables RoboClockII to accept PECL inputs. The minimum differential voltage swing (V_{DIFF}) and the common mode range (V_{COM}) specifications in the data sheet provide enough flexibility to allow RoboClockII to accept HSTL, LVDS, and SSTL inputs.

Any RoboClockII output can be connected to the feedback input; it is NOT limited to the QFA0 or QFA1 outputs only. When directly feeding back a RoboClockII output to the selected feedback input, the single-ended mode configuration is used. Generally, the output used for feedback is connected to the "+" input pin.

13. Can RoboClockII drive differential loads?

Bank3 can be configured into two pairs of differential outputs by setting the INV3 pin LOW (gnd). In this mode each matched output pair becomes complementary ([3QA0+, 3QA1–] and [3QB0+, 3QB1–]). The output buffers of Bank3 are designed to have matched delay, pulse width and rise/fall times to emulate a real differential output. While RoboClockII outputs are LVTTL, LVPECL is a 1V logic centered about $V_{CC}/2$ and so RoboClockII outputs represent a superset of PECL. If the line receiver has no maximum voltage swing limit then the outputs will be sufficient to drive PECL loads. If the line receiver has a 1V nominal swing, then a combination of series and parallel termination on the line will make them compatible.

14. What effect does slow rise and fall times on the REF input have on RoboClock operation?

A slow rise time affects the apparent t_{PD}, which is the propagation delay (REF rise to FB rise). t_{PD} is measured at an arbitrary, but standard, 1.5V. The actual threshold voltage (V_{TH}) of REF and FB will vary around 1.5V ($0.8v<V_{TH}<2.0V$) depending upon V_{CC}, temperature and process variation. This change in V_{TH} will affect t_{PD}. For example, if the input ramp rate is approximately 1 V/ns then 100 mV variation in V_{TH} will change the apparent t_{PD} of the REF and FB input gate by approximately 100 ps. This is normally not a problem, since both FB and REF are threshold matched and are driven by similar edge rates.

If the REF ramp rate is much longer than FB, then this "apparent" t_{PD} variation will show up as increased (or decreased) t_{PD} through the RoboClockII. Actually (disregarding the minimal effect of edge rate on V_{TH}) the t_{PD} does not change. Only the measurement changes. The propagation delay from the time REF begins to rise, until the time when the output begins to rise, will look like it is increasing with a slower REF rise rate or with increasing REF V_{TH}. In reality, when measured at the 'actual' V_{TH}, t_{PD} is constant.

Another possible effect of slow rise and fall times could be introduced jitter. This is due to the increased amount of time that the input is near the threshold voltage. At threshold, the input buffer is much more sensitive to variations and noise.

15. What's the difference between the two disable states?

RoboClockII offers the user two disable options; HI-Z and HOLD-OFF. The part is disabled by putting the respective bank DIS pin HIGH. These DIS inputs have an internal pull-down. Once the DIS pin has been set HIGH, the actual disable state is determined by the OUTPUT_MODE setting. This is shown in *Table 3*. When a bank of outputs is disabled to the HI-Z state, the outputs will go HI-Z immediately. An output bank disabled to the HOLD-OFF state will do so after a maximum of 6 output clock cycles from the time the respective DIS pin is HIGH. In this state, non inverting outputs will drive LOW on their falling edge and inverting outputs will drive HIGH on their rising edge. This insures that disabled outputs are stopped or re-started, at the expected time, without narrow pulses.

Table 3. DIS[1:4]/FBDIS Pin Functionality

OUTPUT_MODE	DIS[1:4]/FBDIS	Output Mode
HIGH	HIGH	HI-Z
LOW		HOLD-OFF

16. How are the three level control pins programmed in RoboClock?

For all three state inputs, HIGH indicated a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal circuitry holds an unconnected input to Vcc/2 with internal pull-up and pull-down resistors.

17. What are the required voltage levels of a three level input? How do you model a three-level input?

The voltage levels are V_{IHH}, V_{IMM}, and V_{ILL} on the data sheet. The ranges for the CY7B993/4V are from $0.87*V_{CC}$ to V_{CC} for V_{IHH}, from $0.47*V_{CC}$ to $0.53*V_{CC}$ for V_{IMM}, and 0.0V to $0.13*V_{CC}$ for V_{ILL}. These values guarantee that the correct value will be detected. The actual thresholds (high threshold = V_{THH}, low threshold = V_{THL}) will be between the specified ranges,

as shown in *Figure 4*. The voltage thresholds of typical silicon are also shown here. A MID input will typically be detected anywhere from 1.2V to 2.2V, for a 3.3V V_{CC}.

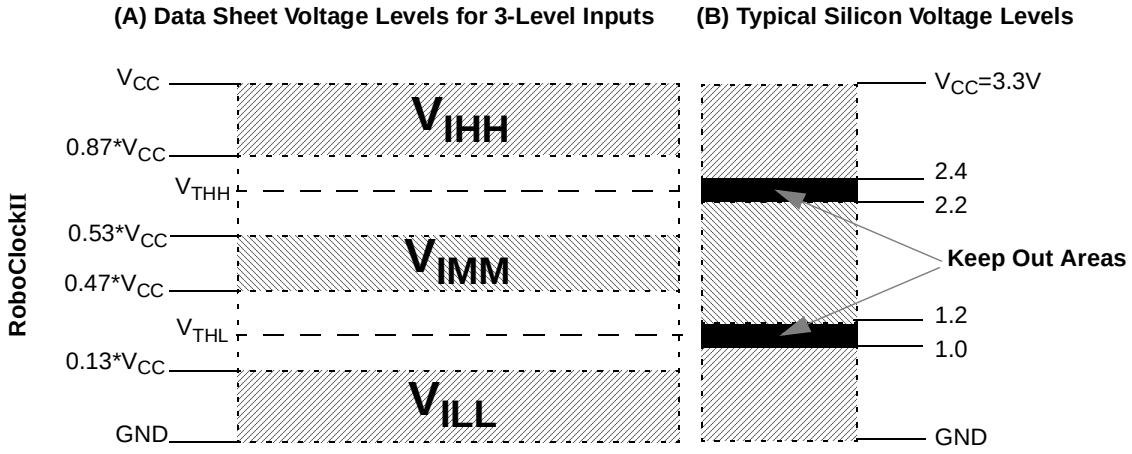

Figure 4. Voltage Levels for 3-Level Inputs

The three-level inputs of the RoboClockII family can be modeled by a pull-up and pull-down resistor. The internal resistor values for the three-level inputs are approximately a 30-KΩ pull-up and 30-KΩ pull-down. This is shown in *Figure 5*.

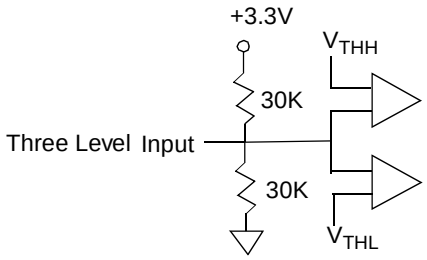

Figure 5. Simplified Internal Pull-Up/Down Resistors of a Three-Level RoboClock Input with Threshold Detection

18. Are there any considerations to be mindful of when driving the 3-level inputs with a tri-state buffer?

It is possible to drive RoboClockII with a tri-state buffer. However, it is important that the I_{OZ} specification of the tri-state buffer be less than the I_{IMM} of RoboClockII. It will be necessary to include 1KOHM pull-up and pull-down resistors on the 3-level inputs of RoboClockII when driving the part with a tri-state buffer if the I_{OZ} specification violates the VIMM specification of RoboClockII.

19. What's the maximum skew I can achieve with RoboClockII?

The skew granularity available with RoboClock is dependent on (1) the part (993 or 994) employed, (2) the FS setting and (3) the operating frequency of the VCO, fNOM. The output skew is programmed through the Skew Function Select Pins, [1:4]F1, [1:4]F0 and FBF0. The RoboClockII skew functionality is dictated in *Table 5*. The time unit (t_U) calculation is illustrated in *Table 4*. The maximum skew granularity is available when a CY7B993V is operating in the FS=LOW range with an fNOM=12MHz. In this instance the t_U is1.3ns. If we configure the bank used for feedback for -8t_U (-10.4ns) and configure

one of the other banks for +8t_U, then the total skew appearing on the bank configured for +8t_U is 10.4-(-10.4)ns=20.8ns. The minimum skew is available when a 994 is operating with an fNOM of 200MHz. The t_U in this instance will be 625ps.

Table 4. N Factor Determination

	CY7B993V		CY7B994V	
FS	N	f_{NOM} (MHz) at which t_U =1.0 ns	N	f_{NOM} (MHz) at which t_U =1.0 ns
LOW	64	15.625	32	31.25
MID	32	31.25	16	62.5
HIGH	16	62.5	8	125

20. What's the difference between the feedback (FB) bank and the 4 other banks?

RoboClockII outputs are divided into five banks. Four of the banks have two pairs of outputs and one bank, the feedback bank, has one pair of outputs. The feedback bank is so called because of its proximity to the feedback inputs. This pair of outputs has the same functionality as all other outputs except that it has limited skew capability. This is illustrated in *Table 5*. Any of the 18 outputs can be used as the feedback input.

Table 5. Output Skew Select Function

Function Selects		Output Skew Function				
[1:4]F1	[1:4]F0 and FBF0	Bank1	Bank2	Bank3	Bank4	Feed-back Bank
LOW	LOW	–4t_U	–4t_U	–8t_U	–8t_U	–4t_U
LOW	MID	–3t_U	–3tu	–7t_U	–7t_U	NA
LOW	HIGH	–2t_U	–2t_U	–6t_U	–6t_U	NA
MID	LOW	–1t_U	–1t_U	BK1[1]	BK1[1]	NA
MID	MID	0t_U	0t_U	0t_U	0t_U	0tu
MID	HIGH	+1t_U	+1t_U	BK2[1]	BK2[1]	NA
HIGH	LOW	+2t_U	+2t_U	+6t_U	+6t_U	NA
HIGH	MID	+3t_U	+3t_U	+7t_U	+7t_U	NA
HIGH	HIGH	+4t_U	+4t_U	+8t_U	+8t_U	+4t_U

21. How do I put RoboClockII into TEST mode?

RoboClockII is put in TEST mode by setting the OUTPUT_MODE pin MID. In TEST mode the part operates with its internal PLL disconnected. In TEST mode the selected FB input(s) must be tied LOW. All functions of the device are still operational in TEST mode except the internal PLL and output bank disables. Obviously, the internal PLL cannot achieve LOCK in TEST mode so the LOCK pin is indeterminate in this state.

22. How slow can REF go in TEST mode?

There is no lower limit for the REF frequency in factory TEST mode. This is because in TEST mode the internal PLL is by-passed and the input levels supplied to REF directly control the internal logic. The input signal applied to REF will drive the internal state machine.

Note:
1. BK1, BK2 denotes following the skew setting of Bank1 and Bank2 respectively

23. How do I determine the expected output frequency in TEST mode?

In TEST mode the REF input takes the place of the VCO output. Thus, the output frequency of the part in TEST mode is the REF frequency divided by whatever dividers are in the path between the VCO output and the output buffer itself. This divide ratio is made up of two components; the internal divide function and the selected external divide ratio for which the output bank is configured. The internal divide ratio is dependent on the part employed (993 or 994) and the FS setting. The divide ratios for the various configuration are illustrated in *Table 6*. The effect of the internal divide ratio must be coupled with the programmed divide ratio for the particular bank. For example, if you had a CY7B994V operating with FS HIGH, the internal divide ratio is 4 per *Table 6*. Now if you configured one of the banks for divide-by-5, the output frequency in TEST mode would be fREF/(4*5)=fREF/20. For a 20-MHz input, the output of this bank would be 1 MHz in TEST mode.

Table 6. TEST Mode Internal Divide Ratios

FS	Internal Divide Ratio	
	CY7B993V	CY7B994V
LOW	32	16
MID	8	4
HIGH	16	8

24. Does the skew function work in TEST mode?

Yes, the normal skew capability of RoboClockII is still available in TEST mode. However, the skew granularity calculation is slightly different. When in TEST mode, a one-REF input period will translate to $2t_U$ for skewed outputs. The positive width of the reference clock cycle is equal to the first time unit and the negative pulse width is equal to the second time unit. Thus, if the reference clock duty cycle is 50%, then half a clock period will be equal to $1t_U$. This is shown in *Figure 6*.

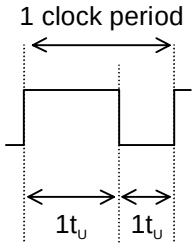

Figure 6. Time Unit Calculation in TEST Mode

25. Why does the LV differential input spec (VIHHP, VILLP) overlap?

As discussed earlier, the reference inputs and feedback inputs are capable of receiving differential signals. The input specifications VIHHP and VILLP describe the Highest Input HIGH Voltage and Lowest Input LOW Voltage when these input buffers are operating in differential mode. It may be confusing to the user that these two input specs overlap each other. When these inputs are used as differential inputs, it is a fact that when the "+" input is HIGH then the "–" input must be LOW, and vice versa. The VIHHP spec describes the possible voltage range of the HIGH input, and the VILLP spec describes the possible voltage range of the LOW input. The reason for the overlap of the specs is that these inputs can accommodate a wide range of differential voltage (400 mV up to V_{CC}) over a wide common mode range (800 mV to V_{CC}–0.4). Here we define the

common mode range as the voltage at which the "+" and "–" input crosses. *Figure 7* depicts the different extreme but legal input scenarios:

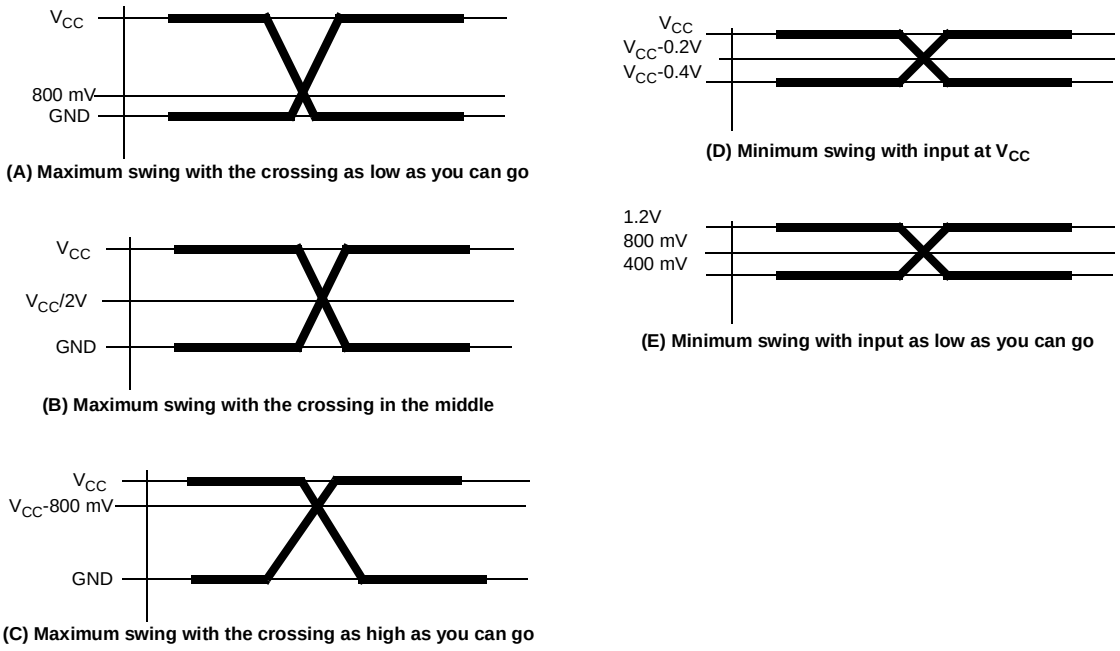

Figure 7. Extreme Differential Input Scenarios

26. What do all the different skew values on the data sheet mean?

Skew is the difference in time between the transitions of a pair of outputs with a fixed time relationship.The skew values apply to the skew between different outputs of the RoboClockII identically loaded as specified by the data sheet. The skew depends upon the function of the two outputs and in many cases the function of the rest of the outputs.

The outputs of RoboClockII have been carefully designed to control delay and edge rate, in an attempt to minimize skew. Outputs are built as pairs (XQY0 and XQY1) sharing the same drive and power supply. Each RoboClockII output bank has two pairs of outputs (the feedback bank has one pair) which are physically located close to each other for best matching.

Each bank of outputs can also be categorized by their function. The classes are nominal, divided-by-X, divided-by-Y, and inverted. Ideally all edges would occur at 0 ns. However, minor variation in internal delay, output rise and fall delay, adjacent output transition direction, and edge placement (coupling) affect the position of the output transition. The various skew specifications shown in the data sheet attempt to quantify these variations.

t_{SKEWPR}: Zero Output Matched-Pair Skew

This parameter specifies the maximum amount of skew between two outputs of the same pair (e.g., 1QA1 and 1QA0) when all eighteen outputs are selected for $0t_U$.

$t_{SKEWBNK}$: Zero Output Matched-Bank Skew

This parameter specifies the maximum amount of skew between four outputs of the same bank (e.g., 1QA1 and 1QB0) when all eighteen outputs are selected for $0t_U$.

t_{SKEW0}: Zero Output Skew (same frequency and phase, rise to rise, fall to fall)

This parameter specifies the time between the first output edge and the last output edge of all outputs that are selected for the same frequency and phase.

t_{SKEW1}:Output Skew (same frequency and phase, other banks at different frequency, rise to rise, fall to fall)

This parameter specifies the maximum amount of skew between outputs of the same output class selected for the same output skew and same output frequency without restriction on the placement or function of other outputs. The signals to be compared must be same class and must be rising edge to rising edge, or falling edge to falling edge aligned.

t_{SKEW2}:Output Skew (invert to nominal of different banks, compared banks at same frequency, rising edge to falling edge aligned, other banks at same frequency)

This parameter specifies the amount of output skew between the rising or falling edge of a Nominal output and the opposite edge of an Inverted output. All other banks of outputs must be at the same frequency. The outputs that are compared must be rising edge to falling edge aligned.

t_{SKEW3}: Output Skew (all output configurations outside of t_{SKEW1} and t_{SKEW2})

This parameter specifies the amount of output skew for configurations outside of those specified in t_{SKEW1} and t_{SKEW2}.

$t_{SKEWCPR}$: Output Skew (crossing to crossing, complementary outputs of the same bank)

This parameter specifies the maximum time between the crossing-point of one pair of complementary outputs and the other pair of complementary outputs in the same bank. This is different from tSKEWPR because the measurement point is self-relative instead of 1.5V.

t_{PD}:Propagation Delay (REF Rise to FB Rise)

This is a measure of the misalignment between the reference input rise and feedback input rise. It can be either positive or negative.

27. What is the difference between t_{ODCV} (Output Duty Cycle Variation) and t_{PWH}/t_{PWL}?

t_{ODCV} is the deviation of the output from 50% duty cycle measured at 1.5V. t_{PWH}/t_{PWL} is the deviation measured at the corresponding high and low thresholds (t_{PWH} is measured at 2.0V, t_{PWL} is measured at 0.8V). The differences account for rise and fall time “pulse-narrowing” from the 50% point measurement.

28. What are the package options available for RoboClockII?

RoboClockII can be purchased in two different packages. The low frequency part (CY7B993V) is available in a 100-pin TQFP package only. The high frequency unit (CY7B994V) is available in both a 100-pin TQFP and 100-ball Thin Ball Grid Array. The package diagrams and ordering information are available in the data sheet.

29. I need to estimate the reliability in my design. How many components does it contain?

For complete documentation on the reliability of the RoboClockII see the yearly Reliability Report. The most commonly desired reliability information is as follows.

Technology:	0.25µ BiCMOS
Number of components:	7745
Number of transistors:	15000
Number of gates:	3750
Die size:	115 mils x 115 mils
Commercial Theta JC:	TBD degrees C / Watt
Commercial Theta JA:	46.8 degrees C / Watt
Max Junction Temp.:	150 degrees C