Replace MPC973 with RoboClock II

Introduction

Cypress CY7B993 and CY7B994 (RoboClock II) contain a comprehensive feature set that performs a superset of those contained in the Motorola MPC973 and MPC972. Systems that were originally designed around the Motorola part can be upgraded by the substitution of RoboClock II. This application note is divided into sections that step through the issues involved with this conversion.

Comparison of Block Diagrams

The main function of the Motorola part is to provide multiple copies of a few clock frequencies derived from a master reference frequency source. It does this by offering three banks of four outputs and a couple of special-purpose single outputs. The output frequency of each bank is based on a divided version of an internal high-frequency Voltage Controlled Oscillator (VCO) (See *Figure 1*). The '973 has a differential PECL input and a pair of TTL-compatible reference inputs with selectors to choose the source for the internal PLL. The '972 substitutes a Crystal Oscillator for the differential PECL input.

Robo II has four banks of four outputs and one bank of two outputs, which can be configured to mimic the functionality of the Motorola parts (See *Figure 2*. *CY7B993/994 Block Diagram*). The CY7B993 and '994 also have dual reference inputs, which can be configured as differential PECL compatible inputs or as TTL inputs. Robo does not support the internal Crystal Oscillator function found in the MPC972, or the third reference input found in the MPC973.

There are a few differences in the way that Motorola and Robo handle output disable, reset and test modes. For most applications, the differences are minor, and can be handled by the default connections of a few control inputs.

Select the Frequency of Operation

The divider function (and the resulting multiply function) of the Motorola part has been chosen such that the internal VCO operates between 200 and 480 MHz and the output frequency is 125 MHz or less.

RoboClock II has three ranges of frequency operation, which are selected by the FS input. When FS is HIGH (connected to VCC) the internal '994 oscillator operates between 100 and 200 MHz (50–100 MHz on the '993). When FS is MID (floating, or externally pulled to VCC/2) the internal '994 oscillator operates between 50 and 100 MHz (25–50 MHz on the '993). When FS is LOW (connected to GND) the internal '994 oscillator operates between 25 and 50 MHz (12.5 and 25 MHz on the '993).

In RoboClock II the frequency of the internal oscillator will be the same as the frequency of any output configured to "divide

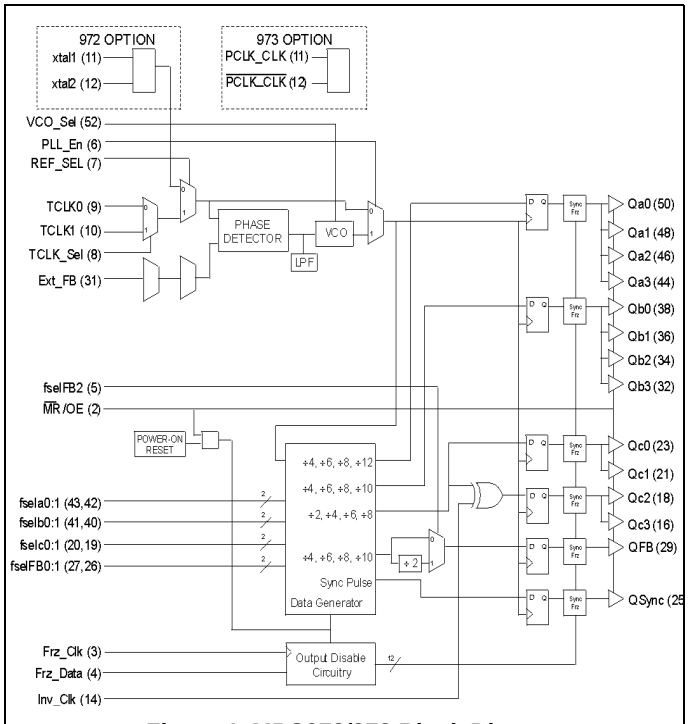


Figure 1. MPC972/973 Block Diagram

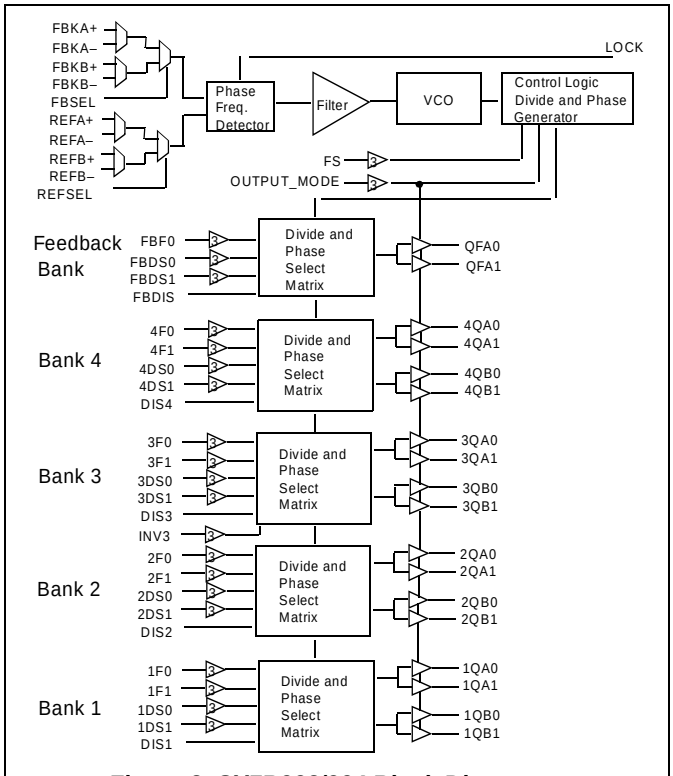


Figure 2. CY7B993/994 Block Diagram

by one". This is in contrast to the Motorola convention where the internal oscillator will run at least four times (or possibly two times) the rate of the output connected to Ext_FB (usually QFB).

Set the Divide Function of Each Bank

The internal dividers in the MPC972/MPC973 can be set to divide by Qa=4,6,8,10, Qb=4,6,8,12, Qc= 2,4,6,8 each using two binary inputs (fsela1:0, fselb1:0, fselc1:0) and QFB=4,6,8,10,12,16,20 using three binary inputs (fselFB2:0).

All five banks of Robo can divide by 1,2,3,4,5,6,8,10,12. Any Robo bank can be substituted for any Motorola bank. RoboClock can achieve exactly the same external behavior as that of the Motorola parts by setting the internal dividers to half of the values used in an equivalent MPC972/973.

The desired multiply/divide function can be configured by setting the Robo dividers to Qa=2,3,4,5, Qb=2,3,4,6, Qc=1,2,3,4, QFB=2,3,4,5,6,8,10, each using two "three-level" inputs ([1:4]DS[1:0] and FBDS[1:0])

However, in conversion projects like those assumed in this note, the divide settings often will have been chosen to satisfy a concern for meeting the Motorola VCO operating range requirement. There are cases where the suggested (typical) factor-of-two-difference gives an incorrect solution. Check to see that the "divide by one frequency" (F_{NOM} in the Robo data sheet) is less than 200 MHz (remember that the max. output frequency is 185 MHz. This can be a problem when the FB bank is set to divide by >10 (fselFB2=1). Usually the preferred solution will be to set the RoboClock Divide-selects at one-quarter of the Motorola equivalents.

Table 1. REF-Input to Qx-Output Frequency Ratios for all combinations of FEEDBACK and OUTPUT divide selections

MPC972/973	CY7B993/994 RoboClock II	MPC972/973 Output Q Divide Function								
		2	4	6	8	10	12	16	20	
		CY7B993/994 Output Q Divide Function								
		1	2	3	4	5	6	8	10	12
2[1]	1	1.000	0.500	0.333	0.250	0.200	0.167	0.125	0.100	0.083
4	2	2.000	1.000	0.667	0.500	0.400	0.333	0.250	0.200	0.167
6	3	3.000	1.500	1.000	0.750	0.600	0.500	0.375	0.300	0.250
8	4	4.000	2.000	1.333	1.000	0.800	0.667	0.500	0.400	0.333
10	5	5.000	2.500	1.667	1.250	1.000	0.833	0.625	0.500	0.417
12	6	6.000	3.000	2.000	1.500	1.200	1.000	0.750	0.600	0.500
16	8	8.000	4.000	2.667	2.000	1.600	1.333	1.000	0.800	0.667
20	10	10.00	5.000	3.333	2.500	2.000	1.667	1.250	1.000	0.833
	12	12.00	6.000	4.000	3.000	2.400	2.000	1.500	1.200	1.000

Note:

1. The MPC972/973 QFB output can't be set to divide by two.This divide ratio might have been achieved by using Qc as the fed-back output (i.e., connect one of the QcX outputs to Ext_FB).

A Few Examples

Example 1 in *Table 2* is an illustration taken from an actual system using an MPC973. The FB divide ratio is set to divide-by-4 to insure that the internal VCO frequency is within the specified operating range (i.e., 62.5x4=250 MHz). The output divide ratios are shown in the table as 0.50, 1.00, and 2.00. An as can be seen in *Table 1*, there are at least two ways to get these divide ratios using the divide ratios available in RoboClock II.

Option 1 will give the correct output frequencies, but is an unacceptable choice because the FB divider (and thus the internal multiplied VCO frequency) is above the operational range of Robo (i.e, 250 MHz is > $Fnom_{max}$ of 200 MHz).

Option 2 gives the same results with a lower VCO frequency (i.e., 125 MHz).

In this example the Robo dividers should be set to one-half the values chosen for the MPC973 to yield the same result.

Table 2. An Example with Outputs at Half, 1x, 2x Reference Frequency of 62.5 MHz

Output Bank	Output Freq. (MHz)	Divide Ratio (fsel_ val)	Bank/QFB ratio	Option 1 Divide Ratio (DS[1:0])	Option 2 Divide Ratio (DS[1:0])
Qa	31.25	÷8 (10)	0.50	÷8 (HL)	÷4 (ML)
Qb	62.5	÷4 (00)	1.00	÷4 (ML)	÷2 (LM)
Qc	125	÷2 (00)	2.00	÷2 (LM)	÷1 (LL)
FB (x4)	62.5	÷4 (000)		÷4 (ML)	÷2 (LM)
				Not OK	**OK**

Example 2 in *Table 3* shows a similar system solution. The FB divide ratio is again set to divide by four to allow the internal VCO frequency to fall within the specified operating range (i.e., 62.5x4=250 MHz). The output divide ratios are shown in the table as 0.50, 1.00, and 1.00. The difference between this example and the previous one is that for this system the maximum desired output frequency is 62.5 MHz (frequency of Qc). This subtle difference allows a different choice of dividers to achieve the desired output frequency.

Both Option 1 and Option 2 will give the correct output frequencies, and each is an acceptable solution since the Fnom is 125 and 62.5 MHz respectively.

Option 1 would require that a CY7B994 have FS wired HIGH. Option 2 would require that a CY7B994 would have FS left unconnected (MID) or if a CY7B993 was used, it would have FS wired HIGH.

In this example the Robo dividers can be set at either one-half or one-quarter the values chosen for the MPC973 to yield the same result.

Table 3. An Example with Outputs at Half and 1x Reference Frequency of 62.5 MHz

Output Bank	Output Freq. (MHz)	Divide Ratio (fsel_ val)	Bank/QFB ratio	Option 1 Divide Ratio (DS[1:0])	Option 2 Divide Ratio (DS[1:0])
Qa	31.25	÷8 (10)	0.50	÷4 (ML)	÷2 (LM)
Qb	62.5	÷4 (00)	1.00	÷2 (LM)	÷1 (LL)
Qc	62.5	÷4 (01)	1.00	÷2 (LM)	÷1 (LL)
FB (x4)	62.5	÷4 (000)		÷2 (LM)	÷1 (LL)
				OK	**OK**

Example 3: *Table 4* shows the requirements for another system. The FB divide ratio has been set to divide by twenty to allow the internal VCO to operate within the specified operating range (i.e., 16.67x20=333.4 MHz). The output divide ratios are shown in the table as 5.00 and 2.50. As can be seen in *Table 1*, there are at least two ways to get these divide ratios using the divide ratios available in RoboClock II.

Table 4. An Example with Outputs at 5x and 2.5x Reference Frequency of 16.67 MHz

Output Bank	Output Freq. (MHz)	Divide Ratio (fsel_ val)	Bank/QFB ratio	Option 1 Divide Ratio (DS[1:0])	Option 2 Divide Ratio (DS[1:0])
Qa	83.5	÷4 (00)	5.00	÷2 (LM)	÷1 (LL)
Qb	83.5	÷4 (00)	5.00	÷2 (LM)	÷1 (LL)
Qc	41.67	÷8 (11)	2.50	÷4 (ML)	÷2 (LM)
FB (x20)	16.67	÷20 (111)		÷10 (HM)	÷5 (MM)
				OK	**OK**

Option 1 will give the correct output frequencies, and is an acceptable solution since the Fnom is 166.7 MHz, well within the range of RoboClock II.

Option 2 gives the same results with a lower VCO frequency (i.e., Fnom=83.5 MHz) which might result in lower power dissipation.

Option 1 would require that a CY7B994 have FS wired HIGH. Option 2 would require that a CY7B994 would have FS left unconnected (MID) or if a CY7B993 was used, it would have FS wired HIGH.

In this example the Robo dividers are set at either one-half or one-quarter the values chosen for the MPC973 to yield the same result.

Choose the Bank Assignment

There are several solutions for mapping of RoboClock Banks to Motorola Banks. Several bank-assignments would work in most systems but some offer a cleaner layout than others. The following examples assume that a '972/'973 PCB layout already exists, and that there is a desire to minimize re-layout of the critical clock traces.

In *Figure 3* the Motorola part has been configured to allow the use of an inverting Qc. The Inv_Clk input (pin14) will be wired HIGH (or might be switched by external logic). To achieve the same result, the RoboClock INV3 input (pin 46) must be wired LOW. If the Motorola input is switched, then a resistive voltage divider must be added to insure that the INV3 input (pin 46) goes to VCC/2 when a non-inverting Qc is desired.

Both examples that follow show a layout conversion on the "component side" of the board. If the layout conversion could have been made using the "solder side" of the board, other problems and simplifications arise.

Both of the examples show the "Feedback input" (Ext_FB) connected through a short connection to the adjacent "Feedback output" (QFB). Since Motorola parts don't have skew control (see the section on ENHANCEMENTS which follows), it is common to find that the QFB to Ext_FB connection is actually connected through a wire about the same length as those that connect each of the other outputs to its respective load. If that describes this system, the Robo QFA1-to-FBKB+ connection should be routed through the same wire.

A more robust system can be built using the short Feedback connection shown to minimize noise injection into the PLL. The required "skew" or "wire-delay" can be achieved by selecting an appropriate skew for either the "Feedback output" or for each of the other banks. (See the section on Enhancements.)

In systems that don't use the "invert" function of Qc, RoboClock can be positioned for more direct access to the REFCLK inputs.

These systems will have the Inv_Clk input (Pin 14) wired LOW. RoboClock will have its INV3 input (Pin 46) unconnected (MID) to achieve the same result. The bank assignments change from those used in *Figure 3*, but all of the functionality remains. *Figure 4* shows an MPC973 (non-inverting Qc) layout example.

If both TCLK1 and TCLK0 (as might be found in an MPC972 application) are used (and the '973-PECL or '972-XTAL inputs are unused), then a simple re-connection of the REFA+ input to the desired TCLK input (example not shown) is all that is required to completely replace the Motorola part.

Select the Appropriate Bank (Driven by Specific Bank Function)

The frequency divider function of the Qa and Qb banks of the '972/973 can be performed by any of the four-output banks and the two-output bank on Robo. However, only Robo Bank-3 can perform the output-invert function of the Qc bank.

On the MPC972/973, Qc0 and Qc1 always rise and fall in phase with Qa and Qb banks if the respective divide ratios are the same. Qc2 and Qc3 allow the choice of "in-phase" or "inverted" operation by the setting of the Inv_Clk pin. This same function is offered in Robo-II by use of the INV3 pin.

If INV3 is left floating (MID) all four outputs of the third bank (3QA1, 3QA0, 3QB1, 3QB0) are in phase with the other outputs.

If INV3 is tied LOW (GND) then two outputs (3QA0 and 3QB0) are in phase and two outputs (3QA1 and 3QB1) are inverted. In this mode, the t_{rise}, t_{fall} and skew are well enough matched to drive differential transmission lines. With a few external resistors, these outputs can be made Differential-PECL compatible.

Robo also offers the option of having all four outputs "inverted" by tying INV3 HIGH (VCC).

If the Qc bank is to be used as a "normal bank of four" any Robo bank can be used in its place. If the Qc bank is to be used as a bank with "two normal" outputs and "two inverted" outputs, then Robo bank 3 (3QA1and 0 and 3QB1 and 0) must be used to mimic the Qc bank.

The QFB output function of MPC972/3 can be achieved by any of the five banks on Robo. Since the Motorola parts only have a single QFB output, it is likely that multiple outputs will not be needed in a conversion project. Any bank can be used for Feedback, but use of the two-output Feedback Bank (QFB0, QFB1) will result in easier PCB routing, lower power and lower noise levels because fewer outputs will be active.

In many systems the second Robo-QFB output can be substituted for the MPC972/973-QSYNC output. Robo has no equivalent for the complete QSYNC function.

Disable Outputs

Typically only three of the available four Robo output banks will be used. To reduce power and minimize switching noise in the system, the unused bank should be disabled. To disable an unwanted output bank, wire its associated disable pin (DIS[1:4]) HIGH (VCC). (See *Table 5*.)

Table 5. Disable Functionality

OUTPUT_MODE	DIS[1:4]/FBDIS	Output Function
HIGH/LOW	LOW	ENABLED
HIGH	HIGH	HI-Z
LOW	HIGH	HOLD_LOW
MID	X	FACTORY TEST

Unused outputs within a bank may be left unconnected with minimal loss of skew precision. The unused output will switch but will not contribute significant power supply imbalance, the only effect that could cause skew degradation. The effect of leaving one or more outputs unconnected falls well within the t_{SKEW} spec. Typically it adds <~15 ps variation between the remaining outputs.

The MPC972/973 includes a circuit to allow output banks to be disabled through a serial input. Robo does not support this function. Output banks on Robo can be logically disabled by individual pins (DIS[1:4] and FBDIS).

The disabled output can be set to High Impedance (HI-Z) or to an active LOW based on the level of the OUTPUT_MODE input. IF OUTPUT_MODE is tied HIGH (VCC) the disabled outputs will be “off” (HI-Z). If OUTPUT_MODE is tied LOW (GND) the disabled outputs will finish the “pulse in progress” and then remain LOW.

The disable function in RoboClock II serves as both the disable and the OE function of the Motorola parts.

Unused and Non-Equivalent Pins

There are a number of pins on the MPC972 and MPC973 that have no equivalent in RoboClock II (See *Table 6*). Likewise, there are a number of pins in RoboClock II that don’t exist on the Motorola parts. In addition, there are several pins on RoboClock II that are unused or connected to a default value for a typical Motorola to Cypress conversion

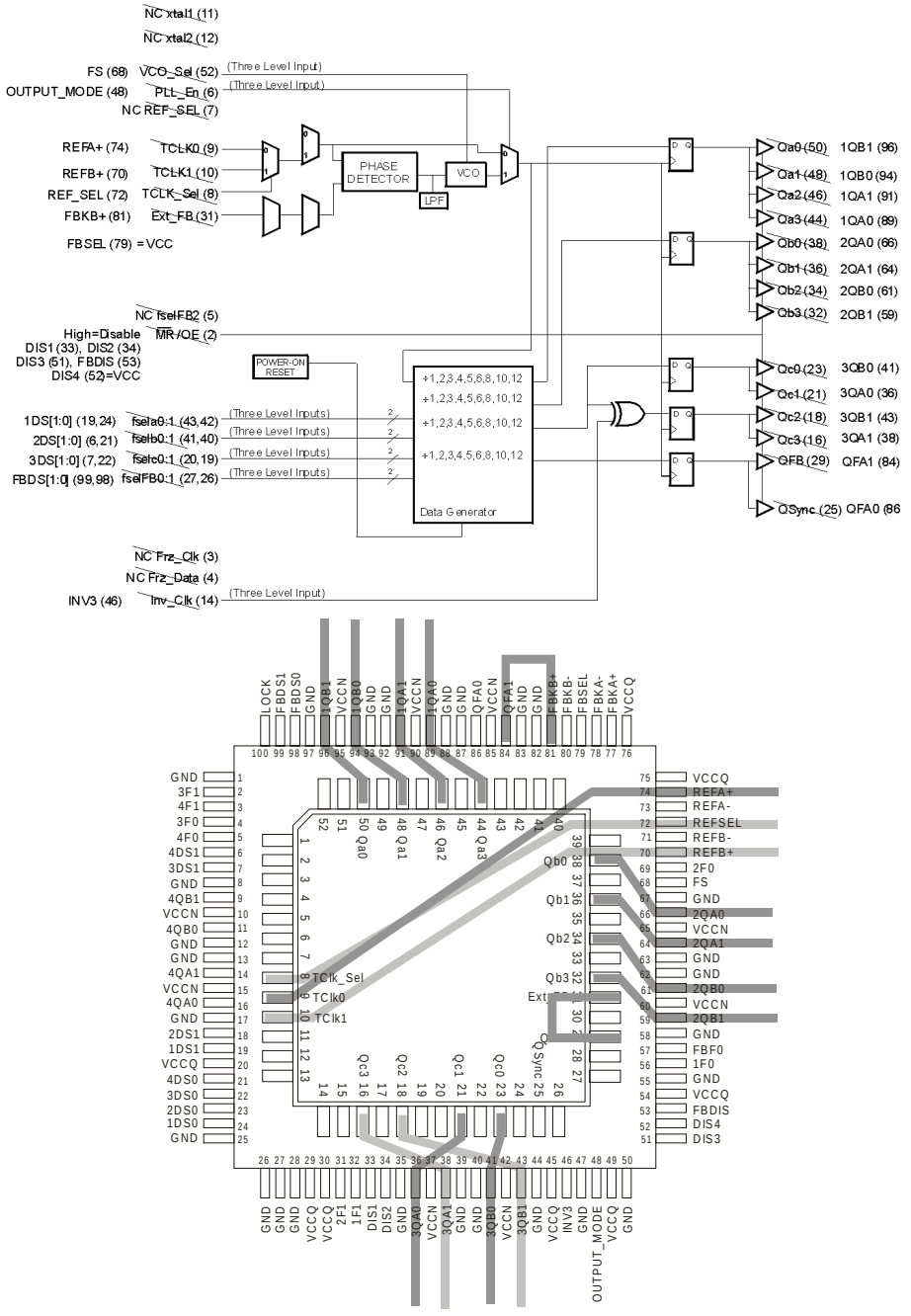


Figure 3. RoboClock II Working as an MPC972 (with Inverting Qc Bank and No QSync)

Control Signals omitted for clarity

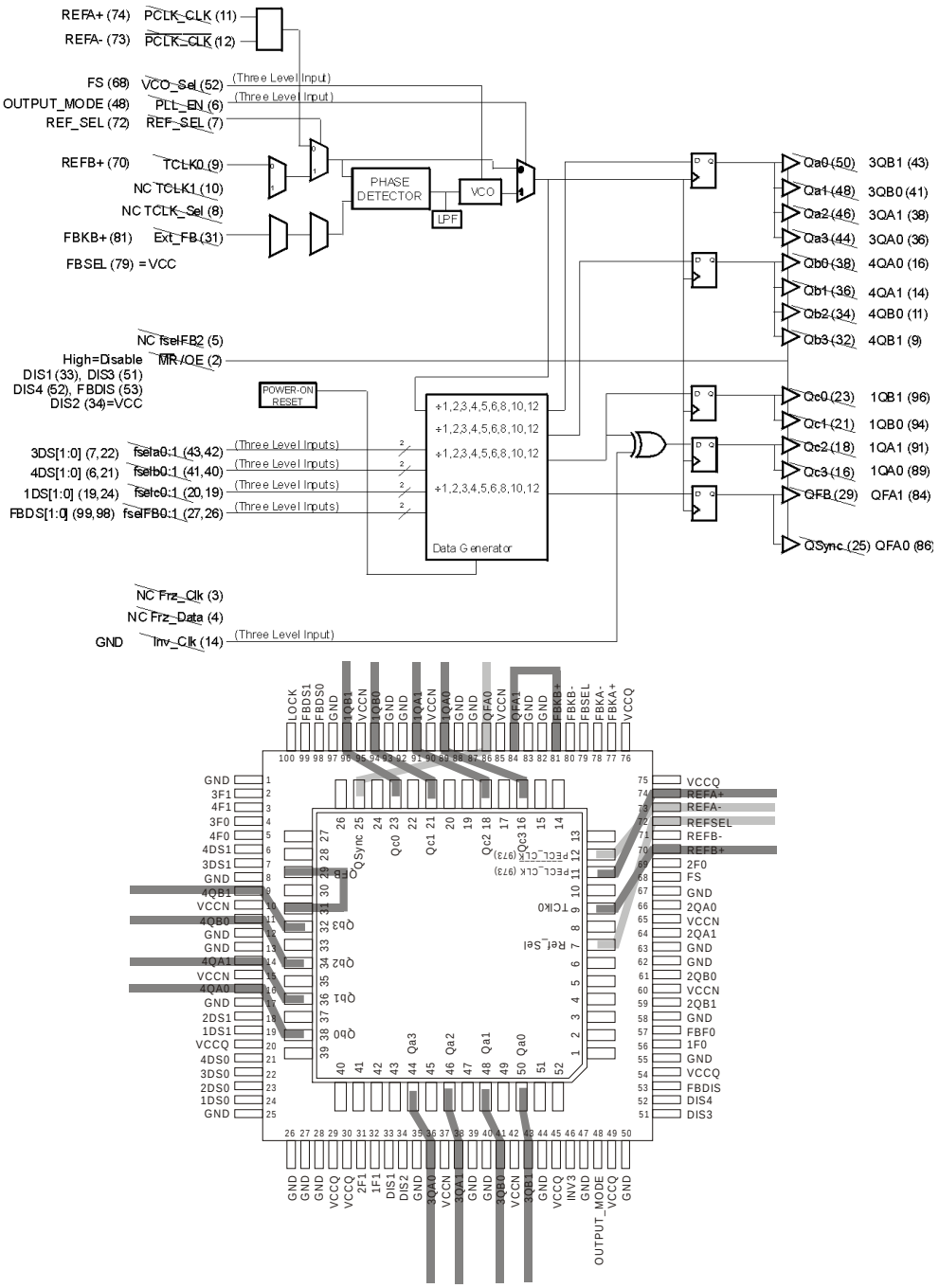


Figure 4. RoboClock II Working as an MPC973 (Non-inverting Qc Bank)

Control signals omitted for clarity.

Table 6. Unused and Non-Equivalent Pin Connections

Pin	Connection	Comment
MPC972 and MPC973 pins and functions *(Motorola pin numbers are indicated)*		
2 $\overline{MR}$/OE	Master Reset when LOW, Output Enabled when HIGH	Equivalent to DIS[1:4] & FBDIS, but input levels are inverted and output "function" is dependent on OUTPUT_MODE.
14 Inv_Clk	Inverts half of Bank C (Qc2 & Qc3) when HIGH Equivalent to LOW is Equivalent to HIGH is Additional feature if needed	Equivalent to INV3, but input levels are different. INV3 level selection is: MID 3QA0, 3QA1, 3QB0, 3QB1 all in phase LOW 3QA0, 3QB0 in phase, 3QA1, 3QB1 invert HIGH 3QA0, 3QA1, 3QB0, 3QB1 all invert
3 FRZ_CLK 4 FRZ_DATA	Output "Freeze" control Clock Output "Freeze" control Data	No direct Robo equivalent. DIS[1:4] & FBDIS can freeze the outputs, but are controlled by a pin per bank.
5 fselFB2	HIGH selects (fselFB0:1)/2 to manage VCO operating range. LOW selects fselFB0:1	No direct Robo equivalent. Dividers can usually be set with bank/bank relationships to preclude the use of this function.
6 PLL_En	HIGH selects internal PLL LOW bypasses VCO for TEST	OUTPUT_MODE=MID sets Robo TEST mode.
52 VCO_Sel	HIGH selects VCO operating range fVCO 200-480 MHz LOW selects VCO/2 operating range fVCO 100-240 MHz	Robo equivalent function is FS '994 '993 (MHz) FS=VCC 96–200 48–100 FS=OPEN 48–100 24–52 FS=GND 24–52 12–26
11, 12 xtal1,2 (MPC972 only)	Crystal oscillator input pins.	No Robo equivalent.
CY7B993 and CY7B994 pins and functions *(RoboClock II pin numbers are indicated)*		
78 FBKA+ 77 FBKA- 74 REFA+ 73 REFA-	Differential or Single ended Feedback inputs selected by FBSEL=LOW Differential or Single ended Reference inputs selected by REFSEL=LOW	If singled ended operation is desired, connect a signal to the pin with the desired "logical sense" and leave the other one open. Non-inverting Feedback is made by connection to FBKA+ or B+ Inverting Feedback is made by connection to FBKA– or B– Inverting the feedback will cause the FALLING output edges to be aligned with the RISING input edges of the selected REF.
81 FBKB+ 80 FBKB- 70 REFB+ 71 REFB-	Differential or Single ended Feedback inputs selected by FBSEL=HIGH Differential or Single ended Reference inputs selected by REFSEL=HIGH	
79 FBSEL 72 REFSEL	Select FBKA or FBKB (int. Pull-Down) Select REFA or REFB (int. Pull-Down)	Can be left unconnected if FBKA or REFA is desired
56 1F0, 32 1F1, 69 2F0, 31 2F1, 4 3F0, 2 3F1, 5 4F0, 3 4F1, 57 FBF0	Phase alignment select inputs.	If both xF0 and xF1 are left unconnected, the output will be phase aligned with the REF input.
33 DIS1, 34 DIS2, 51 DIS3, 53 FBDIS 52 DIS4 (test mode reset)	Output-Disable inputs. Outputs are "disabled" to "Z" or "LOW" when this input is HIGH. (int. Pull-Down)	DIS4 is used when in TEST MODE (OUTPUT_MODE=MID) to reset internal state machine logic.
Unused Outputs	Unused banks should be Disabled by setting that particular Disable input HIGH (i.e., DIS[1:4] or FBDIS wired to V_{CC})	Unused output pins within an active bank may be left open to reduce power dissipation. The difference in Output-Output skew caused by this load imbalance is <~15ps.
VCCQ 20,29,30,45,49,54,75,76 VCCN 10,15,37,42,60,65,85,90, 95	Equivalent to VCCA (Motorola pin 13) & VCCI (Motorola pin 28) Equivalent to VCCO (Motorola pins 17, 22, 33, 37, 45, 49)	All VCC pins should be connected to a common power plane and bypassed to the "global" ground using the lowest impedance connections possible.
GND 1,8,12,13,17,25,26,27,28, 35,39,40,44,47,50,55,58,62,6 3, 67,82,83,92,93,97	Equivalent to GNDI (Motorola pin 1) and GNDO (Motorola pins 15, 24, 30, 35, 39, 47, 51)	All GND pins should be connected to the global ground plane with the low impedance connections possible.

Timing Specifications

The timing specifications of RoboClock are comparable, and mostly superior to the Motorola parts. The following table lists the significant ones.

Parameter	Characteristic	Motorola			Equivalency Qualification	RoboClock II			Unit
		Min.	Typ.	Max.		Min.	Typ.	Max.	
t_{os}	**Output-to-Output Skew**[3]			550	t_{SKEW} Across all outputs: Within any Bank: Between any Pair:		 200 100 65	 350 200 100	ps
t_{jitter}	**Cycle-to-Cycle Jitter** (Peak-to-Peak)		±100		Divide ratio >1 Divider ratio =1		±60 ±85	±100 ±200	ps
t_{pd}[4]	SYNC to Feedback MPC973 TCLK0 TCLK1 PECL_CLK	 –70 –130 –225	 130 70 –25	 330 270 175	FB to selected REF		±100	±250	ps
	MPC972 TCLK0 TCLK1	–270 –330	130 70	530 470					
f_{max}	Maximum Output Frequency Q (÷2) Q (÷4) Q (÷6) Q (÷8)			 125 120 80 60	 CY7B994 CY7B993			 185 100	MHz
f_{ref}	Reference input Frequency[2]			100[2]	Depends on FS and [4:1]DS[1:0]	1.0		185	MHz
$f_{ref}DC$	Reference Input Duty Cycle	25%	75%			700 ps			
t_r, t_f	Output Rise/Fall Time[3] 0.8 to 2.0v	0.15		1.2			0.9	1.3	ns
t_{pw}	Output Duty Cycle[3]	$\frac{t_{CYCLE}}{2}$ –750	$\frac{t_{CYCLE}}{2}$ ±500	$\frac{t_{CYCLE}}{2}$ +750		$\frac{t_{CYCLE}}{2}$ –600	$\frac{t_{CYCLE}}{2}$ ±150	$\frac{t_{CYCLE}}{2}$ +600	ps
f_{VCO}	VCO Lock Range	200		480	Determined by FS	96(994) 48 24 12(993)		200(994) 100 52 26(993)	MHz
t_{PLZ}, t_{PHZ}	Output Disable Time	2		8			3	7	ns
t_{PZL}, t_{PZH}	Output Enable time	2		10			5	8	ns
t_{lock}	Maximum PLL Lock Time			10				10	ms

Notes:

2. Mot-Note 5. Maximum input reference frequency is limited by the VCO lock range and the feedback divider, or 100 MHz. Minimum input reference frequency is limited by the VCO lock range and the feedback divider. *RoboClock's lowest input frequency is limited to 1.0 MHz by FS range setting, Feedback divider selection and PLL bandwidth for clock feed-through (jitter) considerations*.
3. Mot-Note 7. 50Ω transmission line terminated into $V_{CC}/2$.
4. Mot-Note 8. t_{pd} is specified for a 50MHz input reference. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter. *RoboClock's t_{pd} is not a strong function of frequency and does not depend on a particular REFCLK source. The specification shown is valid for all operating frequencies.*

Enhancements

RoboClock II offers other functions not present on the MPC972 and MPC973. A complete description of the full functionality available in RoboClock II can be found in the RoboClock II CY7B993V/CY7B994V Data Sheet.

CY7B993 and 994 include several notable features that can enhance system margins and ease the pressures of product development, debug, and revision.

- RoboClock II has more outputs and more output banks. This adds flexibility in selecting the proper output and allows higher fanout to solve more complicated clock distribution problems.
- RoboClock II outputs operate at higher speeds than the Motorola parts. This will should enhance system flexibility and increase system design margin.
- RoboClock II offers a wider array of divide (and multiply) functions for additional flexibility. Divide functions not available in the Motorola parts and a wider selection on every bank will allow more flexibility in design of the system.
- Both REFA+ and REFB+ can be used as single ended (TTL) inputs or as differential (PECL) inputs.
- Both REF input pairs are “HOT-SWAP” tolerant.
- Input buffers for the Feed Back input (FBKA+, FBKB+) match the selections available for the REF input buffer configurations (Differential and Single-Ended) to allow better T_{pd} performance by matching input thresholds.
- The RoboClock II Skew Select function allows output-to-output skews to be adjusted from their nominal Zero-Skew position. In the examples in *Figure 3* and *Figure 4*, the Skew Select inputs are “OPEN”. When the “F” inputs are OPEN (they are internally biased to VCC/2 or MID level), all outputs are positioned at ZERO skew. If the inputs are wired HIGH (VCC) or wired LOW (GND) many other timing configurations are possible.

Selectable skew is offered in discrete increments and is expressed in “time-unit” (t_u). The value of a $\mathbf{t_u}$ is determined by the FS setting and the nominal frequency of a “divided by one” output. Equation 1 can be used to determine the $\mathbf{t_u}$ value.

$$t_u = 1/(f_{nom}*N) \quad \text{Eq. 1}$$

N is a multiplication factor which is determined by the FS setting. $\mathbf{f_{nom}}$ is the nominal frequency of the device (i.e., the frequency of an output set to “Divide-by-ONE”). **N** is defined in *Table 7*. The nominal frequency that yields a $\mathbf{t_u}$ of 1.0 ns is also shown.

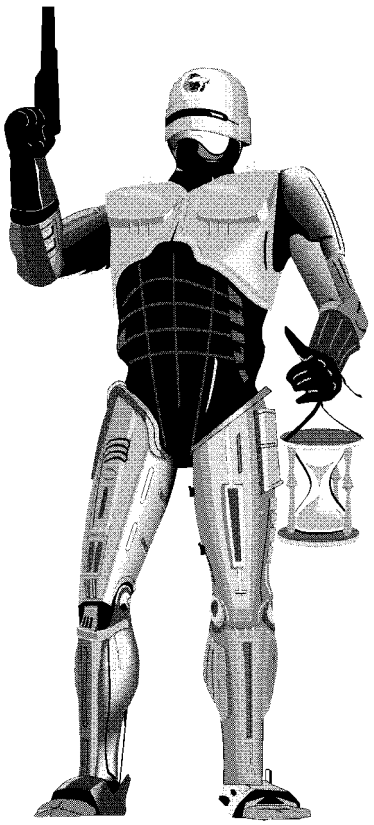
Table 7. .N Factor Determination

FS	CY7B993V		CY7B994V	
	N	f_{nom} (MHz) at which t_u = 1.0 ns	N	f_{nom} (MHz) at which t_u = 1.0 ns
LOW	64	15.625	32	31.25
MID	32	31.25	16	62.5
HIGH	16	62.5	8	125.0

The achievable skews, expressed in units of $\mathbf{t_u}$, are shown in Table *Table 8*.

Table 8. Output Skew Select Function

Function Selects		Output Skew Function				
[1:4] F1	[1:4]F0 and FBF0	Bank 1	Bank 2	Bank 3	Bank 4	Feed-back Bank
LOW	LOW	$-4t_u$	$-4t_u$	$-8t_u$	$-4t_u$	$-4t_u$
LOW	MID	$-3t_u$	$-4t_u$	$-7t_u$	$-4t_u$	NA
LOW	HIGH	$-2t_u$	$-4t_u$	$-6t_u$	$-4t_u$	NA
MID	LOW	$-1t_u$	$-4t_u$	**Same as Bank 1**	**Same as Bank 1**	NA
MID	MID	$0t_u$	$0t_u$	$0t_u$	$0t_u$	$0t_u$
MID	HIGH	$+1t_u$	$+1t_u$	**Same as Bank 2**	**Same as Bank 2**	NA
HIGH	LOW	$+2t_u$	$+2t_u$	$+2t_u$	$+2t_u$	NA
HIGH	MID	$+3t_u$	$+3t_u$	$+3t_u$	$+3t_u$	NA
HIGH	HIGH	$+4t_u$	$+4t_u$	$+4t_u$	$+4t_u$	$+4t_u$



If your system is all SKEWED-UP call for RoboClock