RoboClockII TEST Mode

Introduction to RoboClockII

RoboClockII is the next generation in Cypress's well known family of Programmable Skew Clock Buffers (PSCB). RoboClock differs from most zero delay buffers in that it offers the user the ability to skew outputs relative in time to each other. This 'skew-ability' enables the system designer to offset trace length differences in a synchronous system or work around set-up and hold time differences.

The device has the added flexibility of frequency multiplication and division. This, for example, would enable the designer to take a 25-MHz clock and multiply it up to 150 MHz while also generating a 30-MHz and 50-MHz from the same source. The part has 18 outputs with the capability to drive multiple loads. The device offers very low output skew and jitter.

The combined skew and frequency programmability make RoboClockII the most flexible clock buffer available in the market today. The part has several other features which separate it from the competition. One of these is a flexible TEST mode. The TEST feature is the subject of this note. For more information on the RoboClockII family of clock buffers please refer to the data sheet section of www.cypress.com. There are also several application notes available from our website.

RoboClockII TEST Mode

In some situations you may need to disable the RoboClockII phase-locked loop. For instance, in many board-level testing applications you may need to supply a clock input to the system that may not meet the REF input requirements of RoboClockII. This scenario can occur in bed-of-nails testing or single-step microprocessor execution.

The OUTPUT_MODE pin is a three level input. In normal system operation this pin is set HIGH or LOW. For testing purposes, this three level input can have a removable jumper to ground or V_{CC}. This will allow an external tester to change the change the state of these pins.

If the OUTPUT_MODE pin is forced to its MID state, the device will operate with its internal phase locked loop disconnected. The OUTPUT_MODE pin must be forced between $0.47V_{CC}$ and $0.53V_{CC}$ to ensure that it's set at the MID level. However, there is some flexibility around these settings and the MID level boundaries for typical silicon are compared to the data sheet limits in *Figure 1*. If the pin is left floating, internal resistors will set it to the MID level. When RoboClockII is put in TEST mode, input levels supplied to the reference input will be used in place of the PLL output. The signal applied to the reference input will pass through the internal logic of the device and the output of any given bank will be a divided version of the REF input. The actual divide ratio is dependent on the device being used (CY7B993V or CY7B994V), the FS setting and the divide setting on the output bank. *Figure 2* illustrates the path the reference signal will pass through to reach the output.

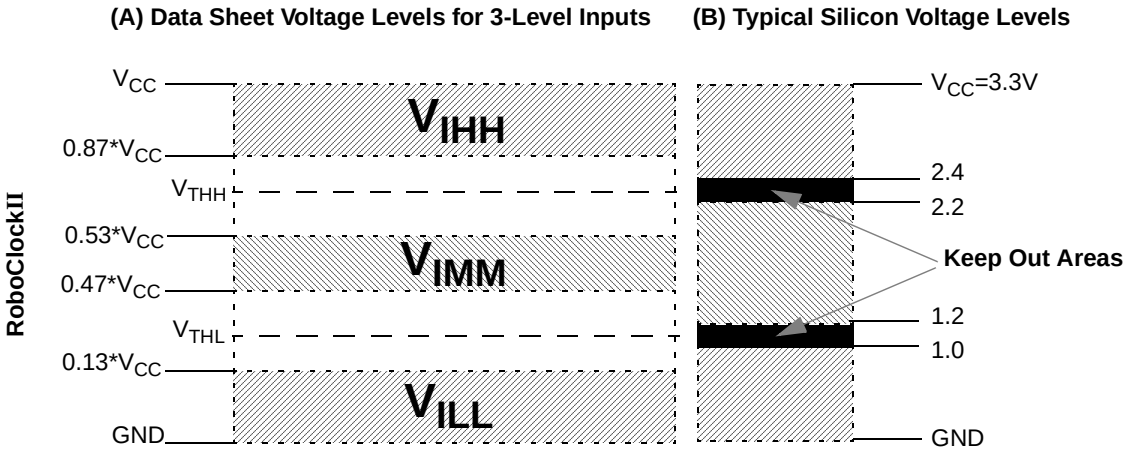

Figure 1. Voltage Levels for the OUTPUT_MODE Input

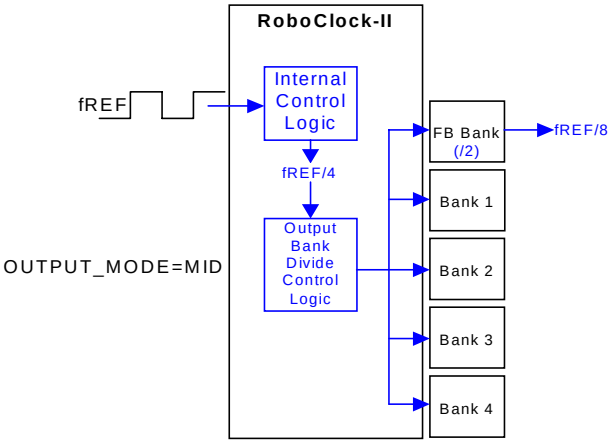

Figure 2. The Path REF Will Take in TEST Mode

The effect of the internal divide ratio must be coupled with the programmed divide ratio for the particular bank. For example, if the designer had a CY7B994V operating with FS HIGH, the internal divide ratio is 4 per *Table 1*.Now if one of the banks was configured for divide-by-5, the output frequency in TEST mode would be $f_{REF}/(4*5)=f_{REF}/20$. For a 20-MHz input, the output of this bank would be 1 MHz in TEST mode. The following equation can be used to determine the output frequency for any given configuration:

$$f_{OUT} = \frac{f_{REF}}{FS\_DIV \times BNK\_DIV}$$

Where:

f_{OUT} = output frequency of a given bank
f_{REF} = reference input frequency to RoboClockII
RS_DIV = the divide ratio for the FS setting (see *Table 1*)
BNK_DIV = the output bank programmed divide ratio

Table 1. Internal Divide Ratios in TEST Mode.

FS	993	994
LOW	32	16
MID	16	8
HIGH	8	4

There is no lower limit for the REF frequency in factory TEST mode. This is because in TEST mode the internal PLL is bypassed and the input levels supplied to REF directly control the internal logic. The input signal applied to REF will drive the internal state machine. The following 'scope waveform, *Figure 3*, shows a RoboClockII with the minimum divide ration of 4 (994v with FS=HIGH and output configured to divide by 1).

An important point to note is that in TEST mode the selected FB input must be tied LOW. All functions of the device are still operational in TEST mode except the internal PLL and the output bank disables. All outputs will be 50% duty cycle in test mode regardless of the REF input duty cycle. This is illustrated in *Figure 3* where the REF input has a 40% duty cycle and the outputs are still 50%.

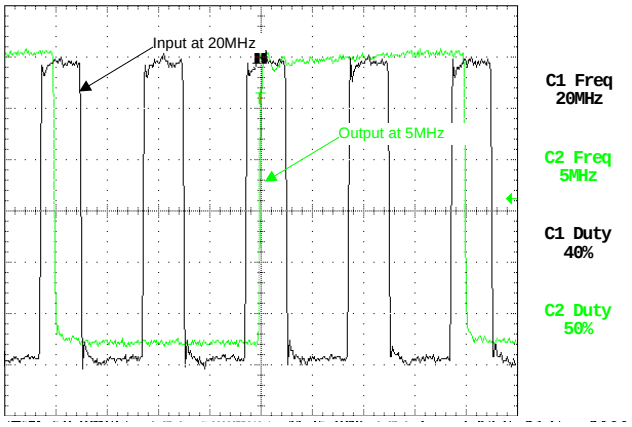

Figure 3. RoboClockII Output in TEST mode.

The normal skew capability of RoboClockII is still available in TEST mode. However, the skew granularity calculation is slightly different. When in TEST mode, a one REF input period will translate to $2t_U$ for skewed outputs. The positive width of the reference clock cycle is equal to the first time unit and the negative pulse width is equal to the second time unit. Thus, if the reference clock duty cycle is 50%, then half a clock period will be equal to $1t_U$. The skew functionality is shown in *Figure 4*.

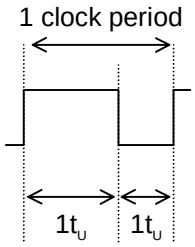

Figure 4. TEST Mode Skew Functionality.

The OUTPUT_MODE pin is designed to be a static pin. Dynamically toggling this input from LOW to HIGH may temporarily cause the device to go into factory TEST mode, when passing through the MID state, and you may have to allow up to t_{LOCK} before the part resumes normal operation.

Factory Test Reset

When in factory test mode, the device can be reset to a deterministic state by driving the DIS4 input HIGH. When the DIS4 input is driven HIGH in factory test mode, all clock outputs will go to HI-Z; after the selected reference clock pin has 5 positive transitions, all the internal finite state machines (FSM) will be set to a deterministic state. The deterministic state of the state machines will depend on the configurations of the divide selects, skew selects, and frequency select input. All clock outputs will stay in high-impedance mode and all FSMs will stay in the deterministic state until DIS4 is deasserted. When DIS4 is deasserted (with OUTPUT_MODE still at MID), the device will re-enter factory test mode.