



CYPRESS

PRELIMINARY

W48C111-17

# 100-MHz Mobile Motherboard System Clock

$V_{DDQ2} = 2.5V \pm 5\%$

## Features

- Maximized EMI suppression using Cypress's Spread Spectrum technology
- Power-on default to spread mode
- Two copies of CPU output
- Six copies of PCI output (synchronous w/CPU outputs)
- One copy of 48-MHz USB output
- One Buffered copy of 14.318-MHz input reference signal
- Supports 100-MHz or 66-MHz CPU operation
- Power management control input pins
- Low Frequency Test Mode
- Available in 28-pin SSOP (209 mil)

## Key Specifications

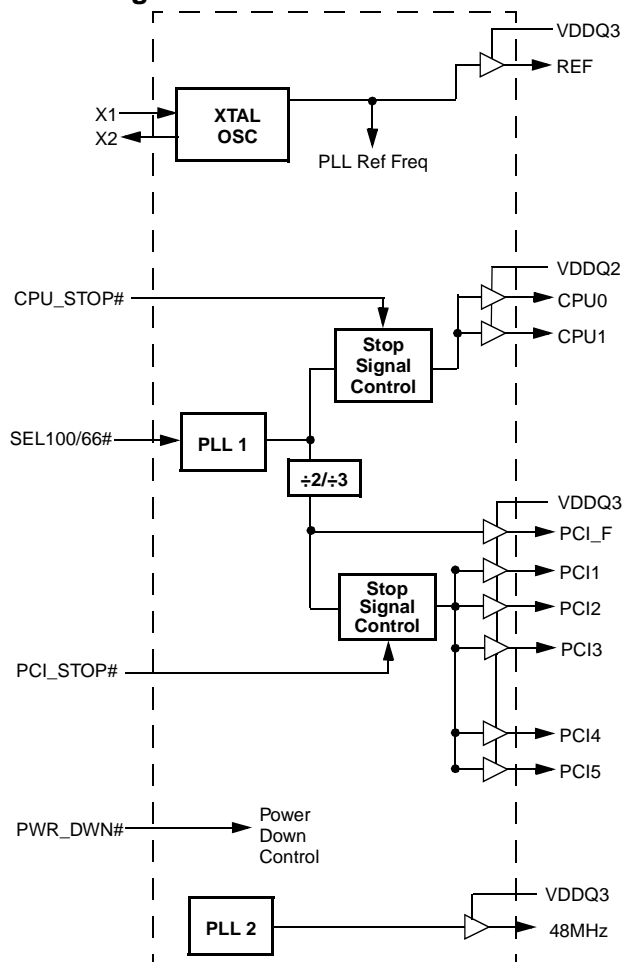
Supply Voltages: .....  $V_{DDQ3} = 3.3V \pm 5\%$

CPU0:1 Skew: ..... 175 ps  
 CPU0:1 Cycle-to-Cycle Jitter: ..... 200 ps  
 PCI\_F, PCI1:5 Skew: ..... 500 ps  
 PCI\_F, PCI1:5 Cycle-to-Cycle Jitter: ..... 250 ps  
 CPU to PCI Skew: ..... 1.5 to 4.0 ns (CPU Leads)  
 Output Duty Cycle: ..... 45/55%  
 PCI\_F, PCI Edge Rate: .....  $\geq 1$  V/ns  
 CPU\_STOP#, PWR\_DWN#, PCI\_STOP#: 250-k $\Omega$  pull-up resistor

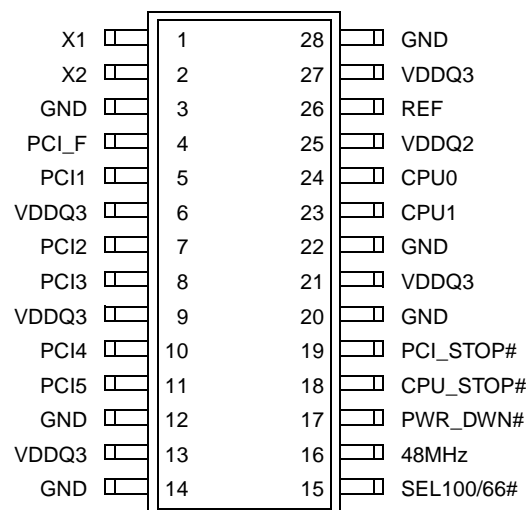
Table 1. Pin Selectable Frequency

SEL100/66#	CPU(0:1)	PCI	Spread%
0	66.6 MHz	33.3	-0.5%
1	100 MHz	33.3	-0.5%

## Block Diagram



## Pin Configuration





**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:1	24, 23	O	<b>CPU Clock Outputs 0 and 1:</b> These two CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ2. Frequency of signals is set by SEL100/66# input.
PCI1:5	5, 7, 8, 10, 11	O	<b>PCI Bus Clock Outputs 1 through 5:</b> These five PCI clock outputs are controlled by the PCI_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDQ3.
PCI_F	4	O	<b>Fixed PCI Clock Output:</b> Unlike PCI1:5 outputs, this output is not controlled by the PCI_STOP# control pin; it cannot be forced LOW by PCI_STOP#. Output voltage swing is controlled by voltage applied to VDDQ3.
48MHz	16	O	<b>48-MHz Output:</b> Fixed clock output at 48 MHz. Output voltage swing is controlled by voltage applied to VDDQ3.
CPU_STOP#	18	I	<b>CPU_STOP# Input:</b> When brought LOW, clock outputs CPU0:1 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:1 start with a full clock cycle (2–3 CPU clock latency).
PCI_STOP#	19	I	<b>PCI_STOP# Input:</b> The PCI_STOP# input enables the PCI1:5 outputs when HIGH and causes them to remain at logic 0 when LOW. The PCI_STOP signal is latched on the rising edge of PCI_F. Its effect takes place on the next PCI_F clock cycle.
REF	26	O	<b>Fixed 14.318-MHz Output:</b> Used for various system applications. Output voltage swing is controlled by voltage applied to VDDQ3.
SEL100/66#	15	I	<b>Frequency Selection Inputs:</b> Select power-up default CPU clock frequency as shown in Table 1 on page 1.
X1	1	I	<b>Crystal Connection or External Reference Frequency Input:</b> This pin can either be used as a connection to a crystal or to a reference signal.
X2	2	I	<b>Crystal Connection:</b> An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
PWR_DWN#	17	I	<b>Power-Down Control:</b> When this input is LOW, device goes into a low-power stand-by condition. All outputs are held LOW. CPU and PCI clock outputs are stopped LOW after completing a full clock cycle (2–3 CPU clock cycle latency). When brought HIGH, CPU and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency).
VDDQ3	6, 9, 13, 21, 27	P	<b>Power Connection:</b> Connected to 3.3V supply.
VDDQ2	25	P	<b>Power Connection:</b> Power supply for CPU0:1 output buffer. Connected to 2.5V.
GND	3, 12, 14, 20, 22, 28	G	<b>Ground Connection:</b> Connect all ground pins to the common system ground plane.



## Spread Spectrum Feature

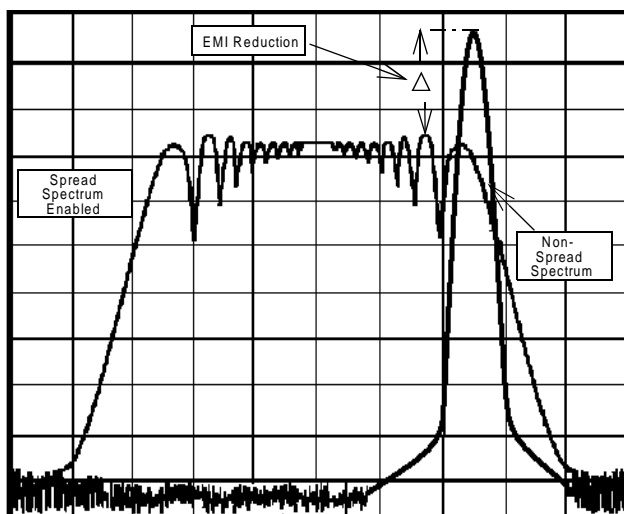
The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

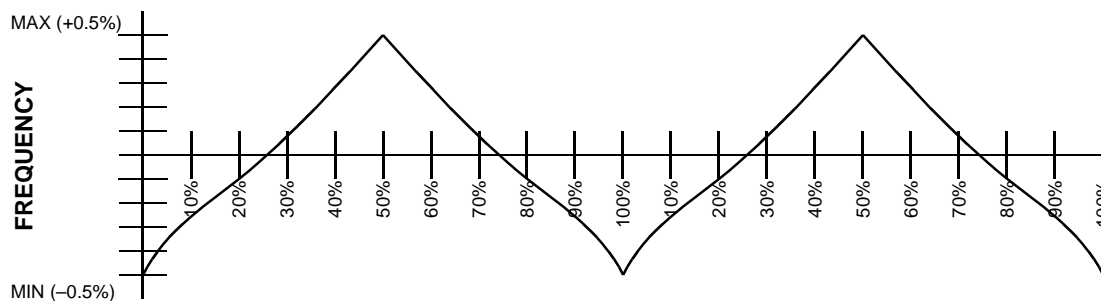
$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

Where  $P$  is the percentage of deviation and  $F$  is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is  $-0.5\%$  of the center frequency. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.



**Figure 1. Typical Clock and SSFTG Comparison**



**Figure 2. Typical Modulation Profile**



## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Operating Temperature	0 to +70	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C
$ESD_{PROT}$	Input ESD Protection	2 (min.)	kV

## DC Electrical Characteristics: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{DDQ3} = 3.3\text{V} \pm 5\%$ , $V_{DDQ2} = 2.5\text{V} \pm 5\%$ , CPU0:1 = 66.6/100 MHz

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I <sub>DD</sub>	3.3V Supply Current		Outputs Loaded <sup>[1]</sup>			75	mA
I <sub>DD2.5</sub>	2.5V Supply Current		Outputs Loaded <sup>[1]</sup>			50	mA
Logic Inputs							
V <sub>IL</sub>	Input Low Voltage			GND – 0.3		0.8	V
V <sub>IH</sub>	Input High Voltage			2.0		V <sub>DD</sub> + 0.3	V
I <sub>IL</sub>	Input Low Current <sup>[2]</sup>					–25	μA
I <sub>IH</sub>	Input High Current <sup>[2]</sup>					10	μA
I <sub>IL</sub>	Input Low Current (SEL100/66#)					–5	μA
I <sub>IH</sub>	Input High Current (SEL100/66#)					5	μA
Clock Outputs							
V <sub>OL</sub>	Output Low Voltage		I <sub>OL</sub> = 1 mA			50	mV
V <sub>OH</sub>	Output High Voltage		I <sub>OH</sub> = –1 mA	3.1			V
V <sub>OH</sub>	Output High Voltage	CPU0:1	I <sub>OH</sub> = –1 mA	2.2			V
I <sub>OL</sub>	Output Low Current	CPU0:1	V <sub>OL</sub> = 1.25V	55	115	190	mA
		PCI1:5, _F	V <sub>OL</sub> = 1.5V	20.5	53	139	mA
		REF	V <sub>OL</sub> = 1.5V	25	37	76	mA
I <sub>OH</sub>	Output High Current	CPU0:1	V <sub>OL</sub> = 1.25V	50	110	195	mA
		PCI1:5, _F	V <sub>OL</sub> = 1.5V	31	55	189	mA
		REFX	V <sub>OL</sub> = 1.5V	27	44	94	mA
Crystal Oscillator							
V <sub>TH</sub>	X1 Input Threshold Voltage <sup>[3]</sup>		V <sub>DDQ3</sub> = 3.3V		1.65		V
C <sub>LOAD</sub>	Load Capacitance, as seen by External Crystal <sup>[4]</sup>				14		pF
C <sub>IN,X1</sub>	X1 Input Capacitance <sup>[5]</sup>		Pin X2 unconnected		28		pF
Pin Capacitance/Inductance							
C <sub>IN</sub>	Input Pin Capacitance		Except X1 and X2			5	pF
C <sub>OUT</sub>	Output Pin Capacitance					6	pF
L <sub>IN</sub>	Input Pin Inductance					7	nH

### Notes:

1. All clock outputs loaded with 6" 60Ω transmission lines with 20-pF capacitors.
2. CPU\_STOP#, PCI\_STOP#, and PWRDWN# logic inputs have internal pull-up resistors.
3. X1 input threshold voltage (typical) is  $V_{DD}/2$ .
4. The W48C111-17 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).



## AC Electrical Characteristics

$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $V_{DDQ2} = 2.5\text{V} \pm 5\%$ ,  $f_{XTL} = 14.31818 \text{ MHz}$

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

### CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.25V	15		15.5	10		10.5	ns
$t_H$	High Time	Duration of clock cycle above 2.0V	5.2			3.0			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	V/ns
$t_F$	Output Fall Edge Time	Measured from 2.0V to 0.4V	1		4	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			200			250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.25V			175			175	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		13.5			13.5		$\Omega$

### PCI Clock Outputs, PCI1:5 and PCI\_F (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.5V	30			ns
$t_H$	High Time	Duration of clock cycle above 2.4V	12			ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	12			ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.5V			500	ps
$t_O$	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
$Z_O$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		$\Omega$



**REF Clock Output (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency generated by crystal oscillator	14.318			MHz
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z <sub>O</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

**48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	CPU = 66.6/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)	48.008			MHz
f <sub>D</sub>	Deviation from 48 MHz	(48.008 – 48)/48	+167			ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)	57/17			
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z <sub>O</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

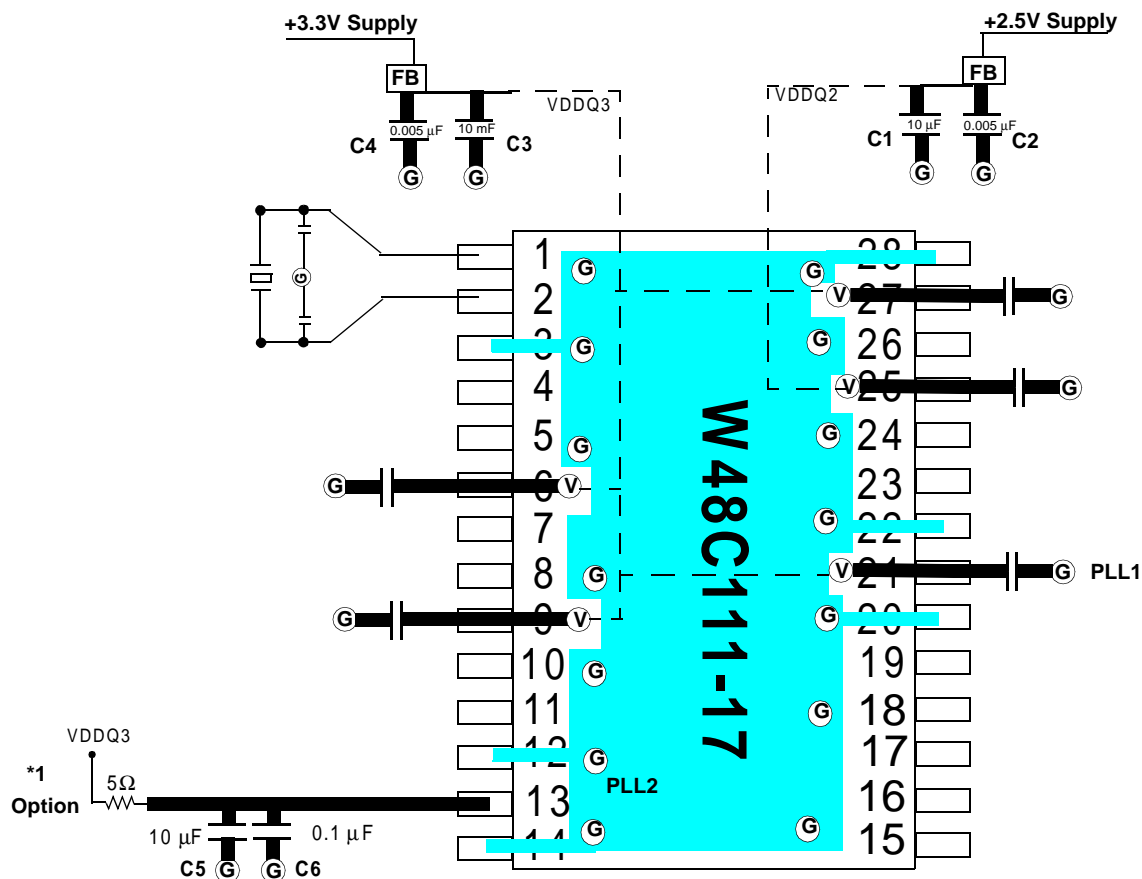
**Ordering Information**

Ordering Code	Freq. Mask Code	Package Name	Package Type
W48C111	-17	H	28-pin SSOP (209 mils)

Document #:38-00843-\*A



**Layout Example**



FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

Ceramic Caps C1 & C3 = 10 – 22 μF C2 & C4 = 0.005 μF C5 = 10 μF C6 = 0.1 μF

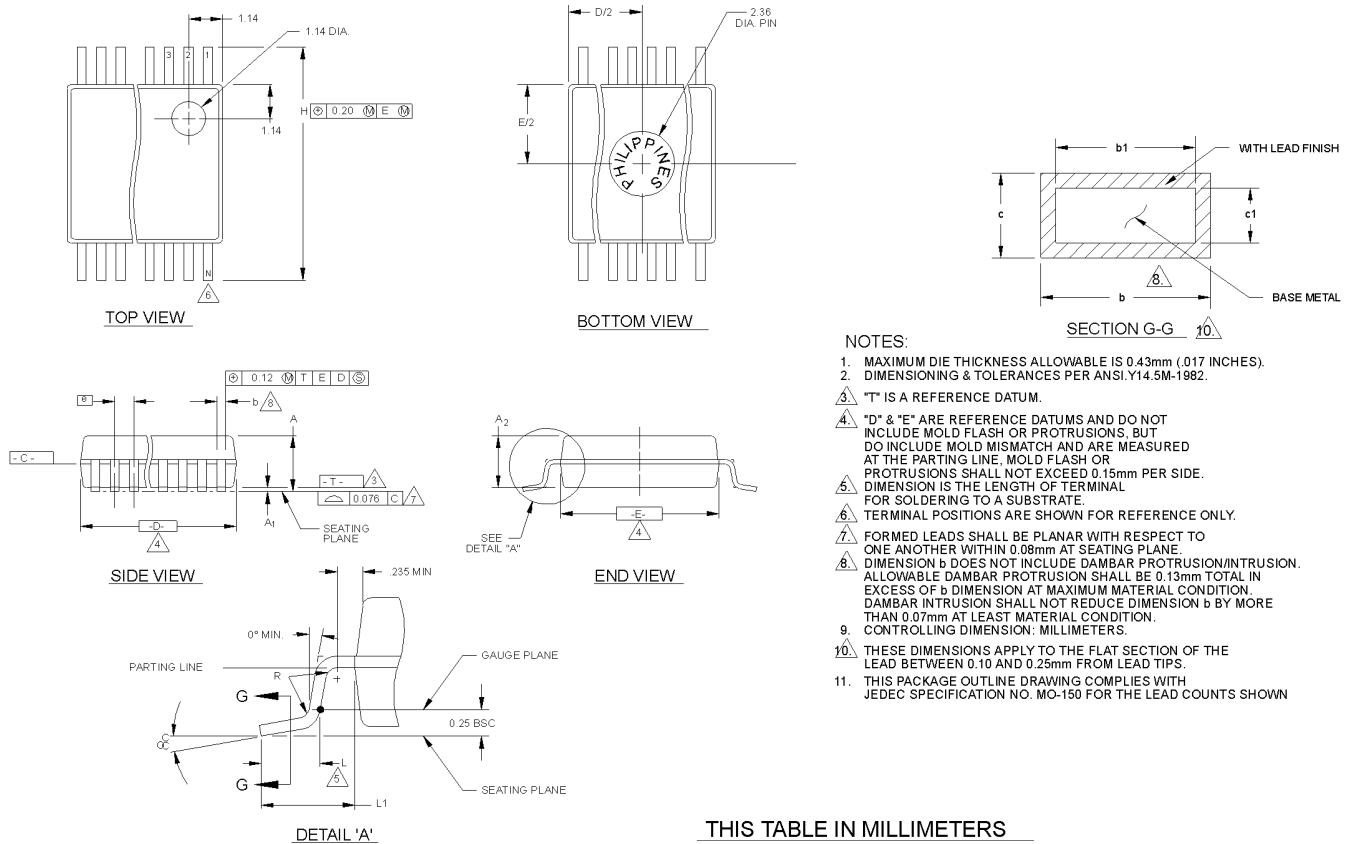
⊗ = VIA to GND plane layer ⊙ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors

All bypass caps = 0.1 μF ceramic

NOTE: \* 1 - If 48 MHz is not used for Video connect pin 13 to VDDQ3



**Package Diagram**
**28-Pin Small Shrink Outline Package (SSOP, 209 mils)**

**THIS TABLE IN MILLIMETERS**

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	1.73	1.86	1.99	AA	6.07	6.20	6.33	14
A <sub>1</sub>	0.05	0.13	0.21	AB	6.07	6.20	6.33	16
A <sub>2</sub>	1.68	1.73	1.78	AC	7.07	7.20	7.33	20
b	0.25	-	0.38	AD	8.07	8.20	8.33	24
b <sub>1</sub>	0.25	0.30	0.33	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	AF	10.07	10.20	10.33	30
c <sub>1</sub>	0.09	0.15	0.16					
D	SEE VARIATIONS							
E	5.20	5.30	5.38					
e		0.65 BSC						
H	7.65	7.80	7.90					
L	0.63	0.75	0.95					
L <sub>1</sub>	1.25 REF.							
N	SEE VARIATIONS							
OC	0°	4°	8°					
R	0.09	0.15						

**VARIAION AF  
IS DESIGNED BUT NOT TOOLED**

**THIS TABLE IN INCHES**

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.068	.073	.078	AA	.239	.244	.249	14
A <sub>1</sub>	.002	.005	.008	AB	.239	.244	.249	16
A <sub>2</sub>	.066	.068	.070	AC	.278	.284	.289	20
b	.010	-	.015	AD	.318	.323	.328	24
b <sub>1</sub>	.010	.012	.013	AE	.397	.402	.407	28
c	.004	-	.008	AF	.397	.402	.407	30
c <sub>1</sub>	.004	.006	.006					
D	SEE VARIATIONS							
E	.205	.209	.212					
e		.0256 BSC						
H	.301	.307	.311					
L	.025	.030	.037					
L <sub>1</sub>	.049 REF.							
N	SEE VARIATIONS							
OC	0°	4°	8°					
R	.004	.006						