PRELIMINARY

CY22393, CY22394, CY22395

Three-PLL Serial Programmable FLASH Programmable Clock Generator

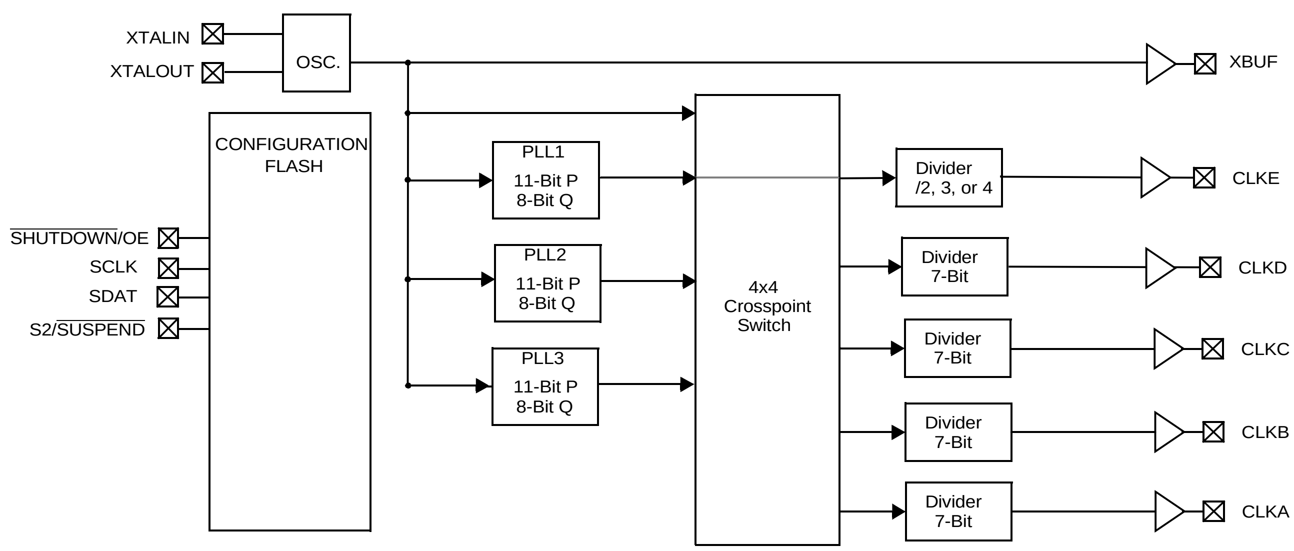
Features	Benefits
Three integrated phase-locked loops	Generates up to 3 unique frequencies on up to 6 outputs from an external source.
Ultra-Wide Divide Counters (8-bit Q, 11-bit P, and 7-bit Post Divide)	Allows for 0 ppm Frequency Generation and Frequency Conversion under the most demanding applications.
Improved Linear Crystal Load Capacitors	Improves frequency accuracy over temperature, age, process, and initial offset.
Flash programmability	Non-Volatile programming enables easy customization, ultra-fast turnaround, performance tweaking, design timing margin testing, inventory control, lower part count, and more secure product supply. In addition, any part in the family can also be programmed multiple times which reduces programming errors and provides an easy upgrade path for existing designs.
Field programmable	Low Cost Distribution or In-House programming support available for all opportunities with Cypress Proprietary Programmers or BP Micro and others.
Low-jitter, high-accuracy outputs	Performance suitable for high-end multimedia, communications, industrial, A/D Converters, and consumer applications.
Power-management options (Shutdown, OE, Suspend)	Supports numerous low-power application schemes and reduces EMI by allowing unused outputs to be turned off.
Configurable Crystal Drive Strength	Adjust Crystal Drive Strength for compatibility with virtually all crystals.
Frequency Select via three External LVTTL Inputs	3-Bit External Frequency Select Options for PLL1, CLKA, and CLKB.
3.3V operation	Industry-standard supply voltage.
16-pin TSSOP Package	Industry-standard packaging saves on board space.
CyClocks RT™ Support	Easy to use software support for design entry.

Advanced Features	Benefits
Serial Programmable	Allows in-system programming into volatile configuration memory. All frequency settings can be changed providing literally millions of frequency options.
Configurable Output Buffer	Adjust Output Buffer strength to lower EMI or improve timing margin.
Digital VCXO	Fine tune crystal oscillator frequency by changing load capacitance.
High Frequency LV PECL Output (CY22394 only)	Differential Output up to 400 MHz.
3.3/2.5V outputs (CY22395 only)	Provides interfacing option for low-voltage parts.

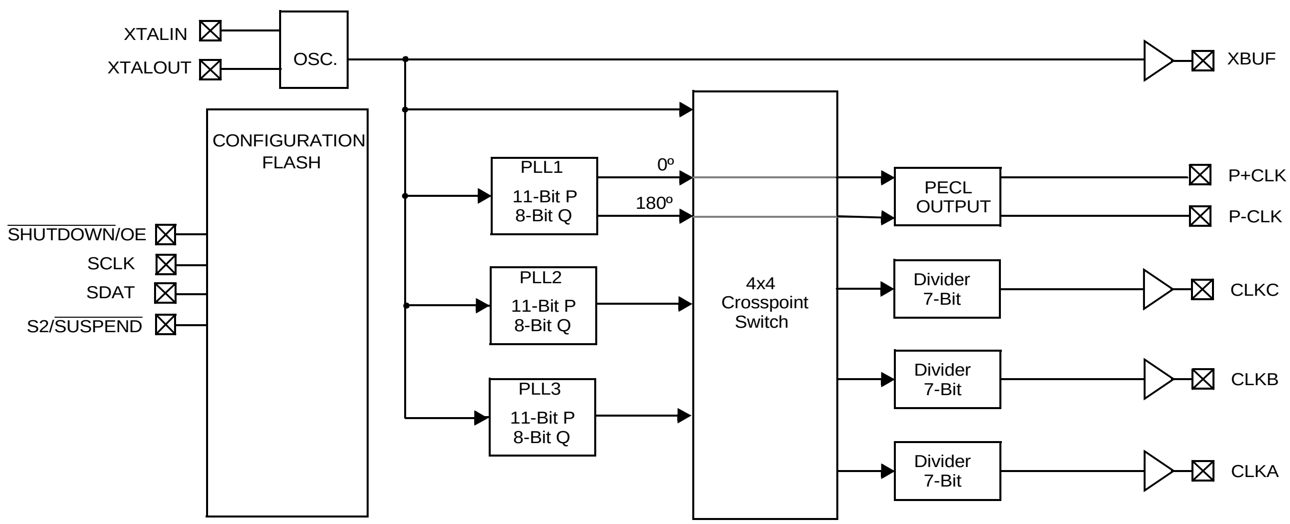
Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY22393FC	6 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–166 MHz (reference clock)	1 MHz–200 MHz	Commercial Temperature
CY22393FI	6 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–150 MHz (reference clock)	1 MHz–166 MHz	Industrial Temperature
CY22394FC	1 PECL / 4 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–166 MHz (reference clock)	100 MHz–400 MHz (PECL) 1 MHz–200 MHz	Commercial Temperature
CY22394FI	1 PECL / 4 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–150 MHz (reference clock)	125 MHz–375 MHz (PECL) 1 MHz–166 MHz (CMOS)	Industrial Temperature
CY22395FC	4 LVC-MOS / 1 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–166 MHz (reference clock)	1 MHz–200 MHz (3.3V) 1 MHz–133 MHz (2.5V)	Commercial Temperature
CY22395FI	4 LVC-MOS / 1 CMOS	8 MHz–30 MHz (external crystal) 1 MHz–150 MHz (reference clock)	1 MHz–166 MHz (3.3V) 1 MHz–133 MHz (2.5V)	Industrial Temperature

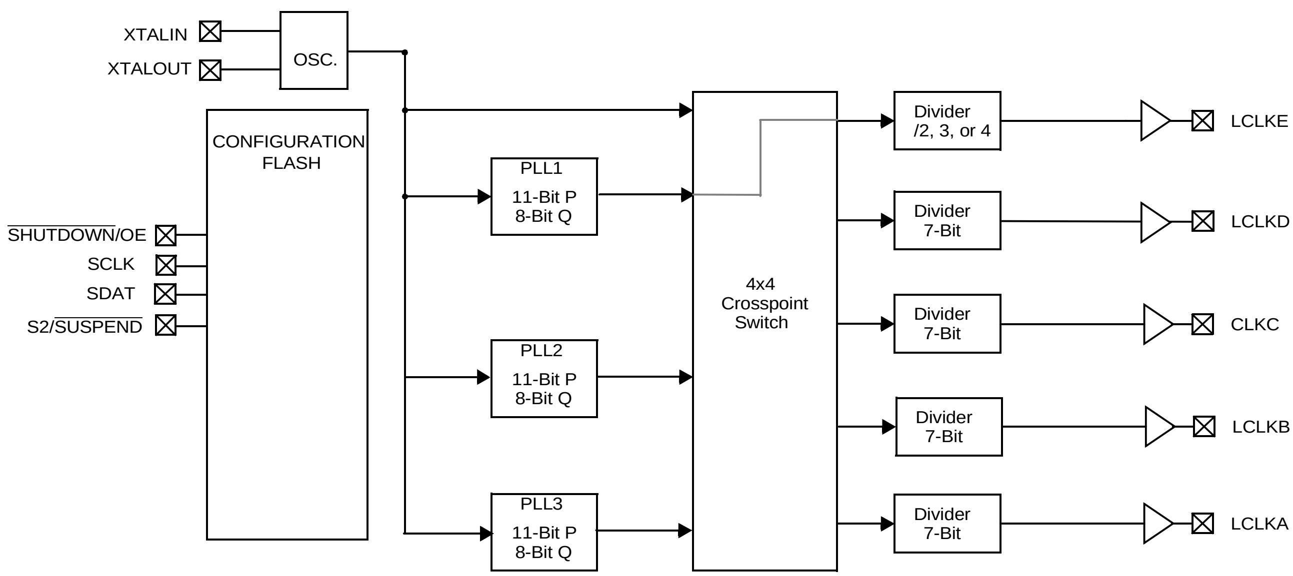
Logic Block Diagram - CY22393



Logic Block Diagram - CY22394

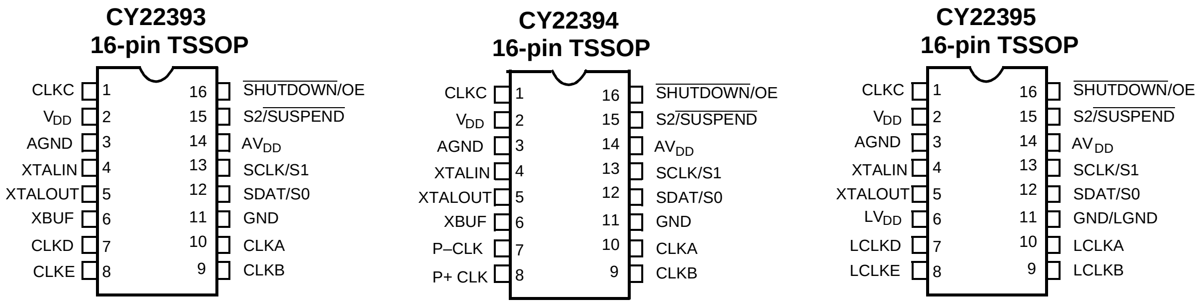


Logic Block Diagram - CY22395



LCLKA, LCLKB, LCLKD, LCLKE referenced to LV_{DD}

Pin Configurations



Pin Summary

Name	Pin Number CY22393	Pin Number CY22394	Pin Number CY22395	Description
CLKC	1	1	1	Configurable clock output C
V_{DD}	2	2	2	Power supply
AGND	3	3	3	Analog Ground
XTALIN	4	4	4	Reference crystal input or external reference clock input
XTALOUT	5	5	5	Reference crystal feedback
XBUF	6	6	N/A	Buffered reference clock output
LV_{DD}	N/A	N/A	6	Low Voltage Clock Output Power Supply
CLKD or LCLKD	7	N/A	7	Configurable clock output D; LCLKD referenced to LVDD
P–CLK	N/A	7	N/A	LV PECL Output[1]
CLKE or LCLKE	8	N/A	8	Configurable clock output E; LCLKE referenced to LVDD
P+ CLK	N/A	8	N/A	LV PECL Output[1]
CLKB or LCLKB	9	9	9	Configurable clock output B; LCLKB referenced to LVDD
CLKA or LCLKA	10	10	10	Configurable clock output A; LCLKA referenced to LVDD
GND/LGND	11	11	11	Ground
SDAT/S0	12	12	12	Two Wire Serial Port Data. S0 value latched during startup.
SCLK/S1	13	13	13	Two Wire Serial Port Clock. S1 value latched during startup.
AV_{DD}	14	14	14	Analog Power Supply
S2/ SUSPEND	15	15	15	General Purpose Input for Frequency Control; bit 2. Optionally Suspend mode control input.
SHUTDOWN/ OE	16	16	16	Places outputs in three-state condition and shuts down chip when LOW. Optionally, only places outputs in three-state condition and does not shut down chip when LOW.

Note:
1. LV PECL outputs require an external termination network.

Operation

The CY22393, CY22394, and CY22395 are a family of parts designed as upgrades to the existing CY22392 device. These parts have similar performance to the CY22392, but provide advanced features to meet more demanding applications.

The clock family has three PLLs which, when combined with the reference, allow up to four independent frequencies to be output on up to six pins. These three PLLs are completely programmable.

Configurable PLLs

PLL1 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL1 is sent to two locations: the crosspoint switch; PECL output (CY22394). The output of PLL1 is also sent to a /2, /3, or /4 synchronous post-divider that is output through CLKE. The frequency of PLL1 can be changed via serial programming or by external CMOS inputs, S0, S1, S2. See the following section on General-Purpose Inputs for more detail.

PLL2 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL2 is sent to the crosspoint switch. The frequency of PLL2 can be changed via serial programming.

PLL3 generates a frequency that is equal to the reference divided by an 8-bit divider (Q) and multiplied by an 11-bit divider in the PLL feedback loop (P). The output of PLL3 is sent to the crosspoint switch. The frequency of PLL3 can be changed via serial programming.

General-Purpose Inputs

S0, S1, and S2 are general-purpose inputs that can be programmed to allow for eight different frequency settings. Options that may be switched with these general purpose inputs are as follows; the frequency of PLL1, the output divider of CLKB, and the output divider of CLKA. Since S0 and S1 are also used for the serial interface, the values of these pins are latched during start-up.

CLKA and CLKB both have 7-bit dividers that point to one of two programmable settings (register 0 and register 1). Both clocks share a single register control, so both must be set to register 0, or both must be set to register 1.

For example: the part may be programmed to use S0, S1, and S2 (0,0,0 to 1,1,1) to control eight different values of P and Q on PLL1. For each PLL1 P and Q setting, one of the two CLKA and CLKB divider registers can be chosen. Any divider change as a result of switching S0, S1, or S2 is guaranteed to be glitch free.

Crystal Input

The input crystal oscillator is an important feature of this family of parts because of its flexibility and performance features.

The oscillator inverter has programmable drive strength. This allows for maximum compatibility with crystals from various manufacturers, process, performance, and quality.

The input load capacitors are placed on-die to reduce external component cost. These capacitors are true parallel-plate capacitors for ultra-linear performance. These were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. Non-linear (FET gate) crystal load capacitors should not be used for MPEG, POTS dial tone, Communications, or other applications that are sensitive to absolute frequency requirements.

The value of the load capacitors is determined by 6 bits in a programmable register. The load capacitance can be set with a resolution of 0.375 pF for a total crystal load range of 6 pF to 30 pF.

Digital VCXO

The serial programming interface may be used to dynamically change the capacitor load value on the crystal. A change in crystal load capacitance corresponds with a change in the reference frequency.

For special pullable crystals specified by Cypress, the capacitance pull range is +150 ppm to –150 ppm from mid-range.

Be aware that adjusting the frequency of the reference will affect all frequencies on all PLLs in a similar manner since all frequencies are derived from the single reference.

Output Configuration

Under normal operation there are four internal frequency sources that may be routed via a programmable crosspoint switch to any of the four programmable 7-bit output dividers. The four sources are: reference, PLL1, PLL2, and PLL3. The following is a description of each output.

CLKA's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. See the section on General Purpose Inputs for more information.

CLKB's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one of two programmable registers. See the section on General Purpose Inputs for more information.

CLKC's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register.

CLKD's output originates from the crosspoint switch and goes through a programmable 7-bit post divider. The 7-bit post divider derives its value from one programmable register. For the CY22394, CLKD is brought out as the complimentary version of a LV PECL Clock referenced to CLKE, bypassing both the crosspoint switch and 7-bit post divider.

CLKE's output originates from PLL1 and goes through a post divider that may be programmed to /2, /3, or /4. For the CY22394, CLKE is brought out as an LV PECL Clock, bypassing the post divider.

XBUF is simply the buffered reference.

The Clock outputs have been designed to drive a single point load with a total lumped load capacitance of 15 pF. While driving multiple loads is possible with the proper termination it is generally not recommended.

Power Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW. If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 5 µA (typical). After leaving shutdown mode, the PLLs will have to re-lock.

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.

With the serial interface, each PLL and/or output can be individually disabled. This provides total control over the power savings.

Improving Jitter

Jitter Optimization Control is useful in mitigating problems related to similar clocks switching at the same moment, causing excess jitter. If one PLL is driving more than one output, the negative phase of the PLL can be selected for one of the outputs (CLKA–CLKD). This prevents the output edges from aligning, allowing superior jitter performance.

In addition to providing a low-voltage option, the CY22395 can be used in applications requiring lower jitter. The LV_{DD} pin can be set to the normal operating voltage and used to reduce the crosstalk between outputs.

Power Supply Sequencing

For parts with multiple V_{DD} pins, there are no power supply sequencing requirements. The part will not be fully operational until all V_{DD} pins have been brought up to the voltages specified in the “Operating Conditions” table.

All grounds should be connected to the same ground plane.

CyClocks RT™ Software

CyClocks RT is our second-generation application that allows users to configure this family of devices. The easy-to-use interface offers complete control of the many features of this family including input frequency, PLL and output frequencies, and different functional options. Data sheet frequency range limitations are checked and performance tuning is automatically applied. You can download a copy of CyClocks RT for free on Cypress’s web site at www.cypress.com.

Cyclocks RT is used to generate P, Q, and divider values used in serial programming. There are many internal frequency rules which are not documented in this data sheet, but are required for proper operation of the device. These rules can be checked by using the latest version of Cyclocks RT.

Serial Interface Operation

The serial port uses industry-standard signaling in both standard and fast modes. This section describes the unique features of the serial interface in this family of devices.

Device Address

The device address is a 7-bit value that is configured during Field Programming. By programming different device addresses, two or more parts can be connected to the serial interface and be independently controlled. The device address is combined with a read/write bit as the LSB and is sent after each start bit.

Memory Address

This family of devices supports 1-byte memory addressing. The memory address is always sent after each Device Address/Write bit combination. It describes the memory location within the device to be accessed. The memory address is incremented after each acknowledge, allowing sequential memory access.

For driven clock inputs the input load capacitors may be completely bypassed. This enables the clock chip to accept driven frequency inputs up to 166 MHz. If the application requires a driven input, then XTALOUT must be left floating.

To read a memory location, a memory address must first be sent specifying the location. This is followed by a repeated start bit and the Device Address/Read byte, after which the desired memory location is available for reading.

Valid memory locations are shown in the “Serial Programming Memory Bitmap” section. All registers are read and write capable. Some reserved registers are not shown. For proper device operation, do not write data outside of the addresses shown.

Memory Data

For writes, all of the bytes sent to the device between the Memory Address and a stop bit or repeated start bit are interpreted as data. Each data byte is written to the current memory address, which is incremented after each acknowledge.

For reads, data is shifted out immediately after the Device Address/Read byte. Bytes are shifted out sequentially until a not-acknowledge followed by a stop bit are received by the device.

Dynamic Updates

The output divider registers are not synchronized with the output clocks. Changing the divider value of an active output will likely cause a glitch on that output.

PLL P and Q data is spread between three bytes. Each byte becomes active on the acknowledge for that byte, so changing P and Q data for an active PLL will likely cause the PLL try to lock on an out-of-bounds condition. For this reason, it is recommended that the PLL being programmed be turned off during the update. This can be done by setting the PLL*_En bit LOW.

PLL1, CLKA, and CLKB each have multiple registers supplying data. Programming these resources can be accomplished safely by always programming an inactive register, and then transitioning to that register. This allows these resources to stay on during programming.

The serial interface is active even with the $\overline{\text{SHUTDOWN}}$/OE pin LOW as the serial interface logic uses static components and is completely self-timed. The part will not meet the I_{DDS} current limit with transitioning inputs.

Serial Programming Memory Bitmap

Addr	DivSel	b7	b6	b5	b4	b3	b2	b1	b0
08	0	ClkA_FS[0]	ClkA_Div[6:0]						
09	1	ClkA_FS[0]	ClkA_Div[6:0]						
0A	0	ClkB_FS[0]	ClkB_Div[6:0]						
0B	1	ClkB_FS[0]	ClkB_Div[6:0]						
0C	-	ClkC_FS[0]	ClkC_Div[6:0]						
0D	-	ClkD_FS[0]	ClkD_Div[6:0]						
0E	-	ClkD_FS[2:1]		ClkC_FS[2:1]		ClkB_FS[2:1]		ClkA_FS[2:1]	
0F	-	Clk{C,X}_ACAdj[1:0]		Clk{A,B,D,E}_ACAdj[1:0]		PdnEn	Xbuf_OE	ClkE_Div[1:0]	
10	-	ClkX_DCAdj[1]		Clk{D,E}_DCAdj[1]		ClkC_DCAdj[1]		Clk{A,B}_DCAdj[1]	
11	-	PLL2_Q[7:0]							
12	-	PLL2_P[7:0]							
13	-	Reserved	PLL2_En	PLL2_LF[2:0]			PLL2_PO	PLL2_P[9:8]	
14	-	PLL3_Q[7:0]							
15	-	PLL3_P[7:0]							
16	-	Reserved	PLL3_En	PLL3_LF[2:0]			PLL3_PO	PLL3_P[9:8]	
17	-	Osc_Cap[5:0]						Osc_Drv[1:0]	

Addr	S2,1,0	b7	b6	b5	b4	b3	b2	b1	b0
40	000	PLL1_Q[7:0]							
41		PLL1_P[7:0]							
42		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
43	001	PLL1_Q[7:0]							
44		PLL1_P[7:0]							
45		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
46	010	PLL1_Q[7:0]							
47		PLL1_P[7:0]							
48		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
49	011	PLL1_Q[7:0]							
4A		PLL1_P[7:0]							
4B		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
4C	100	PLL1_Q[7:0]							
4D		PLL1_P[7:0]							
4E		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
4F	101	PLL1_Q[7:0]							
50		PLL1_P[7:0]							
51		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
52	110	PLL1_Q[7:0]							
53		PLL1_P[7:0]							
54		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	
55	111	PLL1_Q[7:0]							
56		PLL1_P[7:0]							
57		DivSel	PLL1_En	PLL1_LF[2:0]			PLL1_PO	PLL1_P[9:8]	

Memory Bitmap Definitions

Clk{A–D}_Div[6:0]

Each of the four main output clocks (CLKA–CLKD) features a 7-bit linear output divider. Any divider setting may be used between 1 and 127, odd divide values are automatically duty-cycle corrected. Setting a divide value of zero powers down the divider and forces the output to a three-state condition.

CLKA and CLKB have two divider registers, selected by the DivSel bit (which in turn is selected by S2, S1, and S0). This allows dynamic changing of the output divider value. For the CY22394 device, ClkD_Div = 000001.

ClkE_Div[1:0]

CLKE has a simpler divider. For the CY22394 device,

ClkE_Div[1:0]	ClkE Output
00	Off
01	PLL1 0° Phase/4
10	PLL1 0° Phase/2
11	PLL1 0° Phase/3

ClkE_Div = 01.

Clk*_FS[2:0]

Each of the four main output clocks (CLKA–CLKD) has a three-bit code that determines the clock sources for the output divider. The available clock sources are; Reference, PLL1, PLL2, and PLL3. Each PLL provides both positive and negative phased outputs, for a total of seven clock sources.

Clk*_FS[2:0]	Clock Source
000	Reference Clock
001	Reserved
010	PLL1 0° Phase
011	PLL1 180° Phase
100	PLL2 0° Phase
101	PLL2 180° Phase
110	PLL3 0° Phase
111	PLL3 180° Phase

Xbuf_OE

Clk*_DCAdj[1:0]	Output Drive Strength
00	–30% of nominal
01	Nominal
10	+15% of nominal
11	+50% of nominal

This bit enables the XBUF output when high. For the CY22395, Xbuf_OE=0.

PdnEn

This bit selects the function of the $\overline{\text{SHUTDOWN}}$/OE pin. When this bit is HIGH, the pin is an active LOW shutdown control. When this bit is LOW, this pin is an active HIGH output enable control.

Clk*_ACAdj[1:0]

These bits modify the output predrivers, changing the duty cycle through the pads. These are nominally set to 01, with a higher value shifting the duty cycle higher. The performance of the nominal setting is guaranteed.

Clk*_DCAdj[1:0]

These bits modify the DC drive of the outputs. The performance of the nominal setting is guaranteed.

PLL*_Q[7:0]

PLL*_P[9:0]

PLL*_P0

These are the 8-bit Q value and 11-bit P values that determine the PLL frequency. The formula is:

$$F_{PLL} = F_{REF} \times \left(\frac{P_T}{Q_T}\right)$$

$$P_T = (2 \times (P + 3)) + PO$$

$$Q_t = Q + 2$$

PLL*_LF[2:0]

These bits adjust the loop filter to optimize the stability of the PLL. These should always be set according to the following table.

PLL*_LF[2:0]	P_T Min	P_T Max
000	16	231
001	232	626
010	627	834
011	835	1043
100	1044	1600

PLL*_En

This bit enables the PLL when high. If PLL2 or PLL3 are not enabled, then any output selecting the disabled PLL must have a divider setting of zero (off). Since the PLL1_En bit is dynamic, internal logic automatically turns off dependent outputs when PLL1_En goes low.

DivSel

This bit controls which register is used for the CLKA and CLKB dividers.

OscCap[5:0]

This controls the internal capacitive load of the oscillator. The approximate effective crystal load capacitance is:

$$C_{LOAD} = 6pF + (OscCap \times 0.375pF)$$

Set to zero for external reference clock.

OscDrv[1:0]

These bits control the crystal oscillator gain setting. These should always be set according to the following table. The parameters are the Crystal Frequency, Internal Crystal Parasitic

Resistance (available from the manufacuturer), and the OscCap setting during crystal start-up (which occurs when power is applied, or after shutdown is released). If in doubt, use the next higher setting.

OscCap	00H–20H		20H–30H		30H–40H	
Crystal R	30Ω	60Ω	30Ω	60Ω	30Ω	60Ω
8–15 MHz	00	01	01	10	01	10
15–20 MHz	01	10	01	10	10	10
20–25 MHz	01	10	10	10	10	11
25–30 MHz	10	10	10	11	11	NA

Reserved

These bits must be programmed LOW for proper operation of the device.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage..–0.5V to +7.0V

DC Input Voltage ....–0.5V to + (AV_{DD} + 0.5V)

Storage Temperature................................. –65°C to +125°C

Max. Hand Soldering Temperature (10 sec)................260°C

Junction Temperature ....125°C

Data Retention @ Tj=125°C................................> 10 years

Maximum Programming Cycles.......................................100

Package Power Dissipation .... 350 mW

Static Discharge Voltage (per MIL-STD-883, Method 3015) ≥ 2000V

Latch up (per JEDEC 17) .... ≥ ± 200 mA

Operating Conditions[1]

Parameter	Description	Part Numbers	Min.	Typ	Max.	Unit
$V_{DD}/AV_{DD}/LV_{DD}$	Supply Voltage	All	3.135	3.3	3.465	V
LV_{DD}	2.5V Output Supply Voltage	22395	2.375	2.5	2.625	V
T_A	Commercial Operating Temperature, Ambient	All	0		+70	°C
	Industrial Operating Temperature, Ambient	All	–40		+85	°C
C_{LOAD_OUT}	Max. Load Capacitance	All			15	pF
f_{REF}	External Reference Crystal	All	8		30	MHz
	External Reference Clock[2], Commercial	All	1		166	MHz
	External Reference Clock[2], Industrial	All	1		150	MHz

3.3V Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current[3]	V_{OH} = (L)V_{DD} - 0.5, (L)V_{DD}= 3.3V	12	24		mA
I_{OL}	Output Low Current[3]	V_{OH} = 0.5, (L)V_{DD}= 3.3V	12	24		mA
C_{LOAD_XTAL}	Crystal Load Capacitance[3]	Across adjustable range, nominal process	6		30	pF
C_{LOAD_IN}	Input Pin Capacitance[3]	Except crystal pins		7		pF
V_{IH}	HIGH-Level Input Voltage	CMOS levels, % of AV_{DD}	70%			AV_{DD}
V_{IL}	LOW-Level Input Voltage	CMOS levels, % of AV_{DD}			30%	AV_{DD}
I_{IH}	Input HIGH Current	V_{IN} = AV_{DD}–0.3V		<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.3V		<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs			10	µA
I_{DD}	Total Power Supply Current	3.3V Power Supply; 2 outputs @ 20 MHz; 4 outputs @ 40MHz		50		mA
		3.3V Power Supply; 2 outputs @ 166 MHz; 4 outputs @ 83 MHz		100		mA
I_{DDS}	Total Power Supply Current in Shutdown Mode	Shutdown active		5	20	µA

Notes:
1. Unless otherwise noted, Electrical and Switching Characteristics are guaranteed across these operating conditions.
2. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
3. Guaranteed by design, not 100% tested.

2.5V Electrical Characteristics (CY22395 only)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$I_{OH\_2.5}$	Output High Current[3]	$V_{OH} = LV_{DD} – 0.5$, $LV_{DD} = 2.5V$	8	16		mA
$I_{OL\_2.5}$	Output Low Current[3]	$V_{OH} = 0.5$, $LV_{DD}= 2.5V$	8	16		mA

3.3V Switching Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency[3, 4]	Clock output limit, CMOS, Commercial			200	MHz
		Clock output limit, CMOS, Industrial			166	MHz
		Clock output limit, PECL, Commercial (CY22394 only)			400	MHz
		Clock output limit, PECL, Industrial (CY22394 only)			333	MHz
t_2	Output Duty Cycle[3, 5]	Duty cycle for outputs, defined as $t_2 \div t_1$, Fout<100 MHz, divider>=2, measured at $V_{DD}/2$	45%	50%	55%	
		Duty cycle for outputs, defined as $t_2 \div t_1$, Fout>100 MHz or divider=1, measured at $V_{DD}/2$	40%	50%	60%	
t_3	Rising Edge Slew Rate[3]	Output clock rise time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_4	Falling Edge Slew Rate[3]	Output clock fall time, 20% to 80% of V_{DD}	0.75	1.4		V/ns
t_5	Output three-state Timing[3]	Time for output to enter or leave three-state mode after SHUTDOWN/OE switches		150	250	ns
t_6	Clock Jitter[3, 6]	Peak-to-peak period jitter, CLK outputs measured at $V_{DD}/2$		400		ps
v_7	P+/P- Crossing Point[3]	Crossing point referenced to Vdd/2, balanced resistor network (CY22394 only)	–0.2	0	0.2	V
t_8	P+/P- Jitter[3, 5]	Peak-to-peak period jitter, P+/P– outputs measured at crossing point (CY22394 only)		200		ps
t_9	Lock Time[3]	PLL Lock Time from Power-up		0.3	3	ms

2.5v Switching Characteristics (CY22395 only)

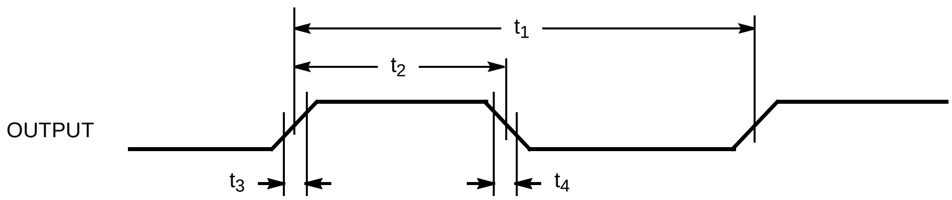
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$1/t_{1\_2.5}$	Output Frequency	Clock output limit, LVCMOS			133	MHz
$t_{2\_2.5}$	Output Duty Cycle[3, 4]	Duty cycle for outputs, defined as $t_2 \div t_1$ measured at $LV_{DD}/2$	40%	50%	60%	
$t_{3\_2.5}$	Rising Edge Slew Rate[3]	Output clock rise time, 20% to 80% of LV_{DD}	0.5	1.0		V/ns
$t_{4\_2.5}$	Falling Edge Slew Rate[3]	Output clock fall time, 20% to 80% of LV_{DD}	0.5	1.0		V/ns

Notes:

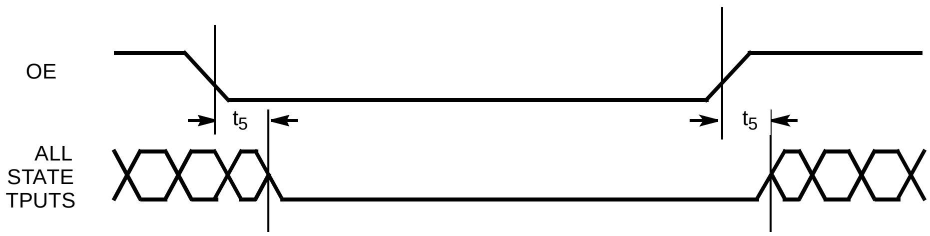
4. Guaranteed to meet 20% - 80% output thresholds, duty cycle, and crossing point specifications.
5. Reference Output duty cycle depends on XTALIN duty cycle.
6. Jitter varies significantly with configuration. Reference Output jitter depends on XTALIN jitter and edge rate.

Switching Waveforms

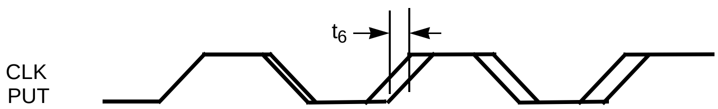
All Outputs, Duty Cycle and Rise/Fall Time



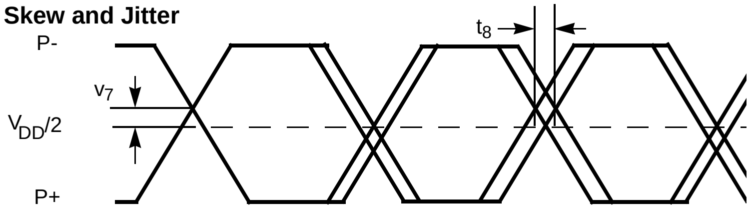
Three-State Timing



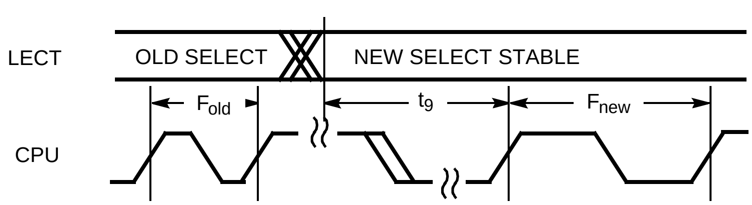
CLK Output Jitter



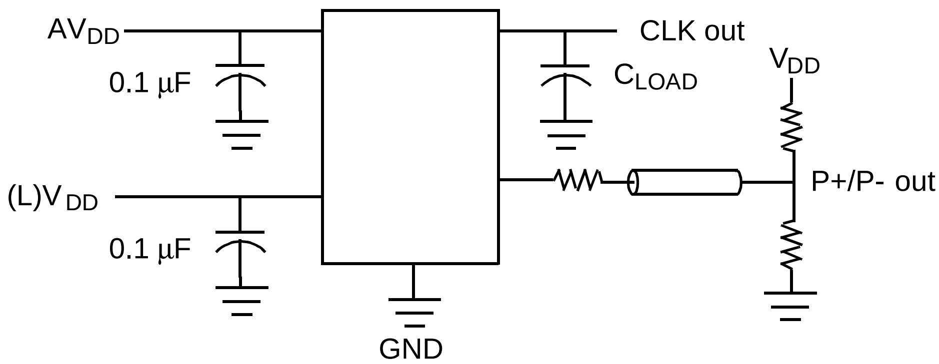
Skew and Jitter



Frequency Change



Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY22393FC	Z16	16-TSSOP	Commercial (T_A=0°C to 70°C)	3.3V
CY22393FI	Z16	16-TSSOP	Industrial (T_A=-40°C to 85°C)	3.3V
CY22394FC	Z16	16-TSSOP	Commercial (T_A=0°C to 70°C)	3.3V
CY22394FI	Z16	16-TSSOP	Industrial (T_A=-40°C to 85°C)	3.3V
CY22395FC	Z16	16-TSSOP	Commercial (T_A=0°C to 70°C)	3.3V,2.5V
CY22395FI	Z16	16-TSSOP	Industrial (T_A=-40°C to 85°C)	3.3V,2.5V

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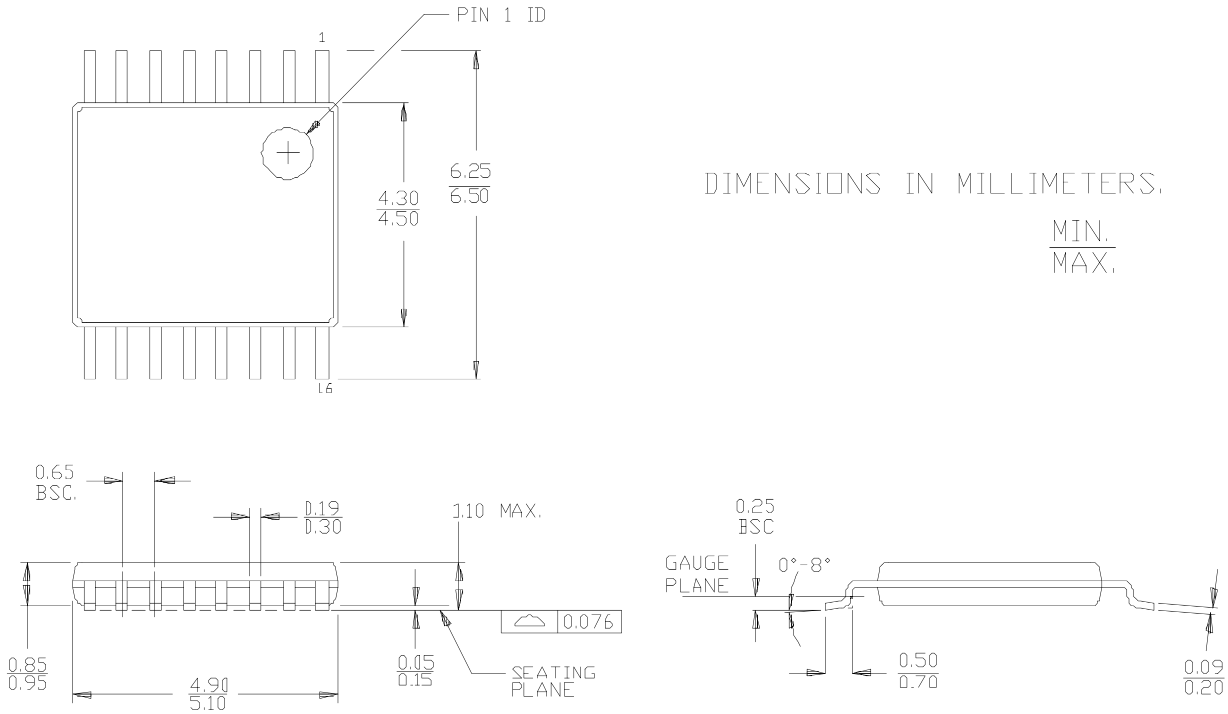
Package Diagrams

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



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