CY2300

Phase-Aligned System Clock

Features	Benefits
• **4-multiplier configuration**	1/2x, 1x, $\overline{1x}$, 2x Ref
• **Single phase-locked loop architecture**	10 MHz to 166.67 MHz operating range (reference input from 20 MHz to 83.33 MHz)
• **Phase Alignment**	All outputs will have a consistent phase relationship with each other and the reference input
• **Low jitter, high accuracy outputs**	Meets critical timing requirements
• **Output enable pin**	Enables design flexibility and lower power consumption
• **3.3V operation**	Supports industry standard design platforms
• **5V Tolerant input**	Allows flexibility on Reference input
• **Internal loop filter**	Alleviates the need for external components
• **8-pin 150-mil SOIC package**	Industry standard packaging saves on board space
• **Commercial and Industrial Temperature available**	Suitable for wide spectrum of applications

Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2300SC	4	20 MHz–83.33 MHz	10 MHz–166.67 MHz	Commercial Temperature
CY2300SI	4	20 MHz–83.33 MHz	10 MHz–166.6 7MHz	Industrial Temperature

Functional Description

The CY2300 is a 4-output 3.3V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

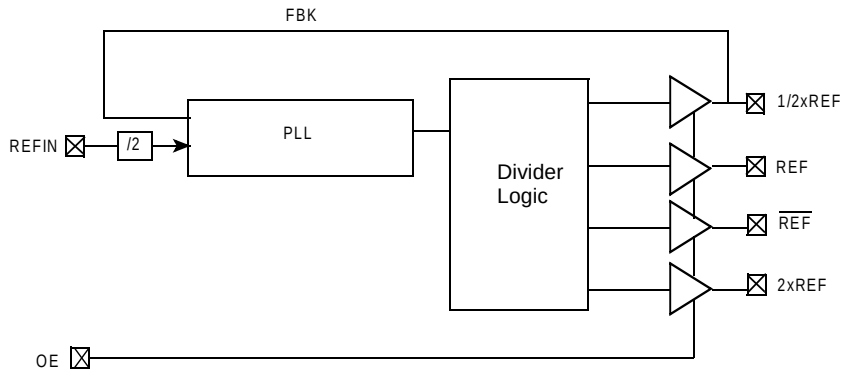
The part allows the user to obtain 1/2x, 1x, $\overline{1x}$ and 2x REFIN output frequencies on respective output pins.

The part has an on-chip PLL which locks to an input clock presented on the REFIN pin. The input-to-output skew is guaranteed to be less than ±200 ps, and output-to-output skew is guaranteed to be less than 200 ps.

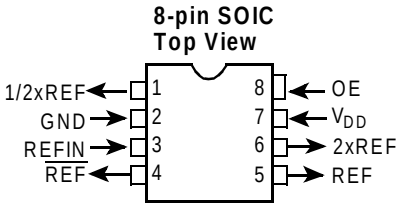
Multiple CY2300 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.

The CY2300 is available in commercial and industrial temperature ranges.

Block Diagram



Pin Configuration



Pin Description

Pin	Signal[1]	Description
1	1/2xREF	Clock output, 1/2x Reference
2	GND	Ground
3	REFIN	Input Reference frequency, 5V tolerant input
4	$\overline{\text{REF}}$	Clock output $\overline{\text{Reference}}$
5	REF	Clock output Reference
6	2xREF	Clock output, 2x Reference
7	VDD	3.3V Supply
8	OE	Output Enable (weak pull-up)

Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage (Except Ref) ..... –0.5V to V_{DD} + 0.5V

DC Input Voltage REF ..... –0.5 to 7V

Storage Temperature ..... –65°C to +150°C

Max. Soldering Temperature (10 sec.) ..... 260°C

Junction Temperature ..... 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions for CY2300SC Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, Fout < 133.33 MHz		18	pF
	Load Capacitance,133.33 MHz < Fout < 166.67 MHz		12	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for CY2300SC Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		100	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		50	µA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –8 mA	2.4		V
I_{DD}	Supply Current	Unloaded outputs, REFIN=66 MHz		45	mA
		Unloaded outputs, REFIN=33 MHz		32	mA
		Unloaded outputs, REFIN=20 MHz		18	mA

Notes:
1. Weak pull-down on all outputs.
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.

Switching Characteristics for CY2300SC Commercial Temperature Devices

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency	18-pF load	10		133.33	MHz
		12-pF load			166.67	MHz
	Duty Cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Rise Time[3]	Measured between 0.8V and 2.0V			1.20	ns
t_4	Fall Time[3]	Measured between 0.8V and 2.0V			1.20	ns
t_5	Output to Output Skew on rising edges[3]	All outputs equally loaded Measured at $V_{DD}/2$			200	ps
t_6	Delay, REFIN Rising Edge to Output Rising Edge[3]	Measured at $V_{DD}/2$ from REFIN to any output			±200	ps
t_7	Device to Device Skew[3]	Measured at $V_{DD}/2$ on the 1/2xREF pin of devices (pin 1)			400	ps
t_J	Period Jitter[3]	Measured at Fout=133.33 MHz, loaded outputs, 18-pF load			±175	ps
t_{LOCK}	PLL Lock Time[3]	Stable power supply, valid clocks presented on REFIN			1.0	ms

Note:

3. All parameters are specified with equally loaded outputs.

Operating Conditions for CY2300SI Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, Fout < 133.33 MHz		15	pF
	Load Capacitance,133.33 MHz < Fout < 166.67MHz		10	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for CY2300SI Industrial Temperature Devices

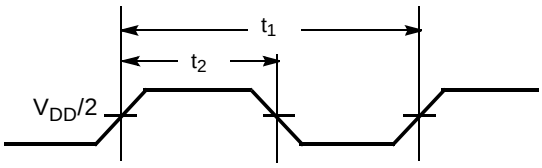
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		100	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		50	µA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –8 mA	2.4		V
I_{DD}	Supply Current	Unloaded outputs, REFIN=66 MHz		48	mA
		Unloaded outputs, REFIN=33 MHz		35	mA
		Unloaded outputs, REFIN=20 MHz		20	mA

Switching Characteristics for CY2300SI Industrial Temperature Devices

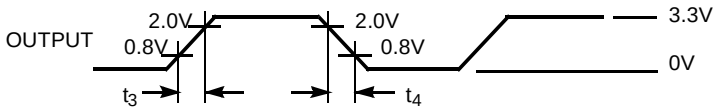
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
$1/t_1$	Output Frequency	15-pF load	10		133.33	MHz
		10-pF load			166.67	MHz
	Duty Cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Rise Time[3]	Measured between 0.8V and 2.0V			1.20	ns
t_4	Fall Time[3]	Measured between 0.8V and 2.0V			1.20	ns
t_5	Output to Output Skew on rising edges[3]	All outputs equally loaded Measured at $V_{DD}/2$			200	ps
t_6	Delay, REFIN Rising Edge to Output Rising Edge[3]	Measured at $V_{DD}/2$ from REFIN to any output			±200	ps
t_7	Device to Device Skew[3]	Measured at $V_{DD}/2$ on the 1/2xREF pin of devices (pin 1)			400	ps
t_J	Period Jitter[3]	Measured at Fout=133.33 MHz, loaded outputs, 15-pF load			±175	ps
t_{LOCK}	PLL Lock Time[3]	Stable power supply, valid clocks presented on REFIN			1.0	ms

Switching Waveforms

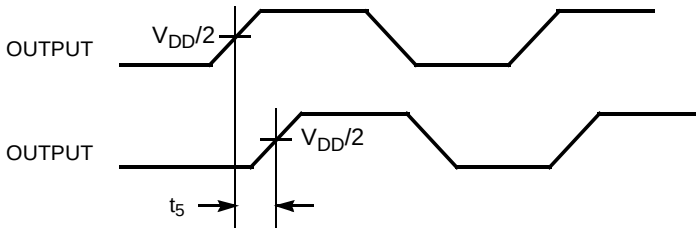
Duty Cycle Timing



All Outputs Rise/Fall Time

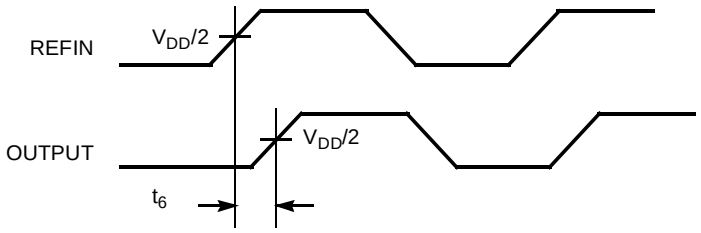


Output-Output Skew

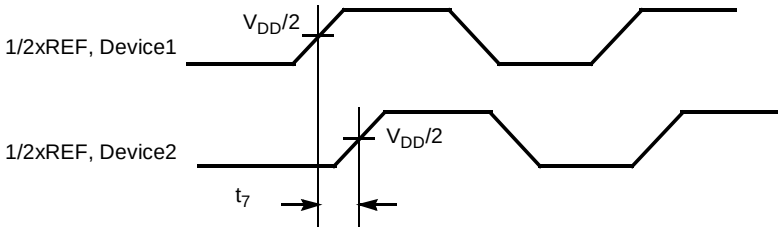


Switching Waveforms

Input-Output Propagation Delay

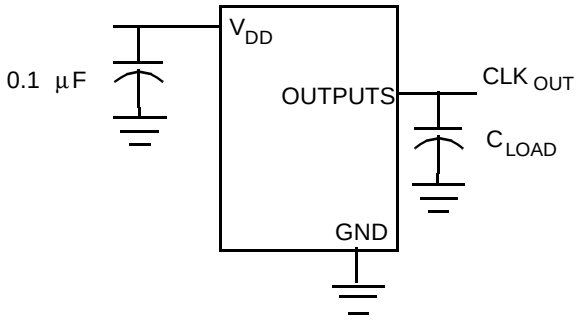


Device-Device Skew



Test Circuits

Test Circuit # 1



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2300SC	S8	8-pin 150-mil SOIC	Commercial
CY2300SI	S8	8-pin 150-mil SOIC	Industrial

Document #:38–01039–*A

Package Diagrams

8-Lead (150-Mil) Molded SOIC S8