Redundant Reference Input Switching

CY23020 Redundant Reference Input Switching

In a system, the clock reference is often thought first to fail if it is quartz crystal based. Quartz oscillators are fundamentally piezoelectric devices, and are subject to mechanical, stress, vibration, and wear-out effects. Because of this, redundant clock references are extremely useful for high-availability systems.

This is a description of the CY23020 when configured with redundant input reference sources. The intent is to give the designer some typical behavioral characteristics when operated in this mode. The timing parameters described are useful for planning the redundant reference source system timing in conjunction with the CY23020.

A block diagram representation of the connection with redundant inputs in *Figure 1*. It is assumed that REF is the primary source that eventually fails, while FBIN is the redundant source that gets switched in.

A discussion of how REF could fail and the resulting response of the CY23020 begins.The first case considered is when REF suddenly stops, and is stuck HIGH or LOW. For this, we would expect that the CY23020 LOCKED pin would go LOW, indicating loss of internal PLL lock. LOCKED signal can then be interpreted by the system as to whether to switch in the FBIN signal. The LOCKED signal from the CY23020 is designed to respond quickly so that the system has adequate time to determine whether to switch. Figure 2 shows the fast response of LOCKED status to a 190-MHz REF that suddenly stuck HIGH. Also notice that the CY23020 outputs continue to run after the REF input stopped (QA1 output in the measurement).

Black, or top waveform = REF input to CY23020

Green, or middle waveform = LOCKED output from the CY23020

Red, or bottom waveform = QA1 output from the CY23020

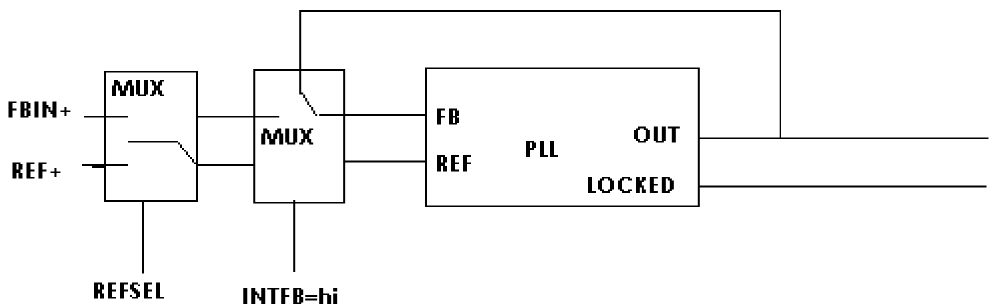

Figure 1. Block Diagram

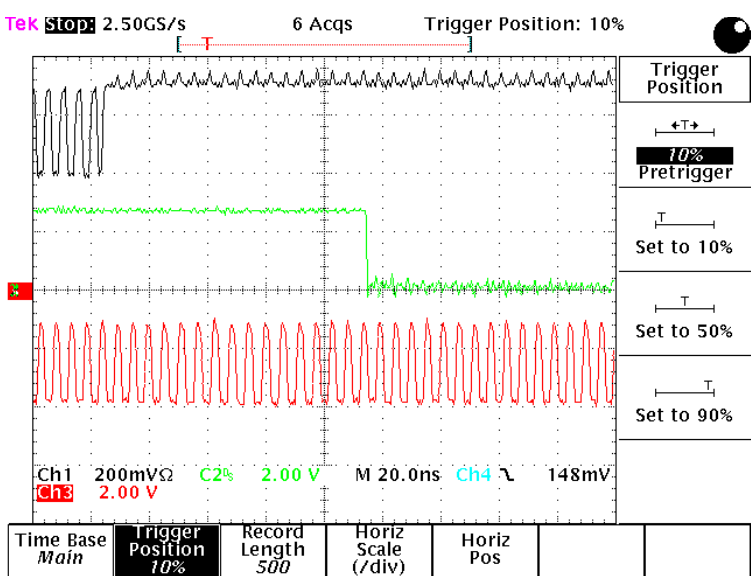

Figure 2.

The CY23020 is designed to have its output frequency decay slowly after the REF input stops. This enhances the ability of the system to keep running, switch in the redundant reference, and possibly keep the system going without a crash. *Figure 3* shows the typical decay time of the CY23020 outputs after REF has stopped.

Another case to consider is when the desired REF frequency changes to some different (error) frequency. The error frequency can be either higher or lower than the intended REF frequency. The measurement in *Figure 4* shows the case where REF was initially 190 MHz, then fell to 75 MHz. This shows the typical fast response to the unlock condition.

Black, or top waveform = falling edge trigger when input switched from 190 MHz down to 75 MHz

Green, or middle waveform = LOCKED output from the CY23020. (lost lock here)

Red, or bottom waveform = QA1 output from the CY23020

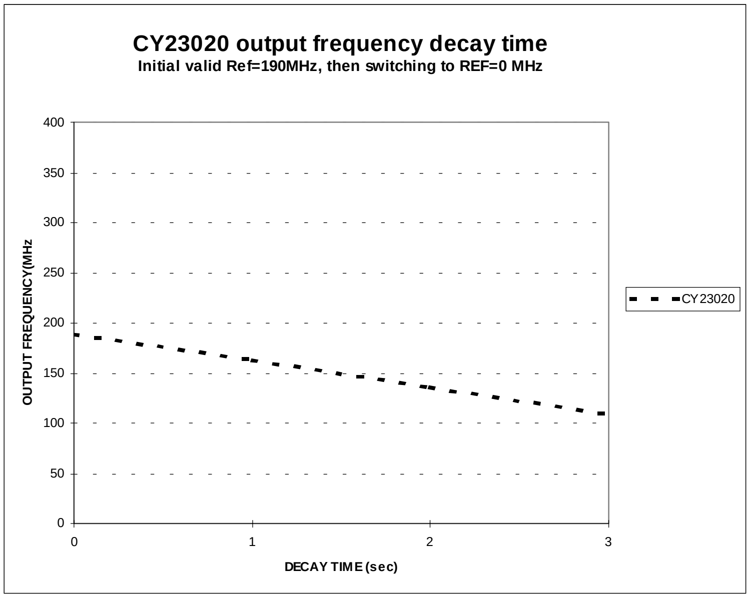

Figure 3.

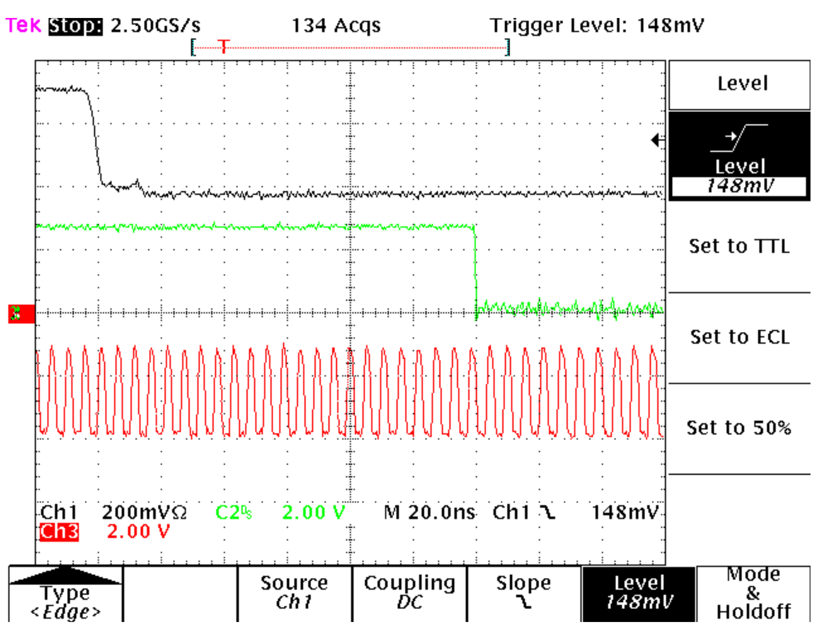

Figure 4.

Figure 5 shows typical measured data of response time of lost lock status. The error frequencies shown are below the intended correct REF target frequency of 190 MHz.

Figure 6 shows typical measured data of alternative error frequencies. The error frequency range is both above and below the intended REF target frequency (75 MHz for this set of measurements).

Once the system decides to switch in the redundant source through FBIN pins, the CY23020 LOCKED condition must be considered. As shown previously, the CY23020 output frequency will predictably drift while unlocked. It will take time for the CY23020 PLL to lock to the new redundant reference source and produce the correct frequency. This is called the lock time. The CY23020 is considered locked when the LOCKED pin goes HIGH.

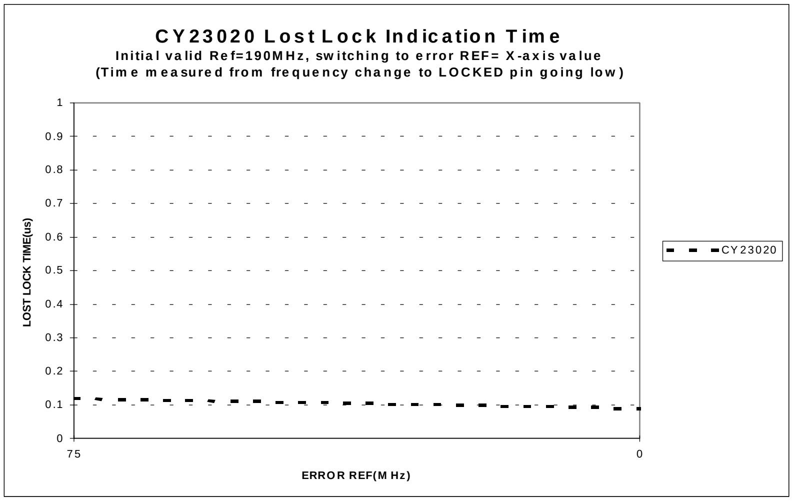

Figure 5.

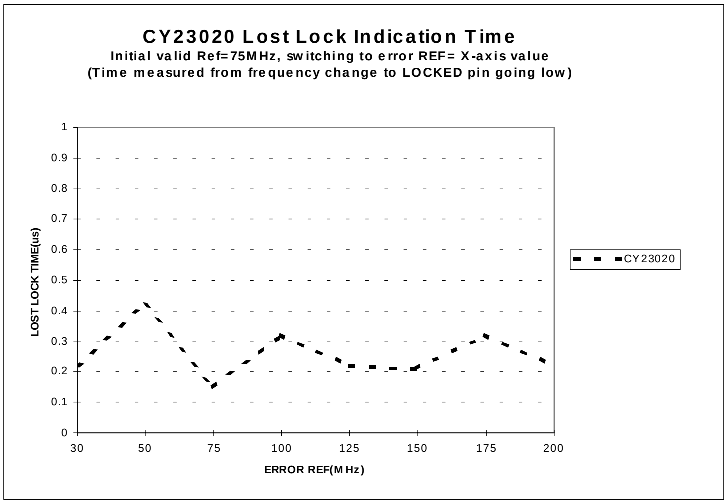

Figure 6.

Figure 7 is a typical measurement of lock time. The intended correct frequency is 190 MHz, but the CY23020 was allowed to drift down to 75 MHz. The REFSEL pin was then switched HIGH, and the resulting lock time is displayed.

Black, or top waveform = REFSEL input switched LOW to HIGH. So internal MUX switches from 75 MHz failed reference over to 190 MHz correct redundant reference.

Green, or middle waveform = LOCKED output from the CY23020. (achieved lock here)

This shows the typical fast response to the lock condition.

Figure 8 shows typical measurements for lock time to other frequencies. The error frequency happens to be 75 MHz, and the intended correct frequency is indicated along the X-axis.

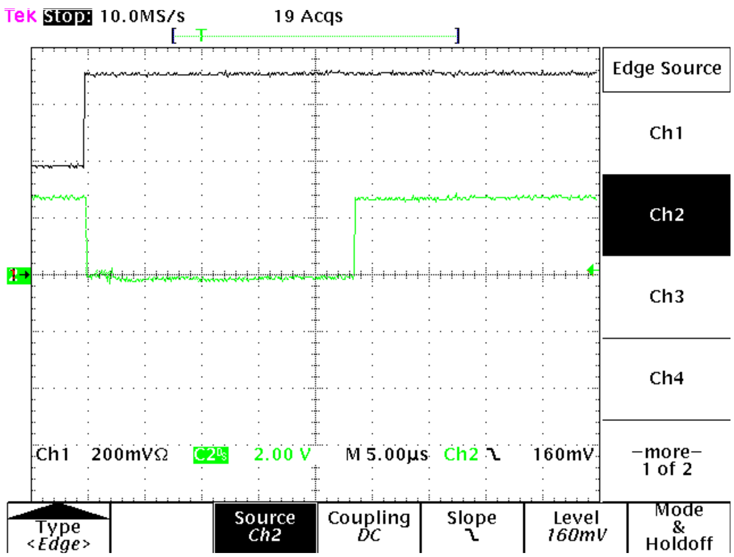

Figure 7.

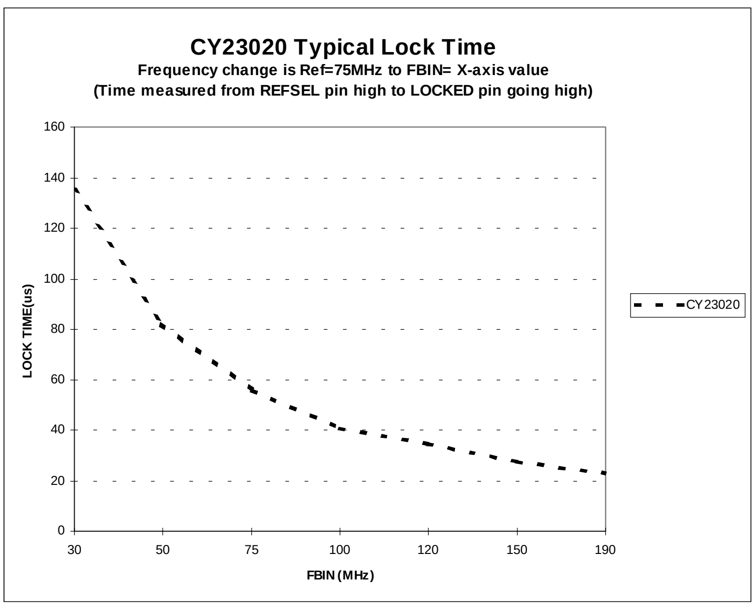

Figure 8.

A scenario/limitation is now considered. Suppose for some reason, the primary reference frequency, while failing, changes very slowly. Consider a frequency change rate of 1 MHz per ms. In this case the CY23020 is not expected to generate the unlocked condition where LOCKED pin goes LOW. This is because the CY23020 is specifically designed to be Spread Aware, and is required to track low frequency modulation of the reference input. This Spread Aware buffer preserves the special modulation profile shape of a source using spread spectrum modulation. This in turn preserves the powerful benefit of maximizing the EMI reduction. Please see Cypress application note “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFG) ICs” describing EMI reduction using spread spectrum modulation for the clock source. The other reason Spread Aware buffer performance can be important is tracking skew. That is the ability of the output to remain in phase with the reference input, even with input modulation present. Tracking skew is usually considered for synchronous portions of a design.

So if detecting a slowly changing, failing reference is deemed important, it needs to be done outside the CY23020. One could envision the need for a third reference to do this. It then can be used to compare the absolute frequency accuracy of REF and FBIN if so desired. The system detects then decides what reference to switch. The CY23020 still responds with a smoothly controlled output waveform.

The preceding information is meant as a guideline to the use of the CY23020 with redundant reference sources. In summary, the CY23020 is well suited for this application because of its fast unlock indicator, slow frequency decay time with no input, and fast lock time to the redundant reference frequency. All this gives the system the best chance of continuing to run when a reference source catastrophically fails.