CY2304

3.3V Zero Delay Buffer

Features

- **Zero input-output propagation delay, adjustable by capacitive load on FBK input**
- **Multiple configurations, see "Available Configurations" table**
- **Multiple low-skew outputs**
  - **Output-output skew less than 200 ps**
  - **Device-device skew less than 500 ps**
- **10-MHz to 133-MHz operating range**
- **Low jitter, less than 200 ps cycle-cycle**
- **Space-saving 8-pin 150-mil SOIC package**
- **3.3V operation**
- **Industrial Temperature available**

Functional Description

The CY2304 is a 3.3V zero delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven into the FBK pin, and can be obtained from one of the outputs. The input-to-output skew is guaranteed to be less than 350 ps, and output-to-output skew is guaranteed to be less than 200 ps.

The CY2304 has two banks of two outputs each.

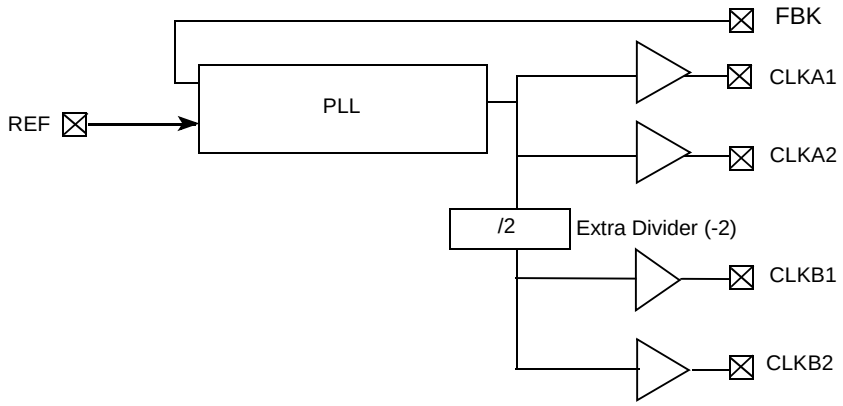
The CY2304 PLL enters a power-down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 50 μA of current draw.

Multiple CY2304 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 500 ps.

The CY2304 is available in two different configurations, as shown in the "Available Configurations" table. The CY2304–1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path.

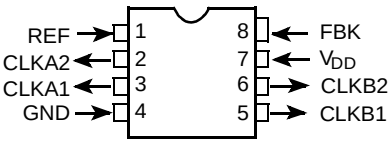
The CY2304–2 allows the user to obtain Ref and 1/2x or 2x frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin.

Logic Block Diagram for CY2304



Pin Configuration

8-pin SOIC
Top View

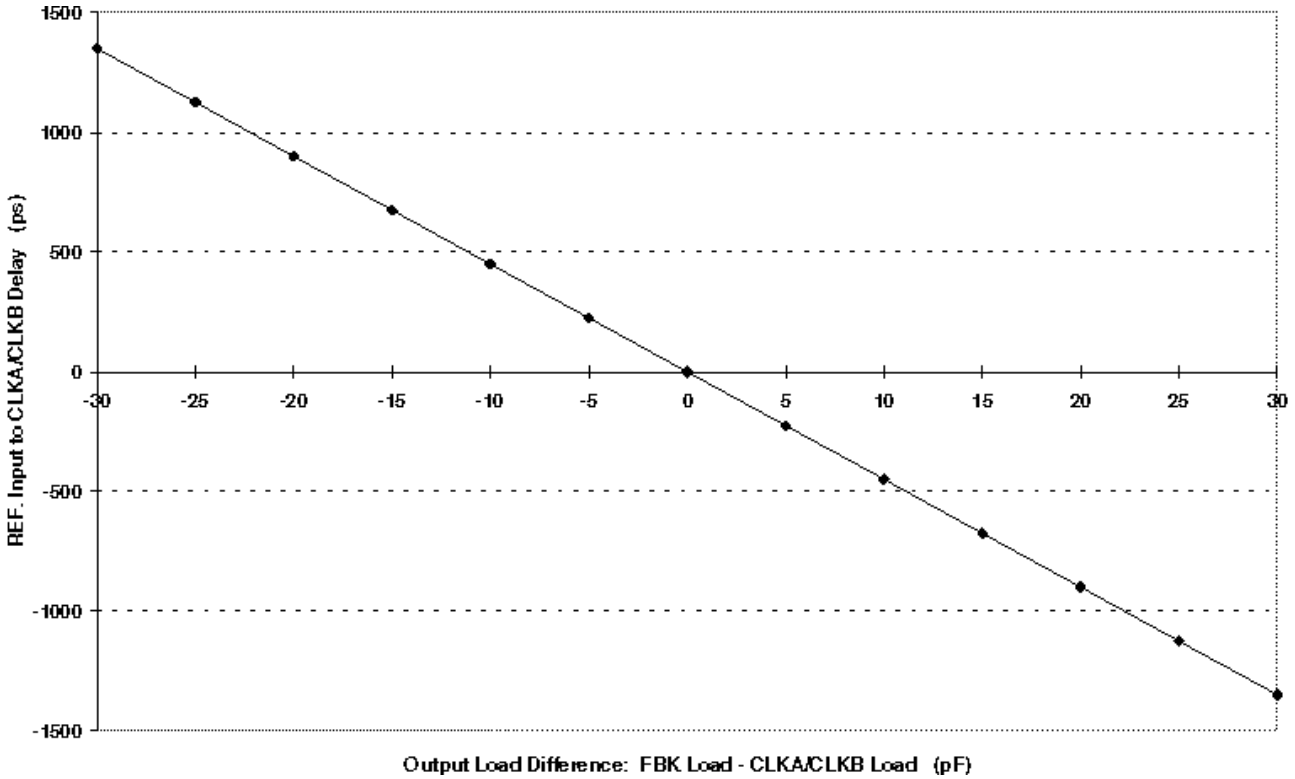


Available Configurations

Device	FBK From	Bank A Frequency	Bank B Frequency
CY2304-1	Bank A or B	Reference	Reference
CY2304-2	Bank A	Reference	Reference/2
CY2304-2	Bank B	2 x Reference	Reference

Zero Delay and Skew Control

REF. Input to CLKA/CLKB Delay vs. Difference in Loading between FBK pin and CLKA/CLKB pins



To close the feedback loop of the CY2304, the FBK pin can be driven from any of the four available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. This is shown in the graph above.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, be sure to load outputs equally. For further information on using CY2304, refer to the application note “CY2308: Zero Delay Buffer.”

Pin Description

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5V tolerant input
2	CLKA1[2]	Clock output, Bank A
3	CLKA2[2]	Clock output, Bank A
4	GND	Ground
5	CLKB1[2]	Clock output, Bank B
6	CLKB2[2]	Clock output, Bank B
7	V_{DD}	3.3V Supply
8	FBK	PLL feedback input

Maximum Ratings

Supply Voltage to Ground Potential–0.5V to +7.0V

DC Input Voltage (Except Ref)–0.5V to V_{DD} + 0.5V

DC Input Voltage REF–0.5 to 7V

Storage Temperature –65°C to +150°C

Max. Soldering Temperature (10 sec.) 260°C

Junction Temperature 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015)>2000V

Operating Conditions for CY2304SC-X Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[3]		7	pF

Electrical Characteristics for CY2304SC-X Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage[4]	I_{OL} = 8 mA (–1, –2)		0.4	V
V_{OH}	Output HIGH Voltage[4]	I_{OH} = –8 mA (–1, –2)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		12.0	µA
I_{DD}	Supply Current	Unloaded outputs, 100-MHz REF, Select inputs at V_{DD} or GND		45.0	mA
		Unloaded outputs, 66-MHz REF (–1,–2)		32.0	mA
		Unloaded outputs, 33-MHz REF (–1,–2)		18.0	mA

Notes:

1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Applies to both Ref Clock and FBK.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for CY2304SC-X Commercial Temperature Devices [5]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency	15-pF load, –1, –2 devices	10		133.3	MHz
	Duty Cycle[4] = $t_2 \div t_1$ (–1,–2)	Measured at 1.4V, F_{OUT} = 66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle[4] = $t_2 \div t_1$ (–1,–2)	Measured at 1.4V, F_{OUT} < 50.0 MHz 15-pF load	45.0	50.0	55.0	%
t_3	Rise Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 30-pF load			2.20	ns
t_3	Rise Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t_4	Fall Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 30-pF load			2.20	ns
t_4	Fall Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t_5	Output to Output Skew on same Bank (–1,–2)[4]	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–1)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–2)	All outputs equally loaded			400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge[4]	Measured at $V_{DD}/2$		0	±250	ps
t_7	Device to Device Skew[4]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	500	ps
t_J	Cycle to Cycle Jitter[4] (–1)	Measured at 66.67 MHz, loaded outputs, 15-pF load			175	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t_J	Cycle to Cycle Jitter[4] (–2)	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			375	ps
t_{LOCK}	PLL Lock Time[4]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

Note:

5. All parameters are specified with loaded output.

Electrical Characteristics for CY2304SI-X Industrial Temperature Devices

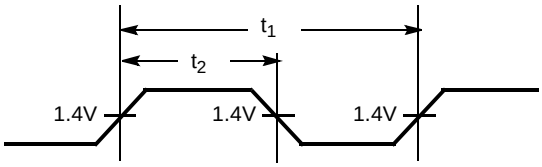
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage[4]	I_{OL} = 8 mA (–1, –2)		0.4	V
V_{OH}	Output HIGH Voltage[4]	I_{OH} = –8 mA (–1, –2)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	µA
I_{DD}	Supply Current	Unloaded outputs, 100 MHz, Select inputs at V_{DD} or GND		45.0	mA
		Unloaded outputs, 66-MHz REF (–1,–2)		35.0	mA
		Unloaded outputs, 33-MHz REF (–1,–2)		20.0	mA

Switching Characteristics for CY2304SI-X Industrial Temperature Devices [5]

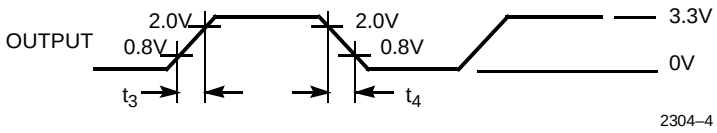
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency	15-pF load, All devices	10		133.3	MHz
	Duty Cycle[4] = $t_2 \div t_1$ (–1,–2)	Measured at 1.4V, F_{OUT} =66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle[4] = $t_2 \div t_1$ (–1,–2)	Measured at 1.4V, F_{OUT} <50.0 MHz 15-pF load	45.0	50.0	55.0	%
t_3	Rise Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 30-pF load			2.50	ns
t_3	Rise Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t_4	Fall Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 30-pF load			2.50	ns
t_4	Fall Time[4] (–1, –2)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t_5	Output to Output Skew on same Bank (–1,–2)[4]	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–1)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–2)	All outputs equally loaded			400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge[4]	Measured at $V_{DD}/2$		0	±250	ps
t_7	Device to Device Skew[4]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	500	ps
t_J	Cycle to Cycle Jitter[4] (–1)	Measured at 66.67 MHz, loaded outputs, 15-pF load			180	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t_J	Cycle to Cycle Jitter[4] (–2)	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			380	ps
t_{LOCK}	PLL Lock Time[4]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

Switching Waveforms

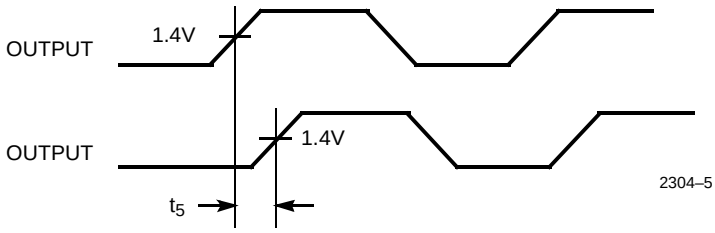
Duty Cycle Timing



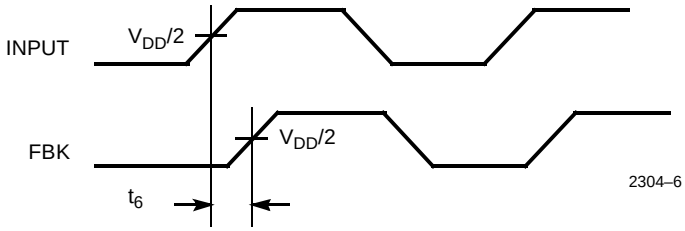
All Outputs Rise/Fall Time



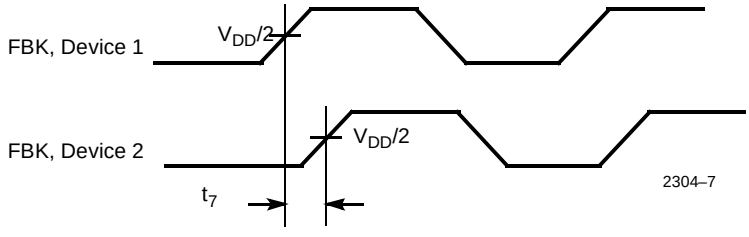
Output-Output Skew



Input-Output Propagation Delay

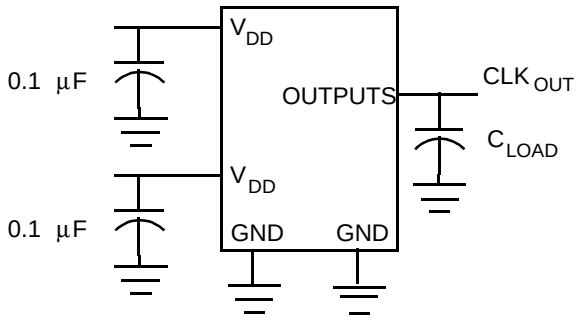


Device-Device Skew



Test Circuits

Test Circuit # 1



Test Circuit for all parameters except t_8

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2304SC–1	S8	8-pin 150-mil SOIC	Commercial
CY2304SI–1	S8	8-pin 150-mil SOIC	Industrial
CY2304SC–2	S8	8-pin 150-mil SOIC	Commercial
CY2304SI–2	S8	8-pin 150-mil SOIC	Industrial

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Package Diagram

8-Lead (150-Mil) SOIC S8