Low-Cost 3.3V Zero Delay Buffer

Features

- 10-MHz to 100-/133-MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input-output propagation delay
- Multiple low-skew outputs
  - Output-output skew less than 250 ps
  - Device-device skew less than 700 ps
  - One input drives five outputs (CY2305)
  - One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309)
- Less than 200 ps cycle-cycle jitter is compatible with Pentium® based systems
- Test Mode to bypass PLL (CY2309 only, see Select Input Decoding table on page 2)
- Available in space-saving 16-pin, 150-mil SOIC or 4.4-mm TSSOP packages (CY2309), and 8-pin, 150-mil SOIC package (CY2305)
- 3.3V operation, advanced 0.65µ CMOS technology
- Industrial Temperature available

Functional Description

The CY2309 is a low-cost 3.3V zero delay buffer designed to distribute high-speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305 is an 8-pin version of the CY2309. It accepts one reference input, and drives out five low-skew clocks. The -1H versions of each device operate at up to 100-/133-MHz frequencies, and have higher drive than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The CY2309 has two banks of four outputs each, which can be controlled by the Select inputs as shown in the Select Input Decoding table on page 2. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

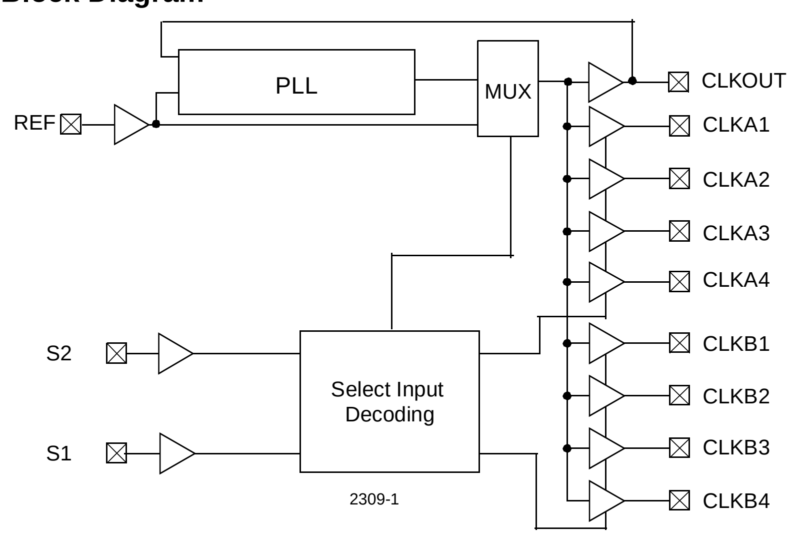
The CY2305 and CY2309 PLLs enter a Power-Down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 12.0 µA of current draw for commercial temperature devices and 25.0 µA for industrial temperature parts. The CY2309 PLL shuts down in one additional case as shown in the table below.

Multiple CY2305 and CY2309 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

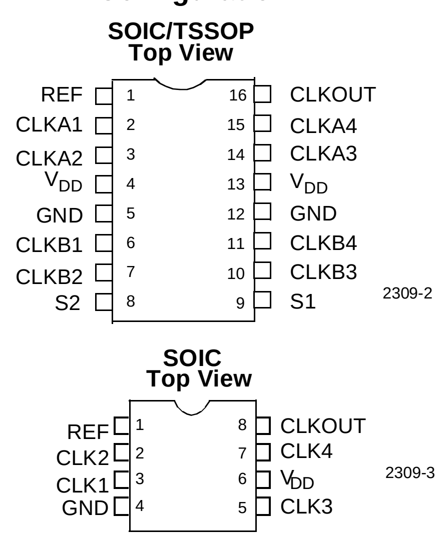
All outputs have less than 200 ps of cycle-cycle jitter. The input to output propagation delay on both devices is guaranteed to be less than 350 ps, and the output to output skew is guaranteed to be less than 250 ps.

The CY2305/CY2309 is available in two/three different configurations, as shown in the ordering information (page 10). The CY2305-1/CY2309-1 is the base part. The CY2305-1H/CY2309-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1's.

Block Diagram



Pin Configuration



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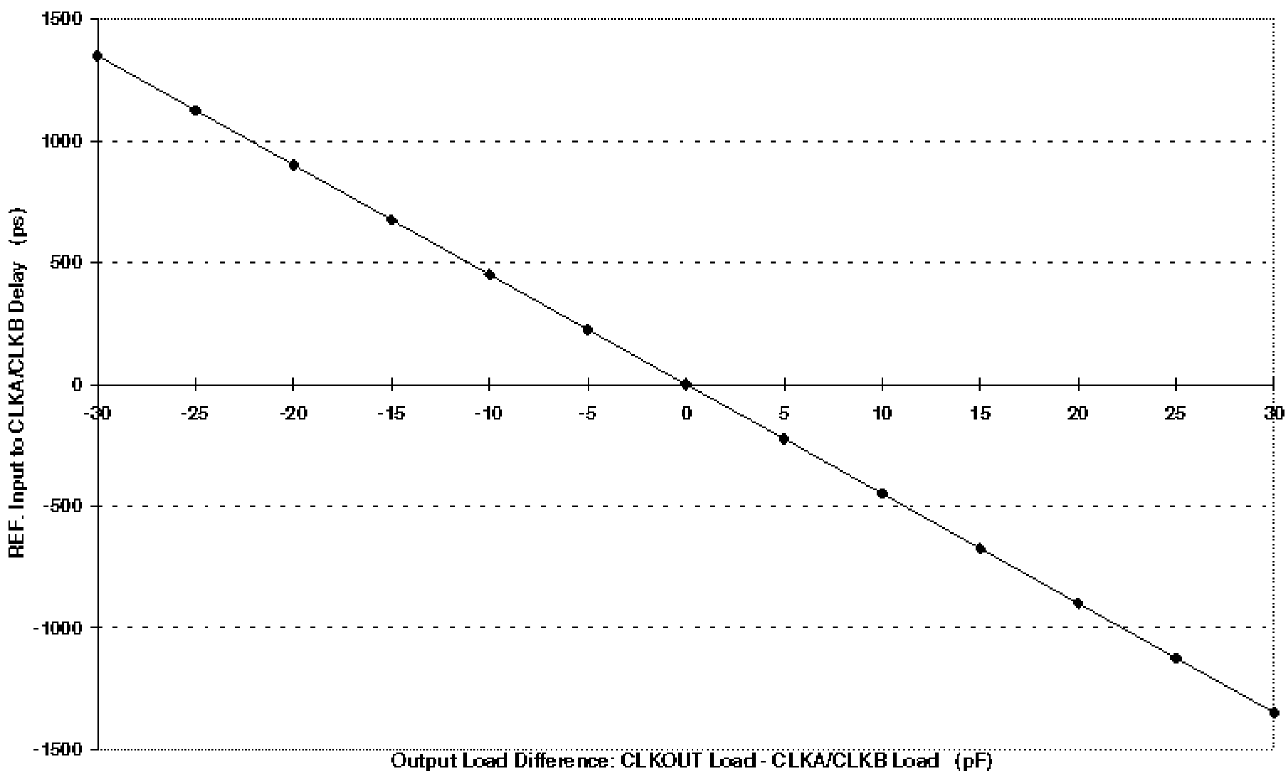
Select Input Decoding for CY2309

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT[1]	Output Source	PLL Shutdown
0	0	Three-State	Three-State	Driven	PLL	N
0	1	Driven	Three-State	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Note:
1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB pins



Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT pin and other outputs.

For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note “CY2305 and CY2309 as PCI and SDRAM Buffers.”

Pin Description for CY2309

Pin	Signal	Description
1	REF[2]	Input reference frequency, 5V-tolerant input
2	CLKA1[3]	Buffered clock output, Bank A
3	CLKA2[3]	Buffered clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[3]	Buffered clock output, Bank B
7	CLKB2[3]	Buffered clock output, Bank B
8	S2[4]	Select input, bit 2
9	S1[4]	Select input, bit 1
10	CLKB3[3]	Buffered clock output, Bank B
11	CLKB4[3]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[3]	Buffered clock output, Bank A
15	CLKA4[3]	Buffered clock output, Bank A
16	CLKOUT[3]	Buffered output, internal feedback on this pin

Pin Description for CY2305

Pin	Signal	Description
1	REF[2]	Input reference frequency, 5V-tolerant input
2	CLK2[3]	Buffered clock output
3	CLK1[3]	Buffered clock output
4	GND	Ground
5	CLK3[3]	Buffered clock output
6	V_{DD}	3.3V supply
7	CLK4[3]	Buffered clock output
8	CLKOUT[3]	Buffered clock output, internal feedback on this pin

Notes:
2. Weak pull-down.
3. Weak pull-down on all outputs.
4. Weak pull-ups on these inputs.

Maximum Ratings

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Input Voltage (Except REF) ....–0.5V to V_{DD} + 0.5V

DC Input Voltage REF .... –0.5V to 7V

Storage Temperature .... –65°C to +150°C

Max. Soldering Temperature (10 sec.) .... 260°C

Junction Temperature .... 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .... >2,000V

Operating Conditions for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage[5]			0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (-1) I_{OH} = 12 mA (-1H)		0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (-1) I_{OL} = –12 mA (-1H)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		12.0	µA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}		32.0	mA

Switching Characteristics for CY2305SC-1and CY2309SC-1 Commercial Temperature Devices[7]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V			2.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V			2.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded			250	ps
t_6	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$		0	±350	ps
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices		0	700	ps
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin			1.0	ms

Notes:
5. REF input has a threshold voltage of $V_{DD}/2$.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.
7. All parameters specified with loaded outputs.

Switching Characteristics for CY2305SC-1H and CY2309SC-1H Commercial Temperature Devices[7]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} <50.0 MHz	45.0	50.0	55.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V			1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V			1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded			250	ps
t_6	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at V_{DD}/2		0	±350	ps
t_7	Device to Device Skew[6]	Measured at V_{DD}/2 on the CLKOUT pins of devices		0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/ns
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin			1.0	ms

Operating Conditions for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage[5]			0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (-1) I_{OH} =12 mA (-1H)		0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (-1) I_{OL} = –12 mA (-1H)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	µA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}		35.0	mA

Switching Characteristics for CY2305SI-1and CY2309SI-1 Industrial Temperature Devices[7]

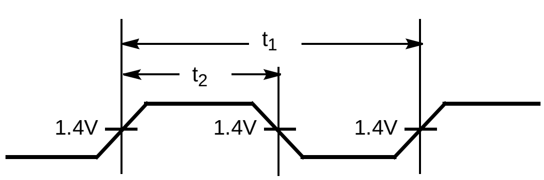
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V			2.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V			2.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded			250	ps
t_6	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at V_{DD}/2		0	±350	ps
t_7	Device to Device Skew[6]	Measured at V_{DD}/2 on the CLKOUT pins of devices		0	700	ps
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin			1.0	ms

Switching Characteristics for CY2305SC-1H and CY2309SC-1H Industrial Temperature Devices[7]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} < 50.0 MHz	45.0	50.0	55.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V			1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V			1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded			250	ps
t_6	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at V_{DD}/2		0	±350	ps
t_7	Device to Device Skew[6]	Measured at V_{DD}/2 on the CLKOUT pins of devices		0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/ns
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin			1.0	ms

Switching Waveforms

Duty Cycle Timing



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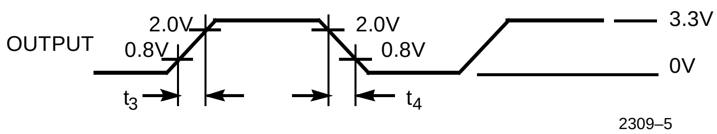
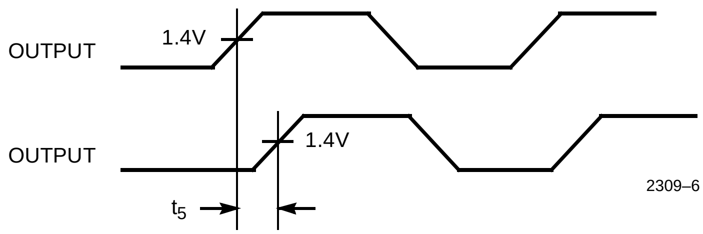
Switching Waveforms (continued)

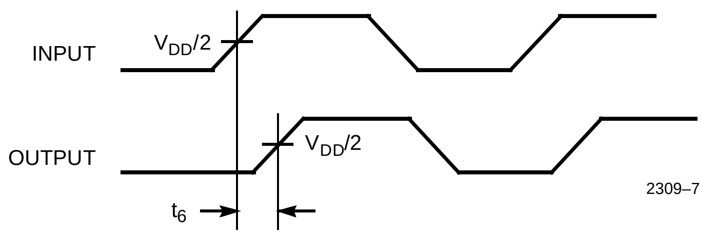
All Outputs Rise/Fall Time



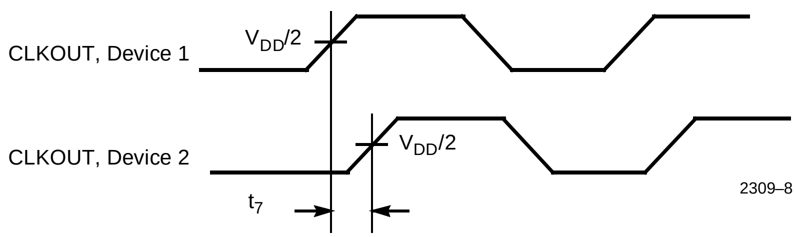
Output-Output Skew



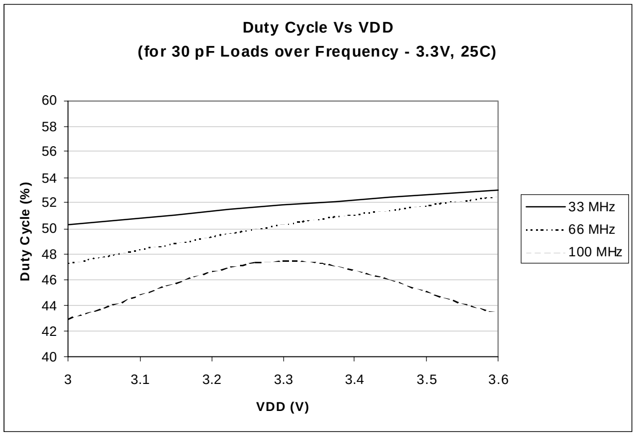
Input-Output Propagation Delay

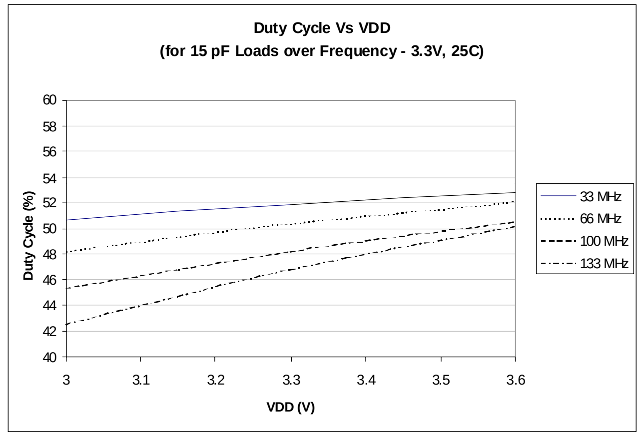


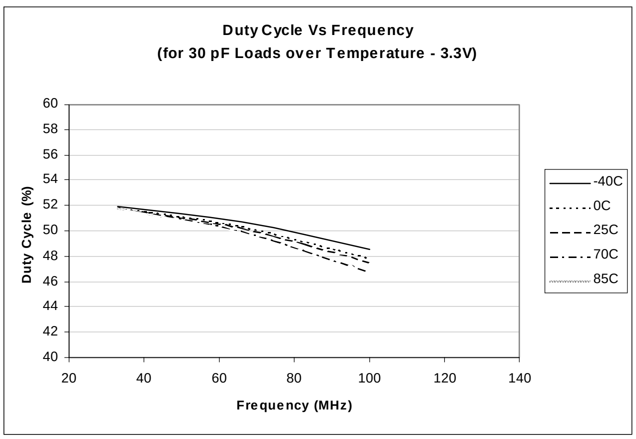
Device-Device Skew

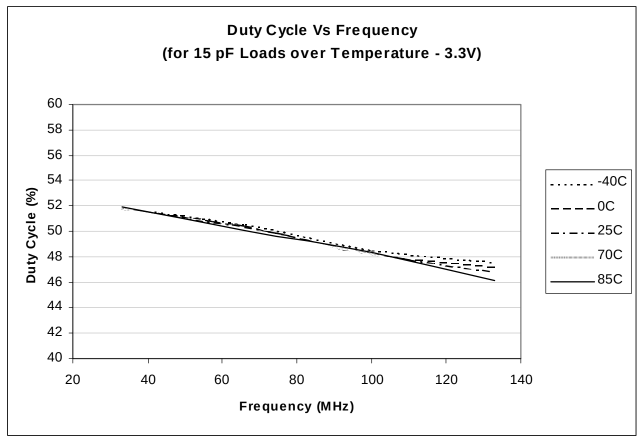


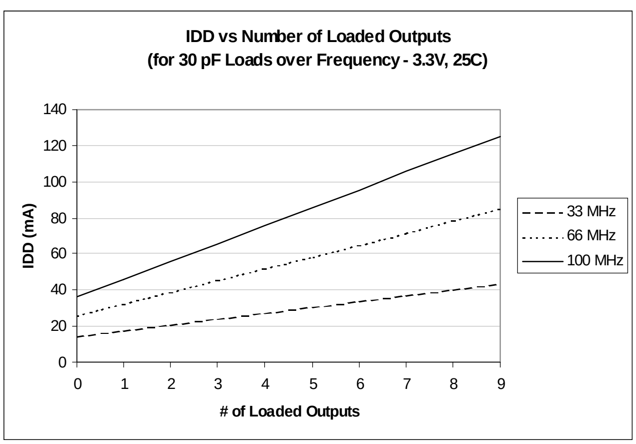
Typical Duty Cycle[8] and I_{DD} Trends[9] for CY2305-1 and CY2309-1

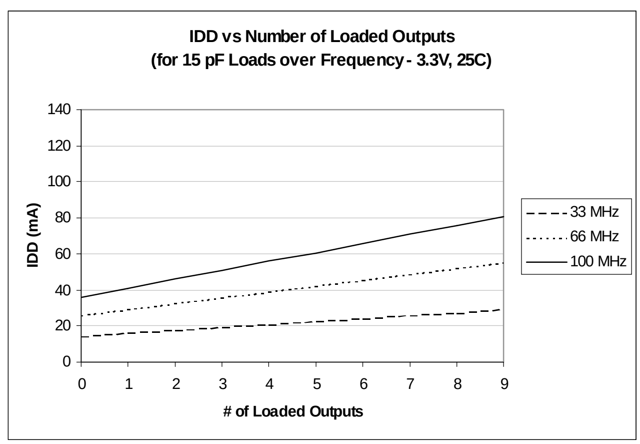








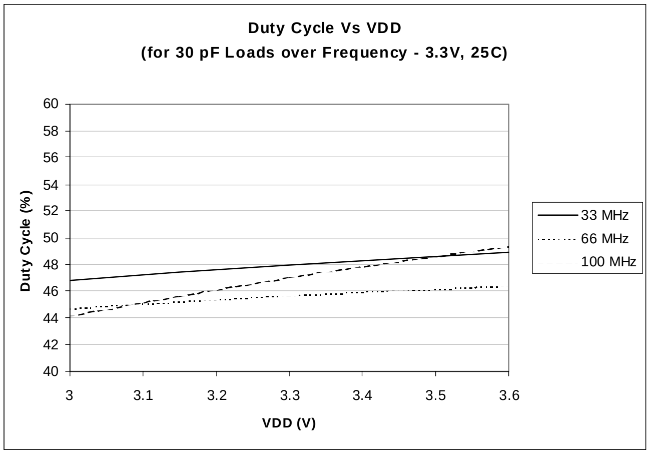


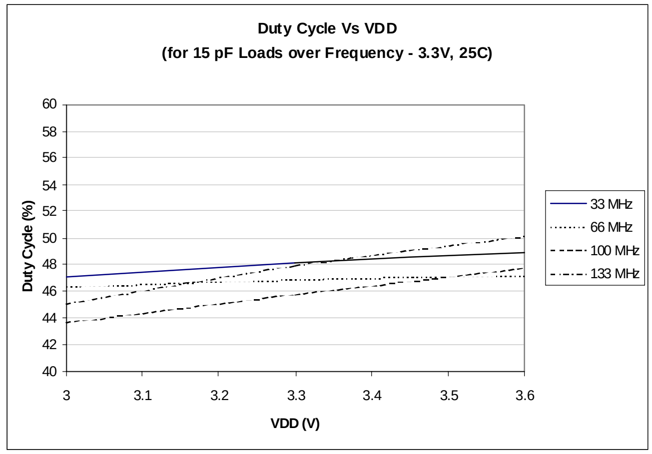


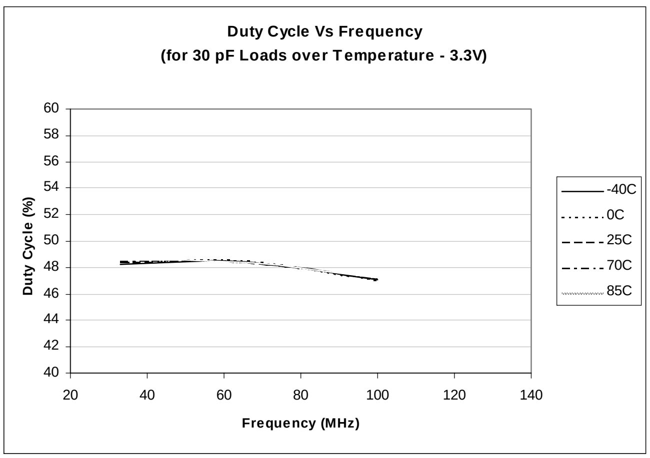
Notes:

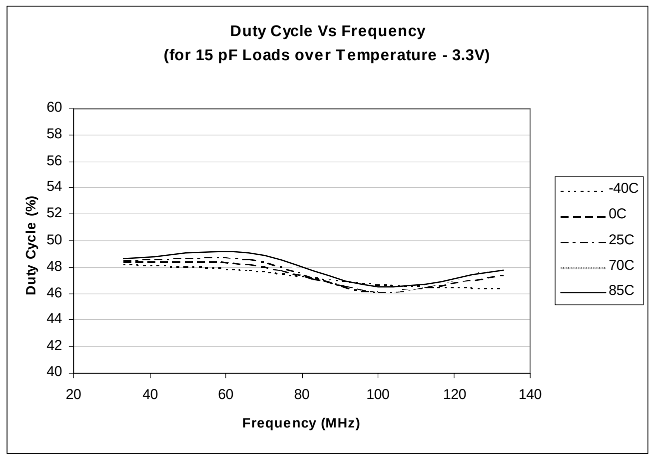
8. Duty Cycle is taken from typical chip measured at 1.4V.
9. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current.
(n = # of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = frequency (Hz))

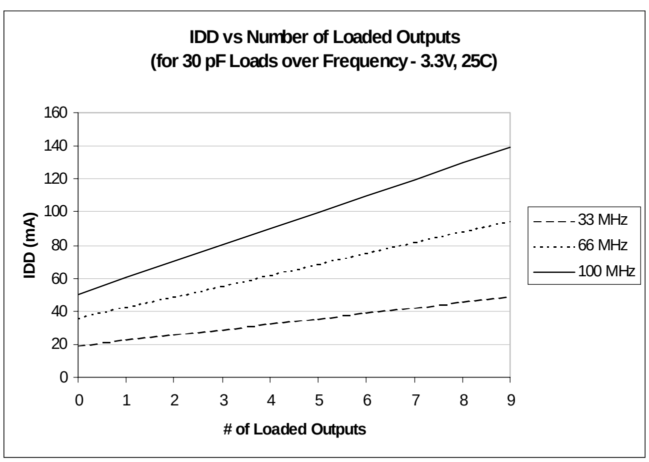
Typical Duty Cycle[8] and I_{DD} Trends[9] for CY2305-1H and CY2309-1H

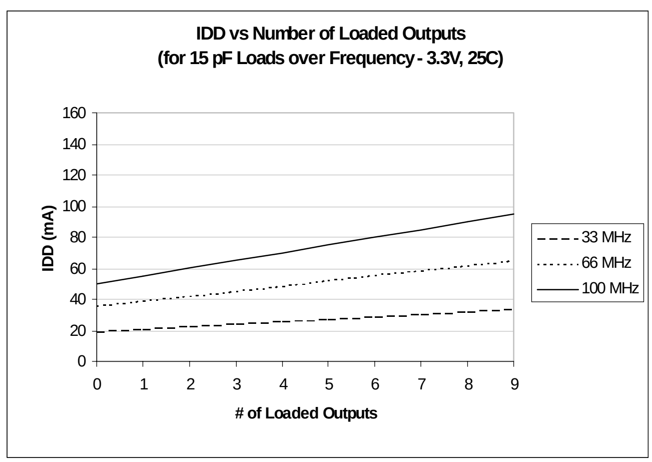




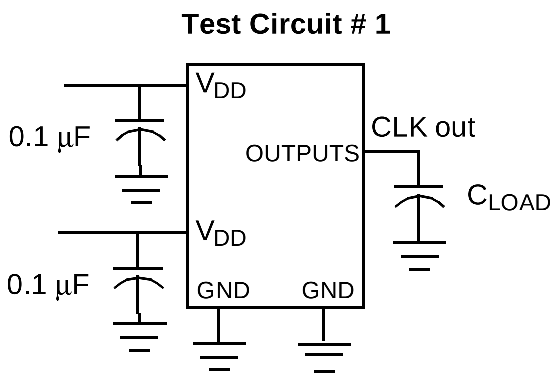


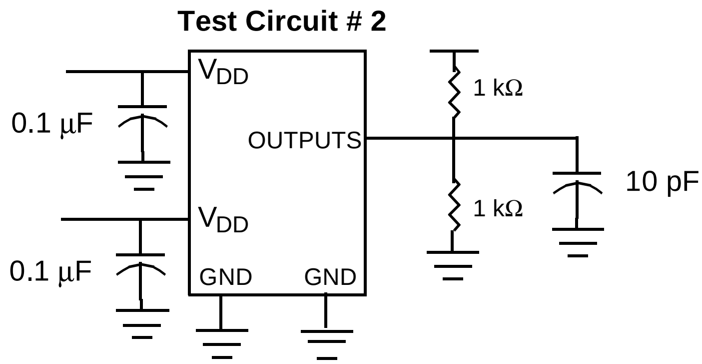






Test Circuits





For parameter t_8 (output slew rate) on -1H devices

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2305SC-1	S8	8-pin 150-mil SOIC	Commercial
CY2305SI-1	S8	8-pin 150-mil SOIC	Industrial
CY2305SC-1H	S8	8-pin 150-mil SOIC	Commercial
CY2305SI-1H	S8	8-pin 150-mil SOIC	Industrial
CY2309SC-1	S16	16-pin 150-mil SOIC	Commercial
CY2309SI-1	S16	16-pin 150-mil SOIC	Industrial
CY2309SC-1H	S16	16-pin 150-mil SOIC	Commercial
CY2309SI-1H	S16	16-pin 150-mil SOIC	Industrial
CY2309ZC-1H	Z16	16-pin 4.4-mm TSSOP	Commercial
CY2309ZI-1H	Z16	16-pin 4.4-mm TSSOP	Industrial

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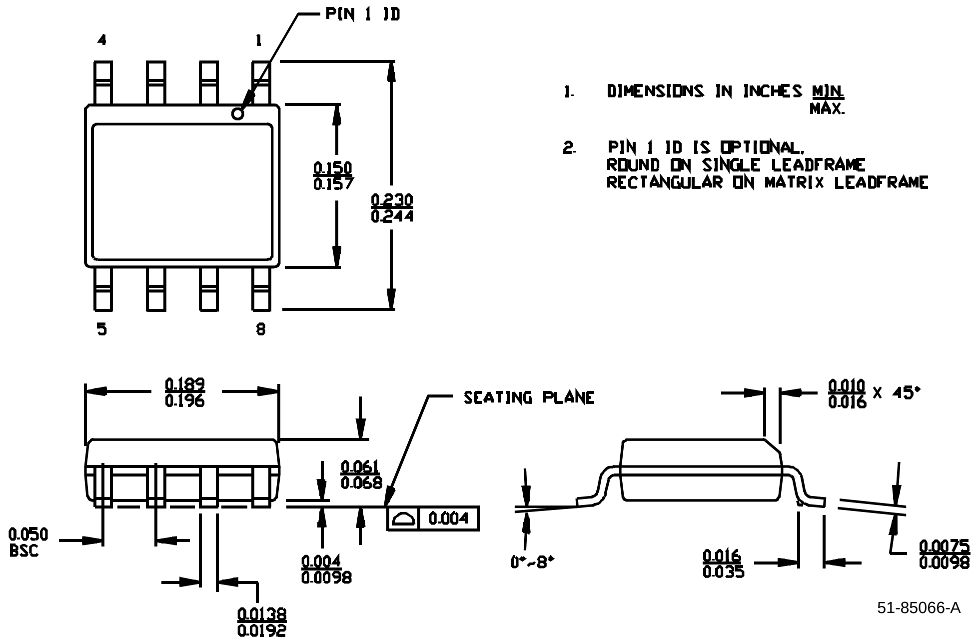
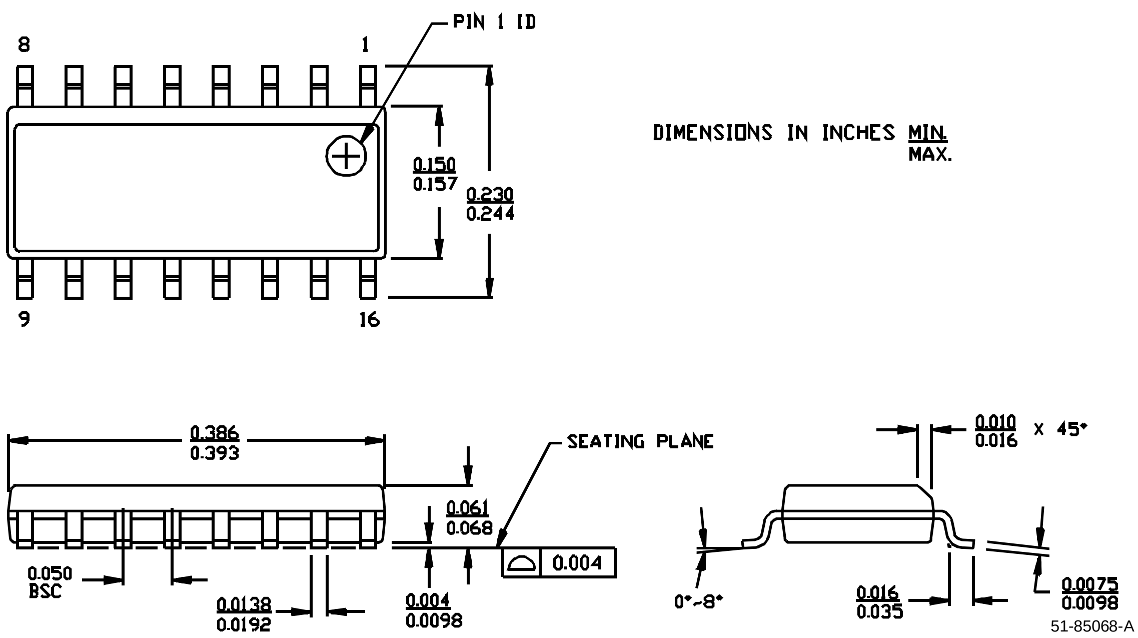
Package Diagrams

8-Lead (150-Mil) SOIC S8

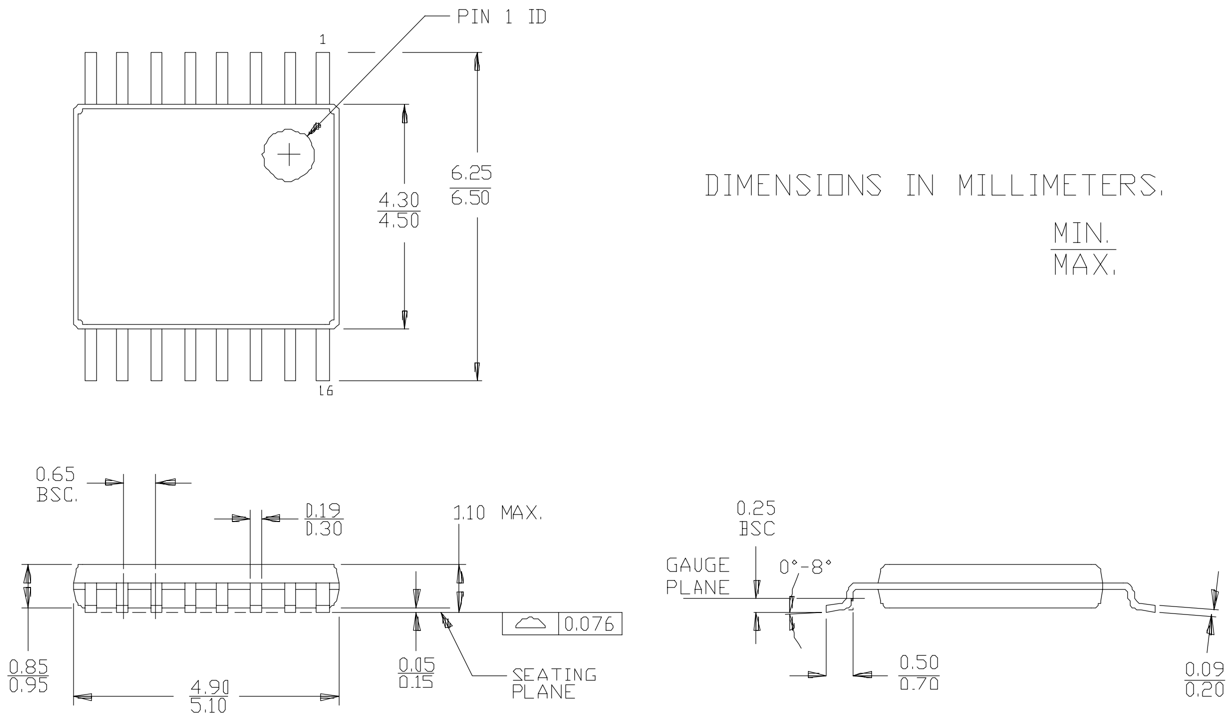


16-Lead (150-Mil) Molded SOIC S16



Package Diagrams (continued)

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



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