



3.3V SDRAM Buffer for Mobile PCs with 4 SO-DIMMs

Features

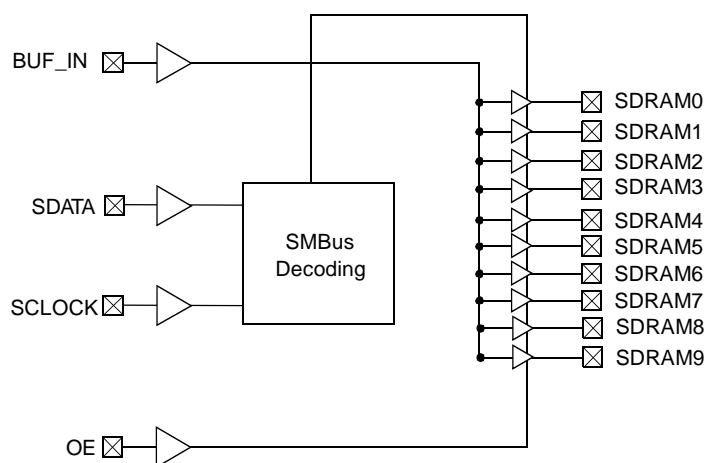
- One input to 10 output buffer/driver
- Supports up to four SDRAM SO-DIMMs
- Two additional outputs for feedback
- SMBus interface for output control
- Low skew outputs
- Up to 100 MHz operation
- Multiple V_{DD} and V_{SS} pins for noise reduction
- Dedicated OE pin for testing
- Space-saving 28-pin SSOP package
- 3.3V operation

Functional Description

The CY2310BNZ is a 3.3V buffer designed to distribute high-speed clocks in mobile PC applications. The part has 10 outputs, 8 of which can be used to drive up to four SDRAM SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium II® processors. The CY2310BNZ can be used in conjunction with the CY2281 or similar clock synthesizer for a full Pentium II motherboard solution.

The CY2310BNZ also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled. A separate Output Enable pin facilitates testing on ATE.

Block Diagram



Pin Configuration

28-pin SSOP Top View

V_{DD}	1	28	V_{DD}
SDRAM0	2	27	SDRAM7
SDRAM1	3	26	SDRAM6
V_{SS}	4	25	V_{SS}
V_{DD}	5	24	V_{DD}
SDRAM2	6	23	SDRAM5
SDRAM3	7	22	SDRAM4
V_{SS}	8	21	V_{SS}
BUF_IN	9	20	OE
V_{DD}	10	19	V_{DD}
SDRAM8	11	18	SDRAM9
V_{SS}	12	17	V_{SS}
V_{DDIIC}	13	16	V_{SSIIC}
SDATA	14	15	SCLOCK

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Pin Summary

Name	Pins	Description
V _{DD}	1, 5, 10, 19, 24, 28	3.3V Digital voltage supply
V _{SS}	4, 8, 12, 17, 21, 25	Ground
V _{DDIIC}	13	SMBus Voltage supply
V _{SSIIC}	16	Ground for SMBus
BUF_IN	9	Input clock
OE	20	Output Enable, three-states outputs when LOW. Internal pull-up to V _{DD}
SDATA	14	SMBus data input, internal pull-up to V _{DD}
SCLK	15	SMBus clock input, internal pull-up to V _{DD}
SDRAM [0–3]	2, 3, 6, 7	SDRAM byte 0 clock outputs
SDRAM [4–7]	22, 23, 26, 27	SDRAM byte 1 clock outputs
SDRAM [8–9]	11, 18	SDRAM byte 2 clock outputs

Device Functionality

OE	SDRAM [0–17]
0	High-Z
1	1 x BUF_IN

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to “0”.
- SMBus Address for the CY2310BNZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 1: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	27	SDRAM7 (Active/Inactive)
Bit 6	26	SDRAM6 (Active/Inactive)
Bit 5	23	SDRAM5 (Active/Inactive)
Bit 4	22	SDRAM4 (Active/Inactive)
Bit 3	--	Initialize to 0
Bit 2	--	Initialize to 0
Bit 1	--	Initialize to 0
Bit 0	--	Initialize to 0

Byte 0: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enabled

Bit	Pin #	Description
Bit 7	--	Initialize to 0
Bit 6	--	Initialize to 0
Bit 5	--	Initialize to 0
Bit 4	--	Initialize to 0
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

Byte 2: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	18	SDRAM9 (Active/Inactive)
Bit 6	11	SDRAM8 (Active/Inactive)
Bit 5	--	Reserved, drive to 0
Bit 4	--	Reserved, drive to 0
Bit 3	--	Reserved, drive to 0
Bit 2	--	Reserved, drive to 0
Bit 1	--	Reserved, drive to 0
Bit 0	--	Reserved, drive to 0

Maximum Ratings

Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage (Except BUF_IN) -0.5V to $V_{DD} + 0.5V$
 DC Input Voltage (BUF_IN) -0.5V to +7.0V

Storage Temperature -65°C to +150°C
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015) >2000V
 Ambient Temperature under BIAS -55°C to +125°C

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Operating Temperature (Ambient Temperature)	-40	85	°C
C_L	Load Capacitance	20	30	pF
C_{IN}	Input Capacitance		5	pF

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any Pin with Respect to GND	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	-55 to +125	°C

DC Electrical Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 5\%$

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
I_{DD}	3.3V Supply Current	at 64MHz	100	140	180	mA
I_{DD}	3.3V Supply Current	at 100 MHz	150	185	220	mA
I_{DD} Tristate	3.3V Supply Current in Three-State			5	10	mA
Logic Inputs						
V_{IL}	Input Low Voltage		$V_{SS}-0.3$		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{DD}+0.5$	V
I_{ILEAK}	Input Leakage Current, BUF_IN		-5		+5	μA
I_{ILEAK}	Input Leakage Current ^[1]		-20		+5	μA
Logic Outputs (SDRAM0:9)^[2]						
V_{OL}	Output Low Voltage	$I_{OL} = 1 \text{ mA}$			50	mV
V_{OH}	Output High Voltage	$I_{OH} = -1 \text{ mA}$	3.1			V
I_{OL}	Output Low Current	$V_{OL} = 1.5\text{V}$	70	110	185	mA
I_{OH}	Output High Current	$V_{OH} = 1.5\text{V}$	65	100	160	mA
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

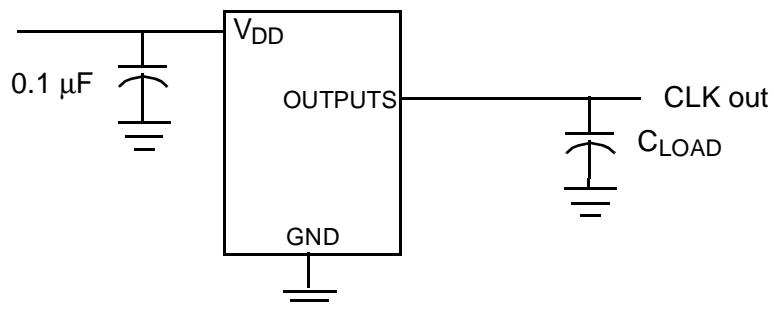
Notes:

1. OE, SDATA, and SCLOCK logic pins have a 250-k Ω internal pull-up resistor ($V_{DD} - 0.8\text{V}$).
2. All SDRAM outputs loaded by 6" transmission lines with 22-pF capacitors on ends.

AC Electrical Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 5\%$ (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	at 64 MHz	0		133	MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
t_{SR}	Output Skew, Rising Edges				200	ps
t_{SF}	Output Skew, Falling Edges				200	ps
t_{EN}	Output Enable Time		1.0		8.0	ns
t_{DIS}	Output Disable Time		1.0		8.0	ns
t_{PR}	Rising Edge Propagation Delay		3.0	3.85	5.0	ns
t_{PF}	Falling Edge Propagation Delay		3.0	3.85	5.0	ns
t_D	Duty Cycle	Measured at 1.5V	50		60	%
Z_o	AC Output Impedance			15		Ω

Test Circuit



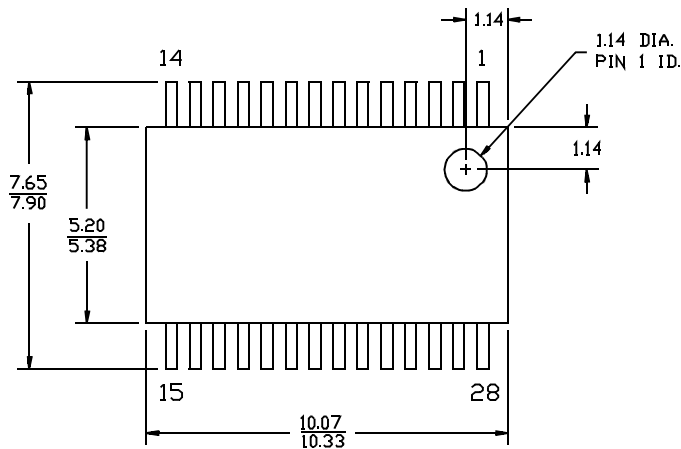
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2310BNZPVI-1	O28	28-pin SSOP	Industrial (-40 to 85°)

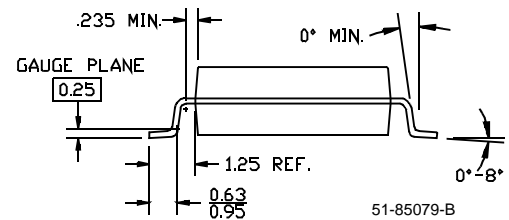
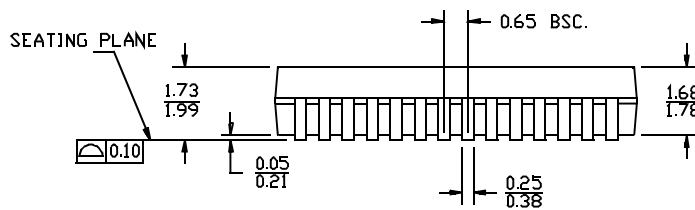
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Package Diagram

28-Lead (210-Mil) Shrunk Small Outline Package O28



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