



## 13 Output, 3.3V SDRAM Buffer for Desktop PCs with 3 DIMMs

### Features

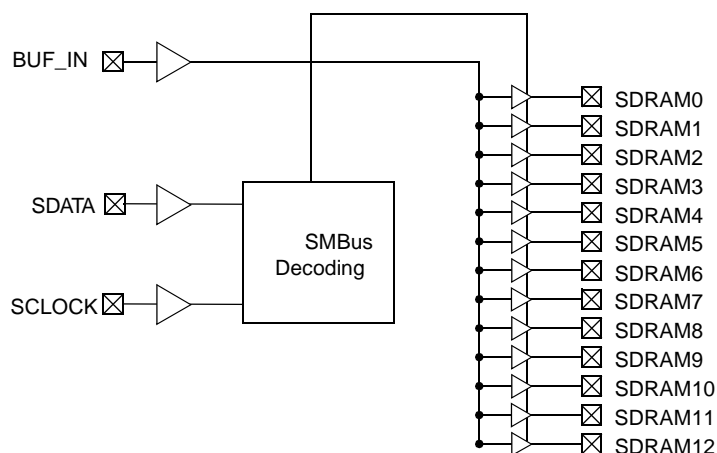
- One input to 13 output buffer/driver
- Supports up to three SDRAM DIMMs
- One additional outputs for feedback
- SMBus interface for output control
- Low skew outputs
- Up to 100 MHz operation
- Multiple  $V_{DD}$  and  $V_{SS}$  pins for noise reduction
- Low EMI outputs
- 28-pin SOIC (300-mil) package
- 3.3V operation

### Functional Description

The CY2313BNZ is a 3.3V buffer designed to distribute high-speed clocks in desktop PC applications. The part has 13 outputs, 12 of which can be used to drive up to three SDRAM DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, thus making it compatible with Pentium® II processors. The CY2313BNZ can be used in conjunction with the CY2280, CY2281, CY2282 or similar clock synthesizer for a complete Pentium II motherboard solution.

The CY2313BNZ also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled.

### Block Diagram



### Pin Configuration

#### 28 SOIC Top View

$V_{DD}$	1	28	$V_{DD}$
SDRAM0	2	27	SDRAM11
SDRAM1	3	26	SDRAM10
$V_{SS}$	4	25	$V_{SS}$
$V_{DD}$	5	24	$V_{DD}$
SDRAM2	6	23	SDRAM9
SDRAM3	7	22	SDRAM8
$V_{SS}$	8	21	$V_{SS}$
BUF_IN	9	20	$V_{DD}$
SDRAM4	10	19	SDRAM7
SDRAM5	11	18	SDRAM6
SDRAM12	12	17	$V_{SS}$
$V_{DDIIC}$	13	16	$V_{SSIIC}$
SDATA	14	15	SCLK

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## Pin Summary

Name	Pins	Description
V <sub>DD</sub>	1, 5, 20, 24, 28	3.3V Digital voltage supply
V <sub>SS</sub>	4, 8, 17, 21, 25	Ground
V <sub>DDIIC</sub>	13	SMBus Voltage supply
V <sub>SSIIC</sub>	16	Ground for SMBus
BUF_IN	9	Input clock
SDATA	14	SMBus data input, internal pull-up to V <sub>DD</sub>
SCLK	15	SMBus clock input, internal pull-up to V <sub>DD</sub>
SDRAM [0-12]	2, 3, 6, 7, 10, 11, 12, 18, 19, 22, 23, 26, 27	SDRAM clock outputs

## Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:
  - Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
  - ...
  - Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0
- Reserved and unused bits should be programmed to "0"
- SMBus Address for the CY2313BNZ is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

## Byte 0: SDRAM Active/Inactive Register (1 = Enable, 0 = Disable), Default = Enabled

Bit	Pin #	Description
Bit 7	11	SDRAM5 (Active/Inactive)
Bit 6	10	SDRAM4 (Active/Inactive)
Bit 5	--	Reserved, drive to 0
Bit 4	--	Reserved, drive to 0
Bit 3	7	SDRAM3 (Active/Inactive)
Bit 2	6	SDRAM2 (Active/Inactive)
Bit 1	3	SDRAM1 (Active/Inactive)
Bit 0	2	SDRAM0 (Active/Inactive)

## Byte 1: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	27	SDRAM11 (Active/Inactive)
Bit 6	26	SDRAM10 (Active/Inactive)
Bit 5	23	SDRAM9 (Active/Inactive)
Bit 4	22	SDRAM8 (Active/Inactive)
Bit 3	--	Reserved, drive to 0
Bit 2	--	Reserved, drive to 0
Bit 1	19	SDRAM7 (Active/Inactive)
Bit 0	18	SDRAM6 (Active/Inactive)

## Byte 2: SDRAM Active/Inactive Register (1 = Active, 0 = Inactive), Default = Active

Bit	Pin #	Description
Bit 7	--	Reserved, drive to 0
Bit 6	12	SDRAM12 (Active/Inactive)
Bit 5	--	Reserved, drive to 0
Bit 4	--	Reserved, drive to 0
Bit 3	--	Reserved, drive to 0
Bit 2	--	Reserved, drive to 0
Bit 1	--	Reserved, drive to 0
Bit 0	--	Reserved, drive to 0

## Maximum Ratings

Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Input Voltage (Except BUF\_IN) ..... -0.5V to  $V_{DD} + 0.5V$   
 DC Input Voltage (BUF\_IN) ..... -0.5V to +7.0V

Storage Temperature ..... -65°C to +150°C  
 Static Discharge Voltage  
 (per MIL-STD-883, Method 3015) ..... >2000V  
 Ambient Temperature under BIAS ..... -55°C to +125°C

## Operating Conditions<sup>[1]</sup>

Parameter	Description	Min.	Max.	Unit
$V_{DD}$	Supply Voltage	3.135	3.465	V
$T_A$	Operating Temperature (Ambient Temperature)	-40	85	°C
$C_L$	Load Capacitance		30	pF

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Operating Temperature	0 to +70	°C
$T_B$	Ambient Temperature under Bias	-55 to +125	°C

## DC Electrical Characteristics: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{DD} = 3.3V \pm 5\%$

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
$I_{DD}$	3.3V Supply Current	BUF_IN = 100 MHz			250	mA
<b>Logic Inputs</b>						
$V_{IL}$	Input Low Voltage		GND-0.3		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DD} + 0.5$	V
$I_{ILEAK}$	Input Leakage Current, BUF_IN		-5		+5	μA
$I_{ILEAK}$	Input Leakage Current <sup>[1]</sup>		-20		+5	μA
<b>Logic Outputs (SDRAM0:12)</b>						
$V_{OL}$	Output Low Voltage	$I_{OL} = 1\text{ mA}$			50	mV
$V_{OH}$	Output High Voltage	$I_{OH} = -1\text{ mA}$	3.1			V
$I_{OL}$	Output Low Current	$V_{OL} = 1.5V$	65	100	160	mA
$I_{OH}$	Output High Current	$V_{OH} = 1.5V$	70	110	185	mA
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance				5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

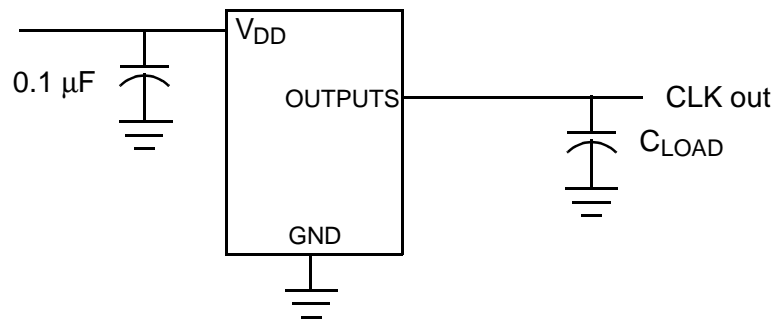
**Note:**

1. SDATA and SCLOCK logic pins have 250-kΩ internal pull-up resistors.

**AC Electrical Characteristics:**  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$  (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition	Min	Typ	Max	Unit
$f_{IN}$	Input Frequency		0		133	MHz
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1.5		4.0	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1.5		4.0	V/ns
$t_{SR}$	Output Skew, Rising Edges				250	ps
$t_{SF}$	Output Skew, Falling Edges				250	ps
$t_{EN}$	Output Enable Time		1.0		8.0	ns
$t_{DIS}$	Output Disable Time		1.0		8.0	ns
$t_{PR}$	Rising Edge Propagation Delay		1.0		5.0	ns
$t_{PF}$	Falling Edge Propagation Delay		1.0		5.0	ns
$t_D$	Duty Cycle	Measured at 1.5V	45		55	%
$Z_o$	AC Output Impedance			15		$\Omega$
$t_{PR}$	Rising Edge Propagation Delay		1.0		5.0	ns

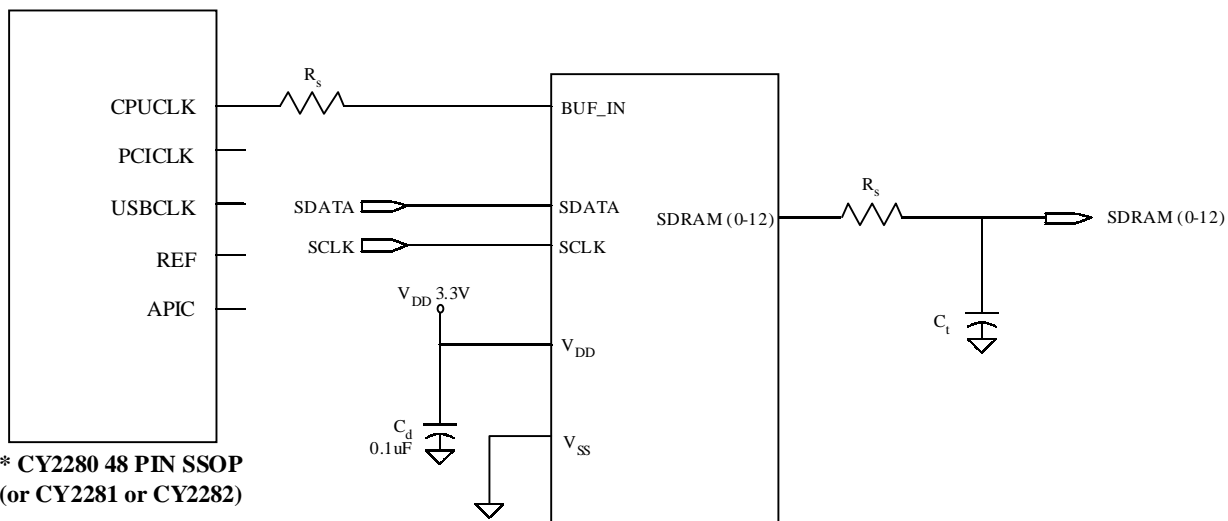
### Test Circuit



## Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

## Application Circuit



\* CY2280 48 PIN SSOP  
(or CY2281 or CY2282)

**CY2313A: 28-PIN SOIC**

\* THIS FREQUENCY SYNTHESIZER IS USED TO  
GENERATE CPU, PCI, USB, REF, AND APIC CLOCKS.

$C_d$  = DECOUPLING CAPACITORS  
 $C_t$  = OPTIONAL EMI-REDUCING CAPACITORS  
 $R_s$  = SERIES TERMINATING RESISTORS

## Summary

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 mF. In some cases, smaller value capacitors may be required.
- The value of the series terminating resistor satisfies the following equation, where  $R_{trace}$  is the loaded characteristic impedance of the trace,  $R_{out}$  is the output impedance of the buffer (typically 25W), and  $R_{series}$  is the series terminating resistor.  
 $R_{series} > R_{trace} - R_{out}$
- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating

resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.

- A Ferrite Bead **may** be used to isolate the Board  $V_{DD}$  from the clock generator  $V_{DD}$  island. Ensure that the Ferrite Bead offers greater than 50W impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.
- If a Ferrite Bead is used, a 10 mF–22 mF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

## Ordering Information

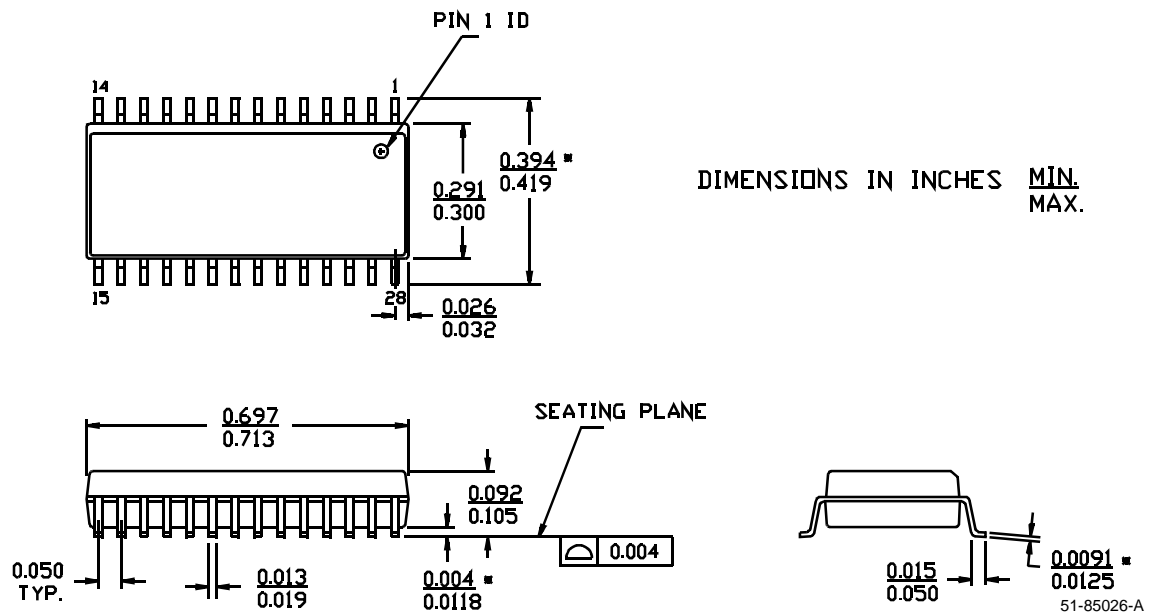
Ordering Code	Package Name	Package Type	Operating Range
CY2313BNZSI CY2313BNZPVI* CY2313BNZZI*	S21	28-Pin SOIC 28-Pin SSOP 28-Pin TSSOP	Industrial Industrial Industrial

\*Call factory for availability

Document #: 38-01090-\*\*

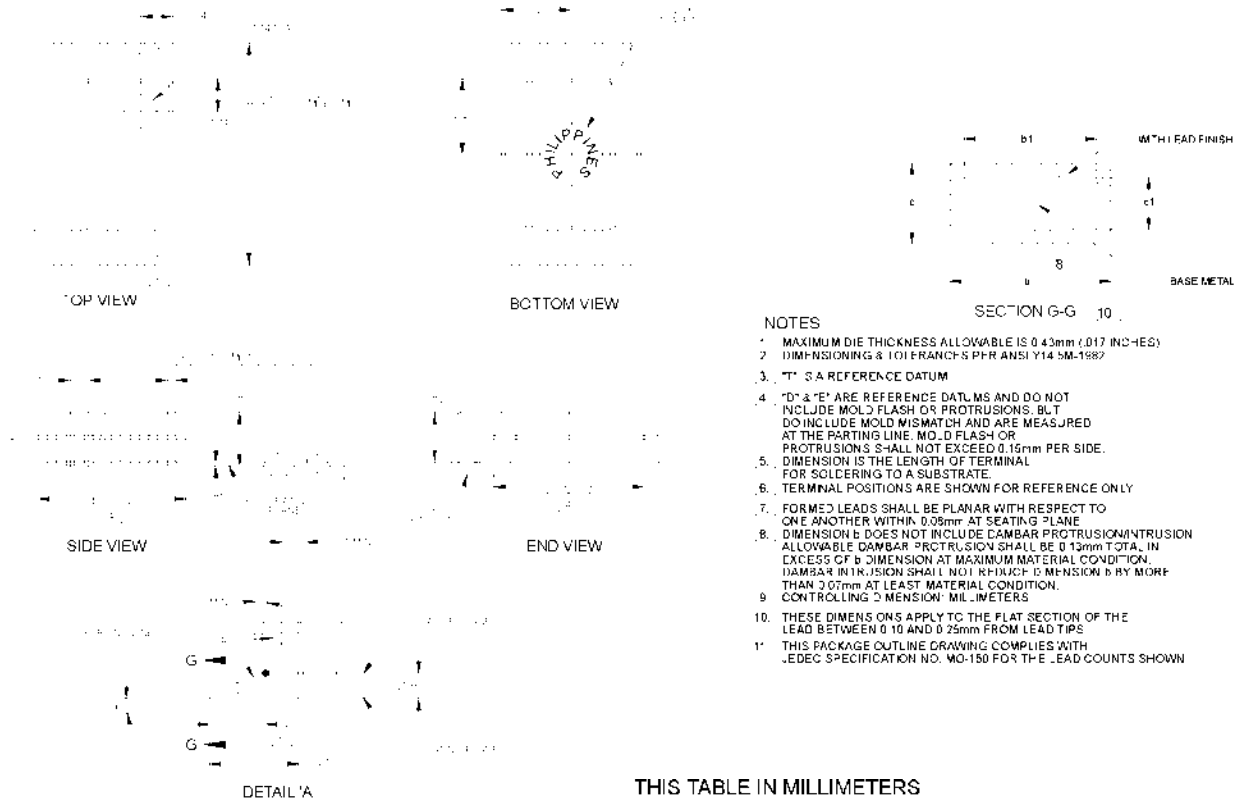
## Package Diagram

28-Lead (300-Mil) Molded SOIC S21



## Package Diagram

### 28-Pin Shrunk Small Outline Package (SSOP, 209-mil)



#### THIS TABLE IN MILLIMETERS

	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	1.73	1.89	1.99	AA	6.07	6.20	6.33	14
A	0.05	0.13	0.21	AF	6.07	6.20	6.33	15
A	1.68	1.73	1.78	AC	7.07	7.20	7.33	23
b	0.25	-	0.38	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	AI	10.07	10.20	10.33	33
c1	0.09	0.15	0.16					
D	SEE VARIATIONS							
E	5.20	5.30	5.38					
e	0.65 BSC							
H	7.65	7.80	7.90					
L	0.63	0.75	0.95					
L1	1.25 REF							
N	SEE VARIATIONS							
R	0" 0.09	4" 0.15	8"					

VARIATION AF

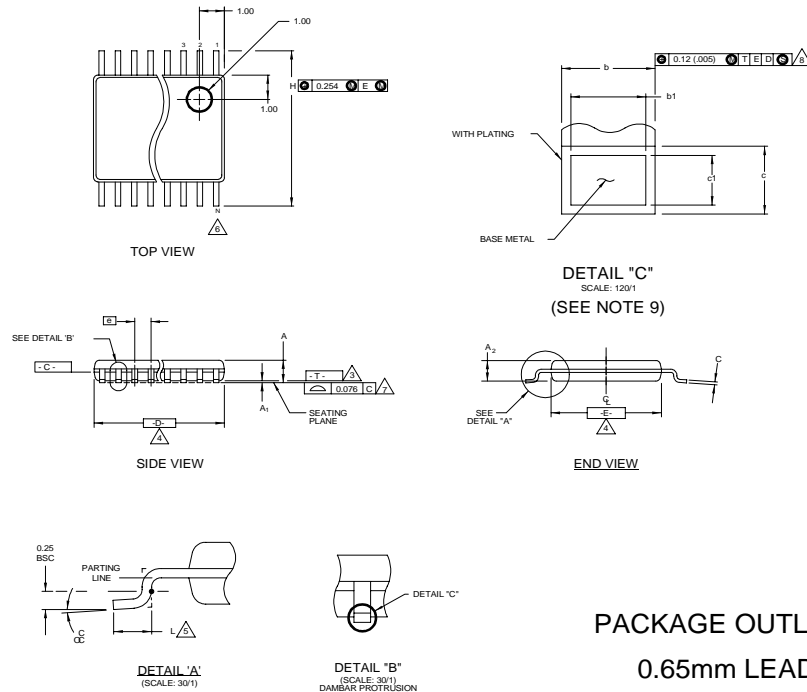
IS DESIGNED BUT NOT TOOLED

#### THIS TABLE IN INCHES

	COMMON DIMENSIONS			NOTE VARIATIONS	4 D			6 N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.068	.073	.078	AA	.239	.244	.249	14
A	.007	.005	.008	AF	.239	.244	.249	15
A	.065	.068	.070	AC	.278	.284	.289	23
b	.010	-	.015	AD	.318	.323	.328	24
b1	.010	.012	.013	AE	.397	.402	.407	28
c	.004	-	.008	AI	.397	.402	.407	33
c1	.004	.006	.006					
D	SEE VARIATIONS							
E	.209	.209	.212					
e	.0258 BSC							
H	.301	.307	.311					
L	.025	.030	.037					
L1	.049 REF							
N	SEE VARIATIONS							
R	0" .004	4" .006	8"					

## Package Diagram

### 28-Pin Thin Shrunk Small outline Package (TSSOP 173 mi)



#### NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.2790.0127 (.0110012 THICKNESS ALLOWABLE IS 0.279.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
8. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS "B" AND "C".
9. DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.

**PACKAGE OUTLINE, 4.40mm (.173") BODY,  
0.65mm LEAD PITCH, TSSOP**

**THIS TABLE IN MILLIMETERS**

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4			6
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	—	—	1.10	AA	2.90	3.00	3.10	8
A <sub>1</sub>	0.05	0.10	0.15	AB	4.90	5.00	5.10	14
A <sub>2</sub>	0.85	0.90	0.95	AC	4.90	5.00	5.10	16
b	0.19	—	0.30	AD	6.40	6.50	6.60	20
b <sub>1</sub>	0.19	0.22	0.25	AE	7.70	7.80	7.90	24
c	0.090	—	0.20	AF	9.60	9.70	9.80	28
c <sub>1</sub>	0.090	0.127	0.135					
D	SEE VARIATIONS			4				
E	4.30	4.40	4.50	4				
e	0.65 BSC							
H	6.25	6.40	6.50					
L	0.50	0.60	0.70	5				
N	SEE VARIATIONS			6				
α	0	4	8					

**THIS TABLE IN INCHES**

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	4			6
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	—	—	.0433	AA	.114	.118	.122	8
A <sub>1</sub>	.002	.004	.006	AB	.193	.197	.201	14
A <sub>2</sub>	.0335	.0354	.0374	AC	.193	.197	.201	16
b	.0075	—	.0118	AD	.252	.256	.260	20
b <sub>1</sub>	.0075	.0087	.0098	AE	.303	.307	.311	24
c	.0035	—	.0079	AF	.378	.382	.386	28
c <sub>1</sub>	.0035	.0050	.0053					
D	SEE VARIATIONS			4				
E	.169	.173	.177	4				
e	.0256 BSC							
H	.246	.252	.256					
L	.020	.024	.028	5				
N	SEE VARIATIONS			6				
α	0	4	8					